NTC and electrical properties of nickel and gold doped n-type silicon material*

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Abstract: Silicon materials compensated by deep level impurities such as nickel and gold have negative temperature coefficient (NTC) characteristics. In this work, n-type silicon wafers are smeared by nickel chloride ethanol solution and gold chloric acid ethanol solution, and subsequently put in the opening environment to heat. The electrical resistance and *B*-value of the thermistors made by this silicon material are measured and analyzed. When the silicon surface concentration of gold atoms is 2×10^{-6} mol/cm^2, the uniformity of the single-crystal silicon material is optimal. When the diffusion temperature is between 900 and 1000 °C, a material with high *B*-value and low electrical resistivity is obtained. The *B*–*T* and *R*–*T* change laws calculated by the theory of semiconductor deep level energy are basically consistent with the experimental results.

Key words: deep level impurities; nickel; gold; NTC; electrical properties

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1. Introduction

Negative temperature coefficient (NTC) thermistors are thermally sensitive resistors whose resistance decreases with increasing temperature. There is a large choice of NTC materials, and the most widely used materials are oxide ceramic and SiC[1–6]. Single-crystal silicon material that is doped by deep level impurities has thermally-sensitive characteristics. Research on a single transition group metal in silicon with thermally-sensitive characteristics has been reported previously[7–9]. Single gold-doped material has larger electrical resistivity, better uniformity, and a higher *B*-value, while single nickel-doped material has relatively lower electrical resistivity, and the uniformity of material is poor due to the existence of vacancies and interstitials. The *B*-value of silicon material mainly depends on the energy level positions of the impurities. At the same *B*-value, such a material's electrical resistivity is lower than that of oxide ceramic thermally-sensitive material. By selecting appropriate deep level impurities, it is possible to make a kind of NTC silicon material which has high *B*-value and low electrical resistivity.

This paper discusses n-type single-crystal silicon doped by transition group metal elements. Nickel and gold are the choices of two such elements, which are mixed in accordance with certain proportions. Smearing impurities on the surface of silicon wafers, we put them in an opening environment to heat. Nickel is a fast and low solubility transition metal in silicon[10]. A small number of vacant position nickel atoms in the n-type silicon are ionized, and the bulk of the interstitial nickel atoms are electrically neutral. Because fewer defects are present in the single crystal silicon and high-concentration gold atoms are on the silicon surface, lattice displacement plays a major role in the diffusion process[11]. Nickel and gold form complementary mechanisms to each other. Gold atoms in the silicon material occupy the vacancies and suppress the nickel atoms simultaneously. Nickel atoms are distributed in the interstices of single crystal silicon. We can obtain high *B*-value, low electrical resistivity single-crystal silicon material.

2. Physical models

As the electrical resistivity of n-type silicon wafers is 1 Ω·cm, most of the carriers are electrons and silicon is a non-degenerate semiconductor. The top-level band E_C is the conduction band energy level, the Fermi level band is between the center line and the conduction band, and the lowest band E_V is the valence band energy level. The substitutional nickel atoms introduce an acceptor level of $E_c - 0.46$ eV in n-type single crystal silicon[12], which is marked as E_{Ni} in Fig. 1. E_{Au} is the gold acceptor level in silicon 0.54 eV from the conduction band level, and E_d is the shallow impurity energy level introduced by phosphorus atoms.

For limited sources of impurities on the thin surface layer, the formula of silicon surface concentration is[13]

$$N = \frac{Q}{\sqrt{\pi D t}} e^{-x^2/4Dt}. \qquad (1)$$

Here Q is the amount of total amount of impurities, t is the time for constant temperature diffusion, D is the diffusion coefficient of impurities in silicon, N is the concentration of impurities, and N_B is the substrate concentration. The spread

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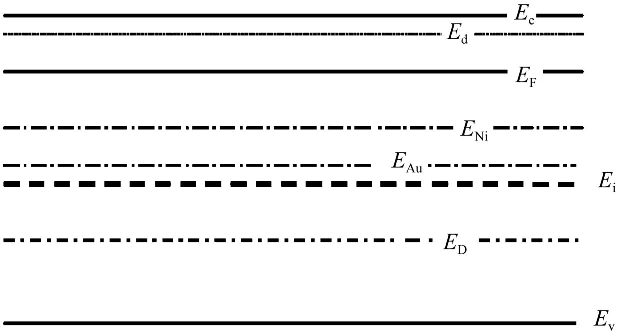

Fig. 1. Energy band configuration for nickel and gold doped silicon.

of the limited impurities source is a Gaussian distribution function. As the substrate is a single crystal and other factors related to n-type silicon conduction band are ignored, the carrier concentration gives[14]

$$n = \frac{N_d - N_A}{N - (N_d - N_A)} g_{Ni} N_c e^{-(E_c - E)/kT}. \qquad (2)$$

N_c is the effective density of states in the conduction band, N_d is the electron concentration introduced by nickel impurity, N_A is the hole concentration introduced by gold atoms, and E is the actual Fermi energy level. We get the conductivity formula:

$$\sigma = e\mu g_{Ni} N_c \frac{N_d - N_A}{N - (N_d - N_A)} e^{-(E_c - E)}. \qquad (3)$$

The main scattering mechanism of doped silicon semiconductors at room temperature is acoustic wave scattering and scattering of ionization. The temperature characteristics of the mobility is

$$\mu = \frac{e}{m^*} \frac{1}{AT^{3/2} + BN_i/T^{3/2}}. \qquad (4)$$

m^* is an effective quality, N_i is the ionization concentration of impurities, β is the ionization rate, e is the electronic charge, and μ is the mobility. We can now write the formula of electrical resistivity as

$$\rho = \frac{m^*}{e^2 g_{Ni}} \frac{N - (N_d - N_A)}{N_d - N_A} (AT^{3/2} + BN_i/T^{3/2}) e^{(E_c - E)/kT}. \qquad (5)$$

The result is

$$\rho = \rho_0 e^{(\Delta E - mkT \ln T)/kT}, \qquad (6)$$

where

$$AT^{3/2} + BN_i/T^{3/2} = CT^{-m}, \; E_c - E = \Delta E,$$

$$\rho_0 = \frac{m^* C}{e^2 g_{Ni}} \frac{N - (N_d - N_A)}{N_d - N_A}.$$

This shows us that electrical resistivity of silicon doped by nickel and gold is exponentially attenuated as the temperature increases.

In n-type silicon the nickel band level from the conduction band is 0.46 eV, so $\Delta E = 0.46$ eV. As the Boltzmann constant is $k = 8.86 \times 10^{-5}$ eV/K and electron mobility is ignored, we calculate that the B-value of the material is about 5300 K in the range of test values.

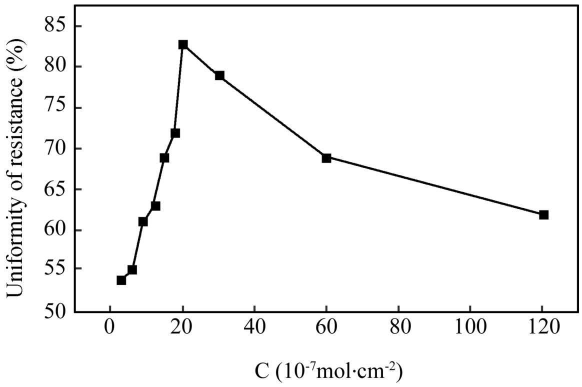

Fig. 2. Relationship between uniformity of resistance and silicon surface concentration of gold atoms.

3. Experimental procedures and results

3.1. Change law of electrical resistivity and *B*-value at different surface concentrations of gold atoms

The initial samples for this work were 1 Ω·cm, 320 μm thick n-type silicon wafers, which were diced into squares of 1 × 1 cm^2. The pieces were cleaned with organic solvents in an ultrasonic cleaner. This was done to remove any dirt and handling grease, in particular, the oxide layer. After the cleaning process, the wafers were smeared with nickel chloride ethanol solution and gold chloric acid ethanol solution, where the silicon surface concentration of nickel atoms was 1.05×10^{-5} mol/cm^2 and the silicon surface concentration of gold atoms was from 3×10^{-7} to 1.2×10^{-5} mol/cm^2. We dripped the source of diffusion onto the surface of the silicon and then evenly distributed it, subsequently using infrared light to dry the wafers. The wafers were put into a high-temperature furnace at 1000 °C for 2h, which allowed the proliferation of two kinds of impurities into the silicon, and then was cooled rapidly. The silicon wafers were nickel-plated, diced, electrode welded and packaged. The electrical resistance was measured at 25 and 50 °C by a two-probe technique with an Agilent34970 digital multimeter.

While the silicon surface concentration of nickel atoms remained invariant and the silicon surface concentration of gold atoms increased from 3×10^{-7} to 1.2×10^{-5} mol/cm^2, the electrical resistivity and B-value kept increasing.

Figure 2 shows the change law between the uniformity of thermistor resistance and silicon surface concentration of gold atoms. As the gold concentration increases, the uniformity gets better. When the silicon surface concentration of gold atoms is 2×10^{-6} mol/cm^2, we get the best-uniformity material. Subsequently, uniformity worsens with increasing silicon surface concentration of gold atoms. The best uniformity is 83%. Nickel and gold form complementary mechanisms to each other: gold atoms in silicon material occupy the vacancies, displacing nickel atoms at the same time, and nickel atoms are distributed in the interstices of the silicon material, so the uniformity of the silicon material is improved.

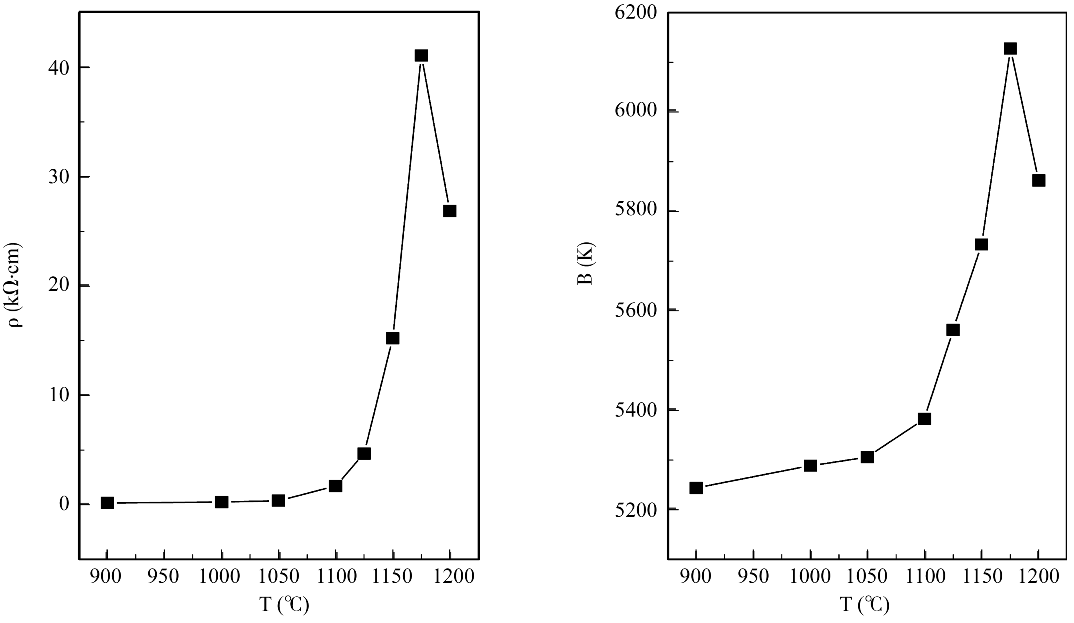

Fig. 3. Curves of electrical resistivity and *B*-value at different diffusion temperatures.

3.2. Change law of electrical resistivity and *B*-value at different diffusion temperatures

After the above work, when the silicon surface concentration of nickel atoms is 1.05×10^{-5} mol/cm^2 and the silicon surface concentration of gold atoms is 2×10^{-6} mol/cm^2, we can obtain the optimal conditions of surface concentration on silicon wafers. The work was done under these concentration conditions hereinafter.

When the diffusion temperature rises from 900 to 1175 °C, the electrical resistivity and *B*-value keep increasing, as shown in Fig. 3. The electrical resistivity rises from 0.16 to 41.07 kΩ·cm, and *B*-value is always from 5200 to 6100 K. When the diffusion temperature exceeds 1175 °C, the electrical resistivity and *B*-value become smaller. The deep level impurities, nickel and gold, trap the majority of carrier electrons. When most electrons are trapped, the majority of carriers become holes. Using a hot and cold probe method to test this material, we can see that n-type silicon changes to p-type silicon when the diffusion temperature is above 1175 °C. If the diffusion temperature is between 900 and 1000 °C, we can get a high *B*-value, low electrical resistivity and better uniformity single-crystal silicon material. The electrical resistivity is under 0.25 kΩ·cm and *B*-value is always above 5200 K.

3.3. Change law of electrical resistance and *B*-value with temperature

Figure 4 shows the change law of thermistor resistance with temperature. The thermistors are made by nickel and gold doped silicon material diffused at 1000 °C. The electrical resistance of thermistors is exponentially attenuated as the temperature increases. On increasing the temperature, the electrons that were bound by nickel and gold atoms are activated. When the carrier concentration is increased, the electrical resistance is reduced. As temperature increases from 40 to 60 °C, lattice scattering also increases, and almost all of the electrons bound by gold and nickel atoms are activated. Lattice scattering causes electron mobility to decrease, and the resistance will increase slightly. With a further rise in temperature, a large number of intrinsic carriers will be generated. The resistance of thermistors will be invariant over 80 °C. Equation (6) shows the electrical resistance and testing temperature change law. The exponential attenuation fit curve is in good agreement with experimental results.

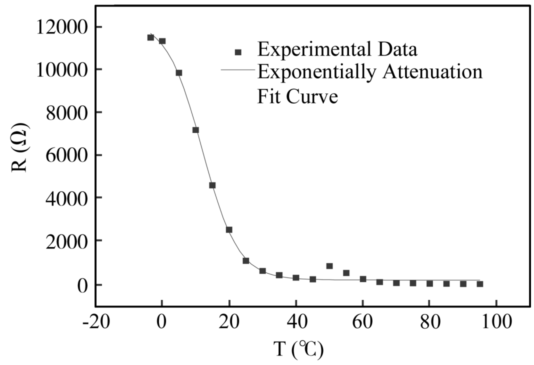

Fig. 4. *R*–*T* curves for nickel and gold doped silicon.

As the working temperature range expands, the *B*-value reduces little as the temperature rises because the activation energy became lower. We can see that the fit curve of the *B*-value is linear and attenuated with increasing temperature from Fig. 5.

4. Conclusion

In summary, the following conclusions can be drawn:

(1) Better-uniformity silicon material doped by pure gold and lower electrical resistivity silicon material doped by pure nickel were synthesized. When the silicon surface concentration of nickel atoms is 1.05×10^{-5} mol/cm^2, the silicon surface concentration of gold atoms is 2×10^{-6} mol/cm^2; when

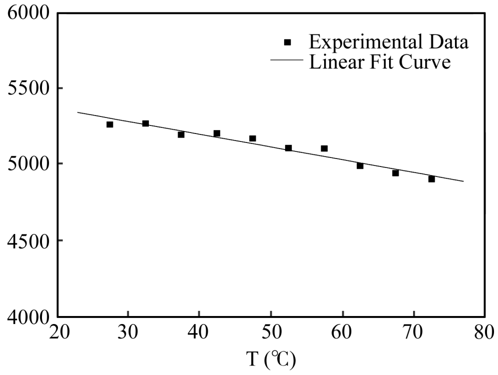

Fig. 5. *B*–*T* curves for nickel and gold doped silicon.

the diffusion temperature is between 900 and 1000 °C, we can get a high *B*-value, low electrical resistivity and better uniformity single-crystal silicon material.

(2) With diffusion temperature rising from 900 to 1200 °C, n-type silicon material turns into p-type, the electrical resistivity and *B*-value of the silicon material increase up to 1175 °C, and then the electrical resistivity and *B*-value decrease.

(3) Taking into account the primary role of ionization scattering and the formula of carrier concentration, we set up a physical model according to the theory of semiconductor deep level energy. On increasing the temperature, the electrical resistivity of compensation silicon is exponentially attenuated and the *B*-value decreases linearly. The physical model is basically consistent with the experimental results.

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