A 60-dB linear VGA with novel exponential gain approximation

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Abstract: A CMOS variable gain amplifier (VGA) that adopts a novel exponential gain approximation is presented. No additional exponential gain control circuit is required in the proposed VGA used in a direct conversion receiver. A wide gain control voltage from 0.4 to 1.8 V and a high linearity performance are achieved. The three-stage VGA with automatic gain control (AGC) and DC offset cancellation (DCOC) is fabricated in a 0.18-μm CMOS technology and shows a linear gain range of more than 58-dB with a linearity error less than ±1 dB. The 3-dB bandwidth is over 8 MHz at all gain settings. The measured input-referred third intercept point (IIP3) of the proposed VGA varies from –18.1 to 13.5 dBm, and the measured noise figure varies from 27 to 65 dB at a frequency of 1 MHz. The dynamic range of the closed-loop AGC exceeds 56 dB, where the output signal-to-noise-and-distortion ratio (SNDR) reaches 20 dB. The whole circuit, occupying 0.3 mm^2 of chip area, dissipates less than 3.7 mA from a 1.8-V supply.

Key words: variable gain amplifier; dB-linear; auto gain control; direct conversion receiver
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1. Introduction

In a wireless receiver, variable gain amplifiers (VGA) are usually employed in an automatic gain control (AGC) loop, to provide an optimum input power to the baseband analog-to-digital converters (ADC) for an unpredictable received signal strength from the antenna, so as to maximize the signal-to-noise ratio (SNR) performance.

While discrete-gain VGAs controlled by digital signals have a disadvantage in complicated additive digital gain control circuits to achieve an AGC function, continuous-gain VGAs controlled by analog signals are preferred for their simplified gain control circuits. In most AGC loops, an exponential gain control characteristic of the VGA is required to maintain the settling time of the AGC independent of the input signal level[1]. For this reason, an exponential function in a CMOS implementation is approximated by CMOS transistors in the saturation region with a square-law characteristic[2–4]. In this way, an exponential gain control circuit has to be implemented, which shows sensitivity to process and temperature variations, making this method less robust. Moreover, since an AGC is the last stage of an RFID receiver front-end, as shown in Fig. 1[5], the linearity performance of a VGA is critical for the whole system. However, a conventional Gilbert-cell VGA with a gain tuned by steering tail currents has a low linearity.

This paper proposes a novel method to control the gain of a Gilbert-cell VGA, by changing the source degeneration resistance instead of the biasing currents. Such a method has two advantages. First, the reduction in circuit complexity not only saves die area but also makes the VGA less sensitive to process and temperature variations. Second, the proposed VGA has a better linearity performance compared with conventional VGAs, which leads to a larger dynamic range of the AGC as well as for the receiver.

This paper also presents a three-stage VGA that adopts a novel approximated exponential equation. An AGC circuit is implemented as well. Furthermore, to prevent the DC offset, which is introduced by the local oscillator (LO) leakage and the component mismatch, to get amplified to such a large value that saturates the successive circuits, a suitable DC offset cancellation (DCOC) circuit is added to attenuate the DC gain.

2. VGA circuit

2.1. Conventional Gilbert-cell VGA

It is common that a Gilbert cell is used as a single-stage VGA, with a source degeneration resistor connected between the source nodes of the two transistors in the input differential pairs to improve the linearity performance, as shown in Fig. 2(a)[4]. The common mode feedback (CMFB) circuit is not depicted. In this VGA, the gain is tuned by steering the tail currents of the two input differential pairs. In principle, the VGA gain can be given as

$$A_{\rm v} \propto \left(\sqrt{I_{\rm bias1}} - \sqrt{I_{\rm bias2}}\right). \quad (1)$$

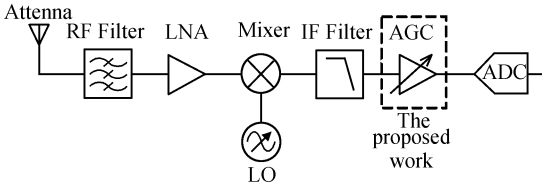

Fig. 1. Block diagram for a direct conversion RFID reader receiver.

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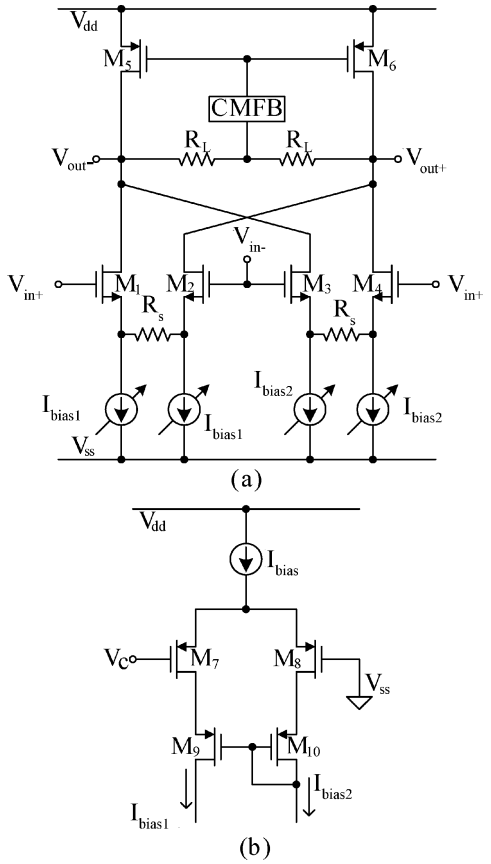

Fig. 2. Conventional VGA based on a Gilbert cell: (a) Gilbert cell; (b) Gain control circuit to generate proper bias currents for exponential gain control.

When I_{bias1} and I_{bias2} have very different amplitudes, a high gain is obtained. When I_{bias1} and I_{bias2} are almost equal to each other, a large attenuation is obtained. Therefore, a Gilbert cell can provide a large gain variation range. In addition, a voltage-to-current (V-to-I) converter is needed to translate the change of the control voltage into a suitable variation in the tail currents, in order to have an exponential dependency of the gain of the Gilbert cell on the control voltage, as shown in Fig. 2(b).

Assuming that $g_{m7,8}$ is the transconductance of the transistors M7 and M8 in the gain control circuits, and V_c is the input control voltage, the gain of the VGA can be expressed as

$$A_v \propto \left(\sqrt{I_{bias1}} - \sqrt{I_{bias2}}\right) \propto \left(\sqrt{\frac{1}{2}I_{bias} + \frac{1}{2}g_{m7,8}V_c} - \sqrt{\frac{1}{2}I_{bias} - \frac{1}{2}g_{m7,8}V_c}\right) \propto \left(\sqrt{1 + \frac{g_{m7,8}V_c}{I_{bias}}} - \sqrt{1 - \frac{g_{m7,8}V_c}{I_{bias}}}\right). \quad (2)$$

In this way the exponential gain control characteristic is approximated in a short range of x by the function as

$$f(x) = \sqrt{1+x} - \sqrt{1-x}. \quad (3)$$

2.2. The proposed VGA

In this paper, the gain of the Gilbert-cell VGA is tuned by changing the source degeneration resistance, which is implemented by a CMOS transistor working in the triode region, as shown in Fig. 3. Unlike conventional Gilbert-cell VGA steering tail currents, when the gain of the proposed VGA is tuned, the tail currents of the two input differential pairs remain constant and equal.

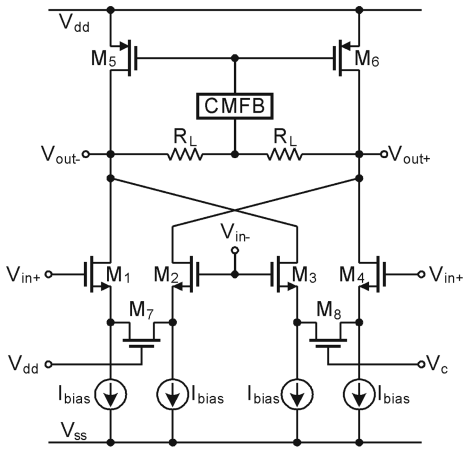

Fig. 3. Gilbert-cell VGA with gain tuned by changing the source degeneration resistor.

With second-order effects neglected, the transconductance of a differential pair (M1–M4) with a source degeneration resistor R_s is given by

$$G_m = \frac{1}{\frac{R_s}{2} + \frac{1}{g_m}}, \quad (4)$$

where g_m is the transconductance of the transistors in the differential pair, and R_s is the value of the source degeneration resistor.

In the proposed VGA, a CMOS transistor (M7 or M8) working in the triode region is implemented as the source degeneration resistor, as shown in Fig. 3. The resistance value is

$$R_s = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})} = \frac{1}{\beta_n(V_{GS} - V_{TH})}. \quad (5)$$

The transconductance of the proposed VGA is the difference between the transconductance of two individual input pairs with different source degeneration resistances, as given by

$$G_m = \frac{1}{\frac{R_{s,M7}}{2} + \frac{1}{g_{m1,2}}} - \frac{1}{\frac{R_{s,M8}}{2} + \frac{1}{g_{m3,4}}}. \quad (6)$$

In the proposed VGA, the gate voltage of M7 is the supply voltage V_{dd} and the gate voltage of M8 is the control voltage V_c. As the two input pairs have the same component size and biasing current, the transconductance of the transistors in the two pairs, i.e., $g_{m1,2}$ and $g_{m3,4}$ are equal. According to Eqs. (3) and (4), it can be concluded that

$$G_m = \frac{1}{\frac{1}{2\beta_{n7}(V_{dd} - V_{source1,2} - V_{TH})} + \frac{1}{g_{m1,2}}}$$

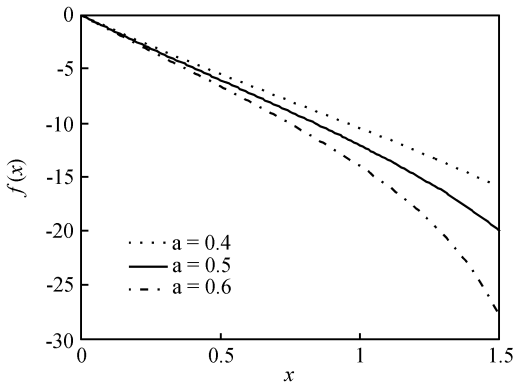

Fig. 4. Decibel scale plots of $f(x)$ for various values of the constant a.

$$\times \quad \frac{1-\dfrac{\beta_{n8}(V_c - V_{source3,4} - V_{TH})}{\beta_{n7}(V_{dd} - V_{source1,2} - V_{TH})}}{1+\dfrac{2\beta_{n8}(V_c - V_{source3,4} - V_{TH})}{g_{m3,4}}}. \tag{7}$$

By assuming

$$A = \frac{1}{\dfrac{1}{2\beta_{n7}(V_{dd} - V_{source1,2} - V_{TH})} + \dfrac{1}{g_{m1,2}}}, \tag{8}$$

$$x = \frac{2\beta - n8(V_c - V_{source3,4} - V_{TH})}{g_{m3,4}}, \tag{9}$$

$$a = \frac{g_{m3,4}}{2\beta_{n7}(V_{dd} - V_{souce1,2} - V_{TH})}, \tag{10}$$

the transconductance of the proposed VGA can be simplified as

$$G_m = A\frac{1-ax}{1+x}. \tag{11}$$

The transconductance is proportional to the new approximated exponential function proposed in this paper, which is given by

$$f(x) = \frac{1-ax}{1+x}. \tag{12}$$

As shown in Fig. 4, the new approximated function $f(x)$ depends exponentially on the variable x in a linear range less than 20-dB wide, when the constant a is 0.4, 0.5, and 0.6. Since the VGA gain is proportional to its transconductance, and the control voltage V_c has a linear relation to the variable x, as shown in Eq. (10), the exponential relation between the control voltage V_c and the gain of the proposed VGA is verified. The sizes of transistors M7 and M8 are chosen to set the constant a at about 0.5. The constant a depends weakly on the process parameters , such as V_{TH}, and may change within a ±5% range as a result of temperature and process variations. However, the exponential function still works for variation of a, which are not larger than 20%.

The 20-dB linear gain range is specified by the size matching of two source degeneration transistors (M7 and M8). At the minimum gain of the VGA, the variable x is set to zero and the function $f(x)$ equals 1. At the maximum gain, with the control voltage as high as the supply voltage V_{dd}, $f(x)$ can be

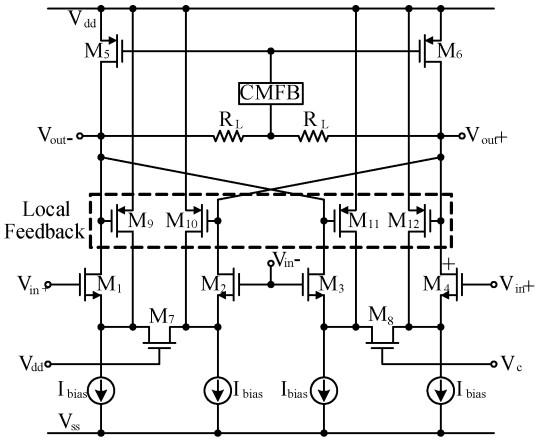

Fig. 5. The proposed VGA cell with local feedback to improve the linearity performance.

simplified to be

$$f(x) = \frac{1-ax}{1+x} = \frac{1-\dfrac{\beta_{n8}}{\beta_{n7}}}{1+\dfrac{1}{a}\dfrac{\beta_{n8}}{\beta_{n7}}}. \tag{13}$$

In the proposed VGA, the ratio of the sizes and β of two source degeneration transistors (M7 and M8) is designed to be 7 : 6. According to Eq. (13), $f(x)$ is 0.1 at the highest control voltage, which makes the minimum gain 20 dB lower than the maximum gain when the control voltage varies from ground to the supply voltage. Even if the constant a varies by ±5% from 0.5 at different temperatures and process conditions, the variation of the gain range is no larger than ±0.2 dB, since the gain range shown in Eq. (13) is weakly related to the constant a.

With a local feedback (M9–M12) to provide a further improvement to the linearity performance, the topology of the proposed VGA cell is depicted in Fig. 5. The exponential function of the VGA does not change with the added feedback loop, as the transconductance and the gain are degenerated by the loop gain, which is not related to the control voltage and can be approximately given as

$$\text{LoopGain} = g_{m9,10} \times r_{on5}, \tag{14}$$

where $g_{m9,10}$ is the transconductance of the local feedback transistors, and r_{on5} is the output resistance of the current sources (M5 or M6).

Compared with conventional Gilbert-cell VGA steering bias currents, the proposed VGA has two obvious advantages. First, an intrinsic exponential gain characteristic is provided, and no additional exponential gain control circuit is required. The circuit is simplified and the area is reduced, and the process and the temperature sensitivity introduced by the gain control circuit are eliminated. As shown by Eq. (13), the gain control range of the proposed VGA depends very weakly on the threshold voltage or other process parameters; so, the VGA is less sensitive to process and temperature variations. With this gain control method, a wide control voltage range from

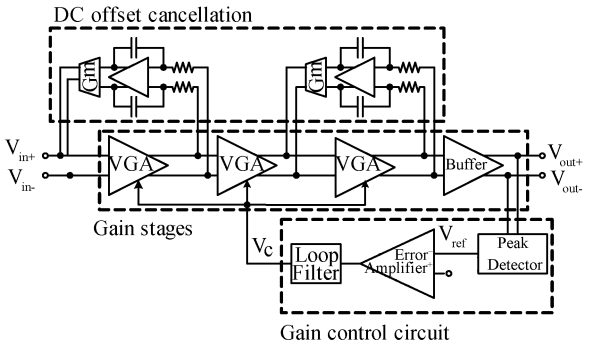

Fig. 6. Block diagram of the proposed three-stage VGA with an AGC loop and DC offset cancellation.

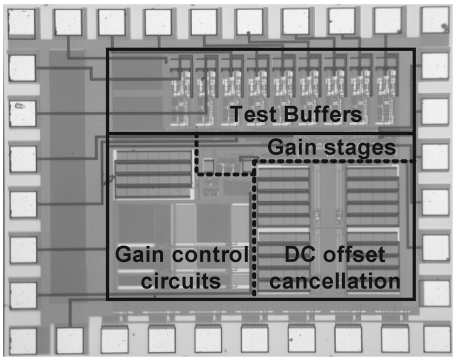

Fig. 7. Microphotograph of a test chip.

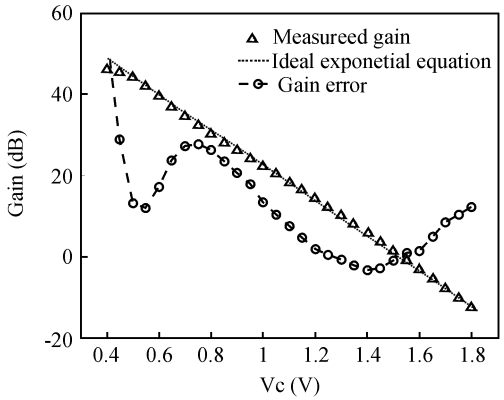

Fig. 8. Measured gain of the proposed VGA versus V_c.

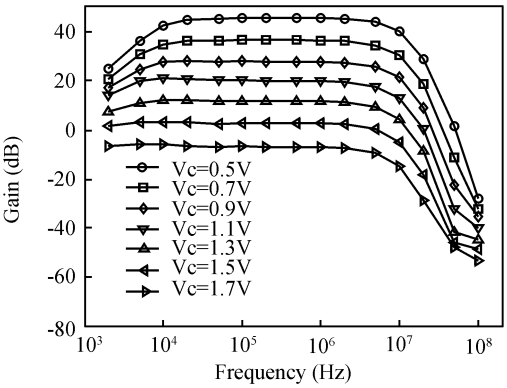

Fig. 9. Measured frequency responses of the proposed VGA at various gain settings.

0.4 to 1.8 V is achieved. This leads to a higher stability of the gain control loop. In addition, less noise and distortion is introduced by the gain control circuits.

Second, the IIP3 of the proposed VGA cell is 7 dB higher than that of a current-steering one with equal power consumption and noise performance, according to the simulation results. The main cause of the improvement is that the two differential pairs have the same size and bias currents, though with different source degeneration resistances. Consequently, distortions introduced by the two respective input pairs cancel each other to a large extend, since they have approximately the same phase. The higher linearity leads to a larger dynamic range of the AGC part and the whole receiver.

2.3. AGC loop

The proposed AGC loop employs a three-stage VGA as gain stages, cascaded with a 12-dB gain output buffer, together with gain control circuits including a peak detector, an error amplifier and a loop filter, as shown in Fig. 6[6]. With the tradeoff between the settling time and the stability of the gain control loop fully considered, a loop filter with a digital-controlled programmable bandwidth is implemented to optimize the AGC performance working at various data rates and signal bandwidths.

2.4. DC offset cancellation

As shown in Fig. 6, the DC offset cancellation blocks are built by adding a low pass filter (LPF) and a transconductance (G_m) stage around the VGA cell to provide a feedback at very low frequencies[7]. In this way, a high pass characteristic is obtained. In order to prevent the signal from being attenuated by the DC offset cancellation blocks, a very low bandwidth is required in the LPF. A Miller capacitance is utilized to implement the DC offset cancellation blocks in a single chip with a metal–insulator–metal (MIM) capacitor.

3. Measurement results

The three-stage VGA with AGC and DC offset cancellation, shown in Fig. 6, was implemented in a 0.18-μm CMOS technology and the micrograph of the test chip is shown in Fig. 7. The proposed VGA has an active area of 0.3 mm^2, excluding the bonding pads and the test buffers. The area of the gain stages is less than 0.05 mm^2. The total current consumption is less than 3.7 mA.

Figure 8 shows the measured gain versus the control voltage V_c of the proposed VGA. The gain varies from about –13 to 45 dB with a linearity error less than ±1 dB, when V_c varies from 0.45 to 1.8 V. Figure 9 shows the measured frequency responses of the proposed VGA at different gain settings. Although long channel transistors are utilized to reduce the flick noise, the 3-dB bandwidth of the VGA is over 8 MHz at all gain settings. Figure 10 shows the measured input-referred third intercept point (IIP3) and the noise figure of the proposed VGA at various gain levels. The IIP3 is 13.5 dBm at the minimum gain, and –18.1 dBm at the maximum gain. The measured noise figure varies from 27 to 65 dB at 1 MHz and

Table 1. Performance of the proposed and previously reported VGAs.

Parameter	This work	Ref. [2]	Ref. [3]
Technology	0.18 μm CMOS	0.18 μm CMOS	0.25 μm CMOS
Max. P_{1dB} (dBm)	1	−17	−8
Max. IIP3 (dBm)	13.5	N/A	7
3-dB BW (MHz)	8	32	30
Power consumption (mW)	6.7 at 1.8 V	6.5 at 1.8 V	27.5 at 2.5 V
Gain variation (dB)	60	95	80
Active area (mm)^2	0.3 (core size 0.06)	0.4	0.49

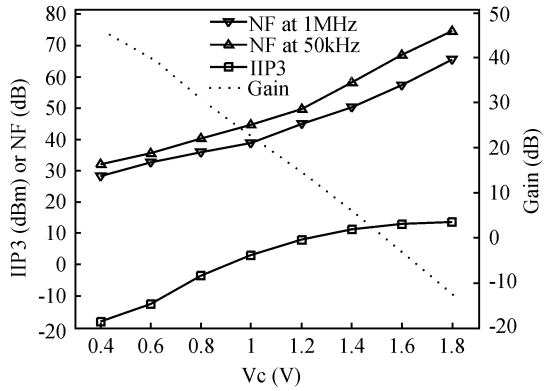

Fig. 10. Measured IIP3 and the noise figure of the proposed VGA at various gain levels.

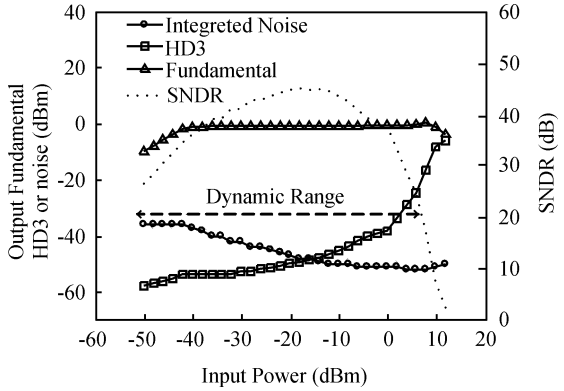

Fig. 11. Measured output power of the fundamental and the third order harmonics, the integrated noise and the calculated SNDR of the AGC.

from 31 to 71 dB at 50 kHz.

Figure 11 shows the output power of the fundamental, the third order harmonics and the in-band integrated noise with different input powers, after the gain of the VGA is properly set by the AGC loop in less than 20 μs. Using the noise and the distortion measurement results, the signal-to-noise-and-distortion ratio (SNDR) of the output of the AGC are calculated and shown as a dotted line in Fig. 11. It is demonstrated that the effective dynamic range of this AGC is more than 56 dB when the 20-dB SNR requirement of an RFID reader is satisfied.

As shown in Table 1, the proposed VGA with the novel exponential gain approximation has an improved linearity performance of the IIP3 and the 1-dB compression point (P_{1dB}) compared to previously published works.

4. Conclusion

An all-CMOS VGA cell with a novel approximated exponential equation is presented in this paper. The circuit performance can be characterized by that fact that no addition gain control circuit is needed and by the high linearity performance. The proposed three-stage VGA with an AGC loop and a DCOC is implemented in a 0.18-μm CMOS technology with a 1.8 V supply voltage. With a power dissipation of less than 3.7 mA, the effective dynamic range of the proposed AGC is larger than 56 dB when the 20-dB SNR requirement of a RFID reader is satisfied.

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