A novel noise optimization technique for inductively degenerated CMOS LNA*

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Abstract: This paper proposes a novel noise optimization technique. The technique gives analytical formulae for the noise performance of inductively degenerated CMOS low noise amplifier (LNA) circuits with an ideal gate inductor for a fixed bias voltage and nonideal gate inductor for a fixed power dissipation, respectively, by mathematical analysis and reasonable approximation methods. LNA circuits with required noise figure can be designed effectively and rapidly just by using hand calculations of the proposed formulae. We design a 1.8 GHz LNA in a TSMC 0.25 μm CMOS process. The measured results show a noise figure of 1.6 dB with a forward gain of 14.4 dB at a power consumption of 5 mW, demonstrating that the designed LNA circuits can achieve low noise figure levels at low power dissipation.

Key words: low noise; optimization; noise factor
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1. Introduction

The advances in modern CMOS technologies make the full integration of communication systems in low cost CMOS processes realizable. In a typical receiver chain, a low noise amplifier (LNA) is the first active stage that achieves input impedance matching and reduces the noise factor of the whole system. The inductively degenerated CMOS LNA was proposed and widely used in narrowband receiver applications due to its potential low noise performance[1−3]. But, due to the complexity of noise analysis in the deep submicron CMOS process, the optimization of the LNA noise is still an important issue in LNA circuit design. This paper proposes a novel noise optimization technique for inductively degenerated CMOS LNA noise design.

A number of LNA noise design techniques have been reported to optimize the noise performance of the inductively degenerated LNA[4−7]. Some noise optimization methods have been presented to give noise parameter expressions and to minimize noise factor under the assumption of a lossless gate inductor[4, 5]. However, these methods can not derive the deviation degree expression from the MOS transistor minimum noise factor and are not suitable for LNA circuits with a low quality factor of the on chip inductor and high operation frequency. Therefore their applications in practice are limited. Recently, other noise optimization methods have been proposed in which the losses of matching inductors are taken into account[6, 7]. But due to the complexity of the mathematical formula of the whole noise factor, the formula can not be used effectively to guide the design of LNA. The designer still has to use computer simulation and iteration methods to optimize the noise factor of the LNA step by step, so that the design cost increases.

This paper presents a novel noise optimization technique that is suitable for two kinds of LNA circuits with an ideal gate inductor for a fixed bias voltage and a nonideal gate inductor for a fixed power dissipation. For LNA with an ideal gate inductor, this paper gives an explicit and intuitive explanation of why the LNA of this structure can achieve an approximately minimum noise factor at any level of power dissipation by using concise mathematical analysis. In addition, the deviation degree of the LNA noise factor from the MOS transistor minimum noise factor is given by this paper for the first time. On the other hand, this paper gives the optimal input quality factor expression for the LNA with a nonideal gate inductor for a fixed power dissipation for the first time by using reasonable approximation methods. The expression is useful in practical LNA design. The proposed technique can help the designers to obtain the main design parameters just by using the proposed formulae and the process model parameters. With the main parameters of LNA, the designed LNA can achieve the required noise performance. Therefore the technique can decrease the simulation time, design cycle and design cost considerably.

2. Low noise optimization technique

2.1. Noise analysis of LNA with an ideal gate inductor for a fixed bias voltage

Figure 1(a) shows a typical inductively degenerated CMOS LNA topology. It consists of an input signal source RF_{in} with a source resistance R_s of 50 Ω, gate inductor L_g, source inductor L_S, load inductor L_d, additional capacitor C_{ext}, supply voltage V_{dd}, transistors M1 and M2. L_g and L_S are used

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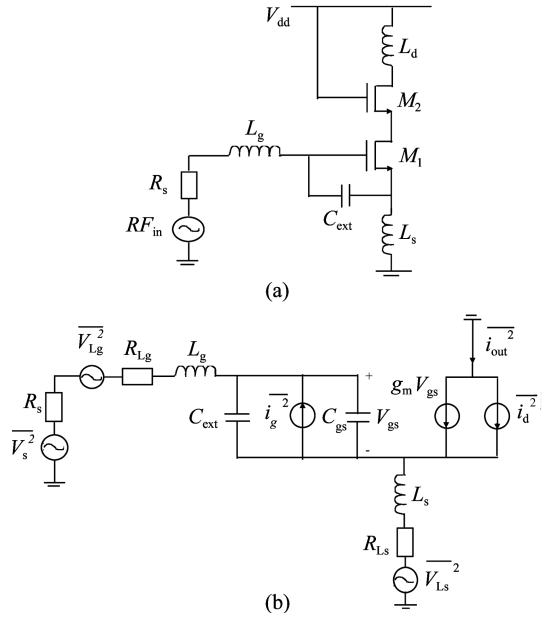

Fig. 1. (a) Schematic of inductively degenerated CMOS LNA; (b) Its small signal equivalent circuit used for calculating the noise factor.

to match input impedance. L_d is used to match output impedance. Figure 1(b) is the simplified small signal equivalent model of the circuit. Since the common gate transistor M2 and the load contribute little noise to the whole circuit, their noise is ignored.

$\overline{i_d^2}$ and $\overline{i_g^2}$ represent the mean squared channel thermal noise current and the mean squared gate induced noise current respectively, and are given by[8]

$$\overline{i_d^2} = 4kT\gamma g_{d0}\Delta f, \quad \overline{i_g^2} = 4kT\delta g_g \Delta f, \tag{1}$$

where $g_g = (\omega^2 C_{gs}^2)/5g_{d0}$, ω is the operation angular frequency, C_{gs} is inherent gate-source capacitance of the transistor, g_{d0} is the zero bias drain conductance, k is the Boltzmann constant, T is the absolute temperature, γ and δ are the coefficient of channel thermal noise and the gate induced noise respectively, and Δf is the bandwidth. The value of C_{gs} is $2WLC_{ox}/3$, where W and L are the channel width and channel length of the transistor respectively, and C_{ox} is the gate oxide capacitance per unit area. In the following analysis, the transistor channel length L is considered equal to the technology feature size, thus is a constant in the LNA design procedure.

The parameters γ and δ have a value of 2/3 and 4/3 for long channel MOS in saturation mode operation, respectively. However their value can be more than two and four for short channel, respectively. The correlation coefficient between the channel thermal noise current and the gate induced noise current is defined as follows[8]

$$c \equiv \overline{i_g i_d^*} \Big/ \sqrt{\overline{i_g^2}}\sqrt{\overline{i_d^2}}. \tag{2}$$

For long channel MOS, the value of c can be predicted theoretically as –0.395j for the polarity shown in Fig. 1(b). Its value in short channel MOS is between –0.3j and –0.35j [9], but its exact value is still under research. In this paper, we use the value –0.35j for c for simplicity.

$\overline{V_S^2}$, $\overline{V_{Lg}^2}$, $\overline{V_{Ls}^2}$ are the thermal noises of source resistance, the thermal noise of parasitic resistance of gate inductor L_g, and the thermal noise of parasitic resistance of source inductor L_S, respectively. The power spectral densities of these three noise sources are given by

$$\overline{V_S^2} = 4kTR_S, \quad \overline{V_{Lg}^2} = 4kTR_{Lg}, \quad \overline{V_{Ls}^2} = 4kTR_{Ls}, \tag{3}$$

where $R_{Lg}$and R_{Ls} are the parasitic resistances of L_g and L_S respectively.

$\overline{i_{out}^2}$ is the mean squared total output noise current, and g_m is the transconductance of the transistor.

Using the small signal equivalent circuit model as shown in Fig. 1(b), the noise factor F under conditions of power matching can be derived as follows[7]

$$F = \frac{R}{R_S}\left(1 + R\frac{\gamma\omega_0^2 C_t^2}{\alpha^2 g_{d0}}\chi\right), \tag{4}$$

where

$$\chi = \frac{\alpha^2\delta}{5\gamma}(1+Q_S^2)\frac{C_{gs}^2}{C_t^2} + 1 - 2|c|\frac{C_{gs}}{C_t}\sqrt{\frac{\alpha^2\delta}{5\gamma}},$$

$$C_t = C_{gs} + C_{ext},\ R = R_S + R_{Lg} + R_{Ls},\ \alpha = g_m/g_{d0},$$

$$Q_S = 1/(\omega_0 C_t R).$$

If we consider that L_g and L_S are ideal inductors and ignore their loss, then $R_{Lg} = R_{Ls} = 0$, so F can be expressed as

$$F = 1 + \eta, \tag{5}$$

where

$$\eta = R_S\frac{\gamma\omega_0^2 C_t^2}{\alpha^2 g_{d0}}\chi. \tag{6}$$

In order to give a simple yet insightful perspective, Equation (5) can be expressed in another form as follows:

$$F = 1 + A_1\frac{P}{Q_S} + A_2\frac{1}{P}\left[\frac{1}{Q_S} + Q_S\right] - A_3\frac{1}{Q_S}, \tag{7}$$

where

$$P = \frac{C_t}{C_{gs}},\ A_1 = \frac{\gamma}{\alpha}\frac{\omega_0}{\omega_T},$$

$$A_2 = \frac{1}{5}\delta\alpha\frac{\omega_0}{\omega_T}, \quad A_3 = 2|c|\sqrt{\frac{\delta\gamma}{5}}\frac{\omega_0}{\omega_T}.$$

ω_T is the MOS transistor's cut off frequency. Note that A_1, A_2 and A_3 are bias voltage and process dependent parameters, so for a fixed bias voltage, the noise factor of LNA is a function of P and Q_S. By solving the minimum value of Eq. (7) with respect to P, the optimum value of P is given by

$$P_{opt} = \sqrt{\frac{\delta\alpha^2}{5\gamma}(1+Q_S^2)}. \tag{8}$$

In the practical case, P is always larger than one because of the non-negligible inherent overlap capacitance between gate and source. Therefore Equation (8) is valid when

$$Q_S > \sqrt{\frac{5\gamma}{\delta\alpha^2} - 1}. \tag{9}$$

For typical values of advanced modern CMOS technology parameters as discussed previously, the value of δ/γ is approximately 2, and the range of α is between 0.8 to 0.9 in general[10], so the right term of Eq. (9) is near to 1. In typical modern CMOS LNA design, the Q_S should be larger than 1 so that the power consumption of LNA circuit is low. Therefore Inequation (9) is valid in general. During the following analysis Inequation (9) is assumed to be always satisfied. Thus for a given bias voltage and Q_S, the minimum value of F in Eq.(7) is expressed as follows by substituting Eq. (8) into Eq. (7).

$$F = 1 + \frac{2}{\sqrt{5}}\frac{\omega_0}{\omega_T}\sqrt{\gamma\delta}\varphi, \tag{10}$$

where

$$\varphi = \frac{\sqrt{1+Q_S^2}}{Q_S} - \frac{|c|}{Q_S}. \tag{11}$$

φ is the function of Q_S. By solving the minimum value of Eq. (11) with respect to Q_S, the optimum value of Q_S can be derived as follows:

$$Q_{S,opt} = \sqrt{1-|c|^2}\Big/|c|. \tag{12}$$

Note that the value of $Q_{S,opt}$ satisfies Ineq. (9) in general, so Equation (12) is valid. By substituting Eq. (12) into Eq. (11), the minimum value of φ can be expressed as

$$\varphi_{min} = \sqrt{1-|c|^2}. \tag{13}$$

Using $|c| = 0.35$, $\delta/\gamma = 2$ and $0.8 < \alpha < 0.9$, the upper limit value of φ in Eq. (11) is 1, so the range of φ is given by

$$\sqrt{1-|c|^2} \leqslant \varphi < 1. \tag{14}$$

Using Eq. (13), the minimum value of F in Eq. (10) is given by

$$F_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega_0}{\omega_T}\sqrt{\gamma\delta(1-|c|^2)}. \tag{15}$$

Note that Equation (15) is exactly the same as the minimum MOS transistor noise factor under noise matching conditions[7].

According to Eq. (14), the upper limit value of F in Eq. (10) is given by

$$F = 1 + \frac{2}{\sqrt{5}}\frac{\omega_0}{\omega_T}\sqrt{\gamma\delta}. \tag{16}$$

Therefore the noise factor F varies between Eqs. (15) and (16) for any value of Q_S as long as Equation (8) and Inequation (9) are satisfied simultaneously.

Considering that the values of Eqs. (15) and (16) are almost equal in modern technology parameters, the noise factor of LNA can be approximately equal to F_{min} of a single MOS transistor under noise matching conditions.

Under the condition of Eq. (8), for a fixed bias voltage and a given Q_S, the width and the value of parallel capacitor C_{ext} of the transistor M1 can be expressed as follows.

$$W = \frac{3}{2LC_{ox}\omega_0 R_S Q_S\sqrt{Q_S^2+1}}\sqrt{\frac{5\gamma}{\delta\alpha^2}}, \tag{17}$$

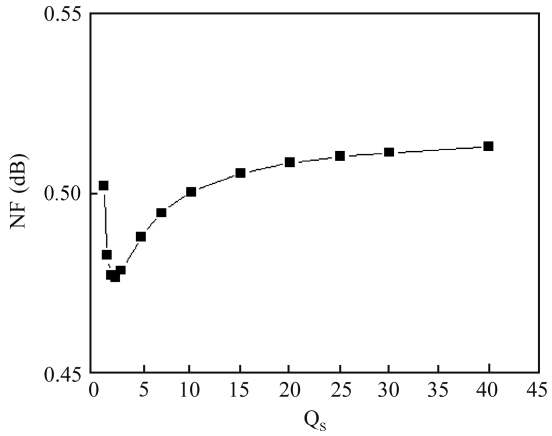

Fig. 2. Relationship between noise figure and Q_S. $\omega_T = 20\omega_0$, $\gamma = 2$, $\delta = 4$.

$$C_{ext} = \frac{1}{\omega_0 R_S Q_S}\left[1 - \frac{1}{\sqrt{Q_S^2+1}}\sqrt{\frac{5\gamma}{\delta\alpha^2}}\right]. \tag{18}$$

If we use Eqs. (17) and (18) to design LNA, the noise factor of LNA can achieve approximately F_{min} at any level of power dissipation for a fixed bias voltage. In addition, when the value of Q_S is equal to $Q_{S,opt}$, the noise factor of LNA can achieve precisely F_{min} at that point.

In order to get a intuitive explanation, the relationship between F and Q_S in Eq. (10) under a given bias voltage is plotted in the curve shown in Fig. 2, where the noise figure NF is defined as NF = 10lg$F$. The noise figure NF varies over a very small range when Q_S varies over a wide range. There is a minimum value of NF at a certain value of Q_S which in fact is the $Q_{S,opt}$ expressed in Eq. (12). At a given bias voltage, larger Q_S implies less power dissipation as seen from Eq. (17); however, the noise figure can still remain approximately at NF_{min}.

2.2. Noise analysis of LNA with a nonideal gate inductor for a fixed power dissipation

In practical applications, the inductor L_g and L_S are not ideal, so they contribute some noise to the whole output noise. In order to calculate their noise contribution, the values of their parasitic resistance should be considered.

The quality factors of L_g and L_S are given by

$$Q_{Lg} = \omega L_g/R_{Lg}, \quad Q_{Ls} = \omega L_S/R_{Ls}, \tag{19}$$

where Q_{Lg} and Q_{Ls} are the quality factors of L_g and L_S respectively. Under the constraint of impedance matching conditions given by

$$s(L_g + L_S) + \frac{1}{sC_t} = 0, \quad \frac{g_m}{C_t}L_S = R_S, \tag{20}$$

the values of L_g and L_S can be expressed as

$$L_g = R_S\left[\frac{Q_S}{\omega_0} - \frac{P}{\omega_T}\right], \quad L_S = R_S\frac{P}{\omega_T}. \tag{21}$$

Using Eqs. (19) and (21), the sum of R_{Lg} and R_{Ls} is given by

$$R_{Lg}+R_{Ls}=R_S\frac{Q_S}{Q_{Lg}}+R_S\left(\frac{\omega_0 P}{\omega_T Q_{Ls}}-\frac{\omega_0 P}{\omega_T Q_{Lg}}\right). \tag{22}$$

Since $R_S\dfrac{Q_S}{Q_{Lg}}\gg R_S\left(\dfrac{\omega_0 P}{\omega_T Q_{Ls}}-\dfrac{\omega_0 P}{\omega_T Q_{Lg}}\right)$ in general, so

$$R_{Lg}+R_{Ls}\approx R_S\frac{Q_S}{Q_{Lg}}. \tag{23}$$

Substituting Eq. (23) into Eq. (4), the noise factor is given by

$$F=1+\frac{Q_S}{Q_{Lg}}+\left(1+\frac{Q_S}{Q_{Lg}}\right)^2\eta. \tag{24}$$

The relationship between power dissipation P_D, P, Q_S and bias voltage is given by[11]

$$PQ_S=\frac{P_0}{P_D}\frac{\rho^2}{1+\rho}, \tag{25}$$

where $\rho=V_{od}/(LE_{sat})$, $P_0=3V_{dd}\nu_{sat}E_{sat}/(2\omega_0 R_S)$, V_{od} is the overdrive voltage, L is the effective channel length, ν_{sat} is the saturation velocity, and E_{sat} is the velocity saturation field strength.

Since $\rho\ll 1$ in general, Equation (25) can be expressed approximately as

$$PQ_S\approx(P_0/P_D)\rho^2. \tag{26}$$

Consider

$$\alpha=g_m/g_{d0}=(1+0.5\rho)\Big/(1+\rho)^2\approx 1. \tag{27}$$

Under the condition of $\rho\ll 1$, so ω_T can be given by

$$\omega_T=g_m\Big/C_{gs}=3\alpha\nu_{sat}\rho/L\approx 3\nu_{sat}\rho/L. \tag{28}$$

Using Eqs. (26)–(28), η can be expressed in another form given as follows:

$$\eta=B_1\frac{1}{Q_S\sqrt{Q_S}}\sqrt{P}+B_2\frac{1}{\sqrt{Q_S}}\left[\frac{1}{Q_S}+Q_S\right]\times\frac{1}{P\sqrt{P}}-B_3\frac{1}{\sqrt{P}}\frac{1}{Q_S\sqrt{Q_S}}, \tag{29}$$

where $B_1=\gamma\dfrac{\omega_0 L}{3\nu_{sat}}\sqrt{\dfrac{P_0}{P_D}}$, $B_2=\dfrac{1}{5}\delta\dfrac{\omega_0 L}{3\nu_{sat}}\sqrt{\dfrac{P_0}{P_D}}$,

$$B_3=2|c|\sqrt{\frac{\delta\gamma}{5}}\frac{\omega_0 L}{3\nu_{sat}}\sqrt{\frac{P_0}{P_D}}.$$

Since the values of γ and δ/γ show less variation with bias at moderate bias voltages when the transistor operates in saturation mode operation[11, 12], the values of B_1, B_2 and B_3 can be seen as constant under a fixed power dissipation P_D.

Substituting Eq. (29) into Eq. (24), by solving the minimum value of Eq. (24) with respect to P, the optimum value of P can be derived as follows:

$$P_{opt,\,fixpd}=-|c|\sqrt{\frac{\delta}{5\gamma}}+\sqrt{\frac{3\delta}{5\gamma}(1+Q_S^2)}\approx\sqrt{\frac{3\delta}{5\gamma}(1+Q_S^2)}. \tag{30}$$

Note that $P_{opt,fixpd}>1$ in modern technology parameters with $\delta/\gamma=2$, so Equation (30) is valid for any given value of Q_S.

Using Eqs. (29) and (30), the minimum noise factor F in Eq. (24) for a given Q_S under fixed power dissipation is given by

$$F=1+\frac{Q_S}{Q_{Lg}}+\lambda(1+\frac{Q_S}{Q_{Lg}})^2\frac{1}{(1+Q_S^2)^{0.25}Q_S^{0.5}}\xi, \tag{31}$$

where

$$\lambda=\frac{4}{\sqrt{15}}\omega_0\gamma\left(\frac{5\delta}{3\gamma}\right)^{0.25}\frac{L}{3\nu_{sat}}\sqrt{\frac{P_0}{P_D}}, \tag{32}$$

$$\xi=\frac{\sqrt{1+Q_S^2}}{Q_S}-\frac{\sqrt{3}|c|}{2Q_S}. \tag{33}$$

The parameter λ can be seen as a constant under fixed power dissipation P_D. Using the same method as discussed in section 2.1, the minimum value of ξ is given by

$$\xi_{min}=\sqrt{1-0.75|c|^2}, \tag{34}$$

the corresponding optimum Q_S about ξ is given by

$$Q_{S,opt\xi}=\frac{\sqrt{4-3|c|^2}}{3|c|}. \tag{35}$$

The value of $Q_{S,opt\xi}$ is near to a value of 1. In fixed power dissipation design using advanced technology parameters, when the value of Q_S is too small, the ratio of channel width to channel length is too large, which will result in the transistor operating in the subthreshold region. Therefore, in practical design under fixed power dissipation, the value of Q_S cannot be designed to be too small due to linearity degradation in the subthreshold region. Therefore, in the following analysis, we assume

$$Q_S\geqslant Q_{S,\,opt\xi}. \tag{36}$$

When $Q_S\geqslant Q_{S,\,opt\xi}$, the upper limit value of ξ is 1. So the range of ξ is given by

$$\sqrt{1-0.75|c|^2}\leqslant\xi<1. \tag{37}$$

The range of ξ is very small and ξ varies very little while Q_S varies over a wide range. Therefore ξ can be seen as a constant of 1 for simplicity.

When $Q_S\geqslant Q_{S,opt\xi}$,

$$(1+Q_S^2)^{0.25}\approx Q_S^{0.5}. \tag{38}$$

By substituting Eq. (38) and $\xi=1$ into Eq. (31), the F in Eq. (31) can be expressed approximately as follows:

$$F\approx 1+Q_S\left(\frac{1}{Q_{Lg}}+\frac{\lambda}{Q_{Lg}^2}\right)+\frac{\lambda}{Q_S}+\frac{2\lambda}{Q_{Lg}}. \tag{39}$$

By solving the minimum value of Eq. (39) with respect to Q_S, the optimum value of Q_S about F is given by

$$Q_{S,\,opt,\,fixpd}=Q_{Lg}\sqrt{\frac{\lambda}{\lambda+Q_{Lg}}}. \tag{40}$$

Equation (40) is valid when Equation (36) is satisfied. When an off-chip gate inductor is used in LNA circuit design, Equation (40) satisfies Ineq. (36) in general due to the large quality factor of the off-chip inductor. However, if an on-chip gate inductor is used whose quality factor is not large enough,

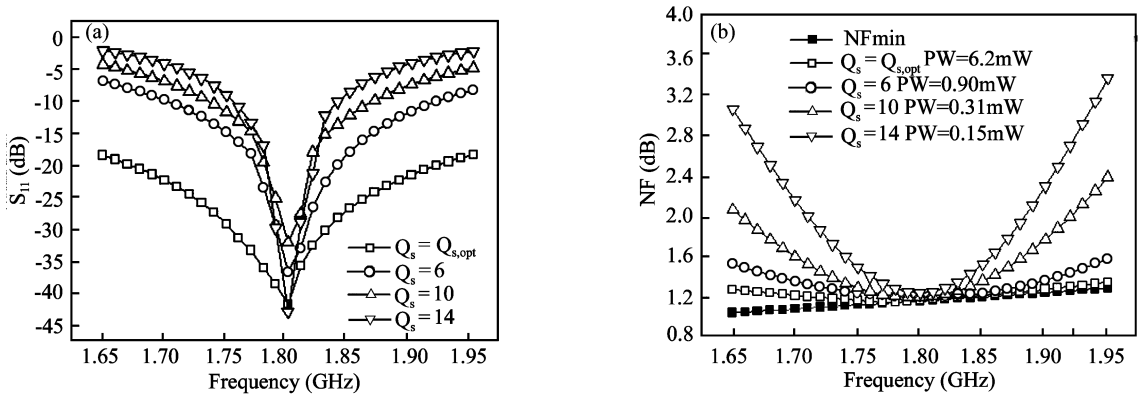

Fig. 3. (a) Simulated S_{11} versus frequency; (b) Simulated NF and NF_{min} for different Q_S. The bias voltage is 0.6 V. PW denotes power dissipation. Noise figure NF is defined as NF = 10lg$F$.

Equation (40) is not valid when the quality factor Q_{Lg} is lower than a certain value. If Equation (40) is not valid, then the value $Q_{S,opt\xi}$ is chosen as the optimum Q_S. In this case, the F in Eq. (39) can achieve its minimum value in the range of Ineq. (36).

With the optimum Q_S, the optimum P can be obtained according to Eq. (30), then the optimum value of the transistor's width and the capacitance of the parallel capacitor can be obtained which give the LNA the minimum noise factor for a fixed power dissipation.

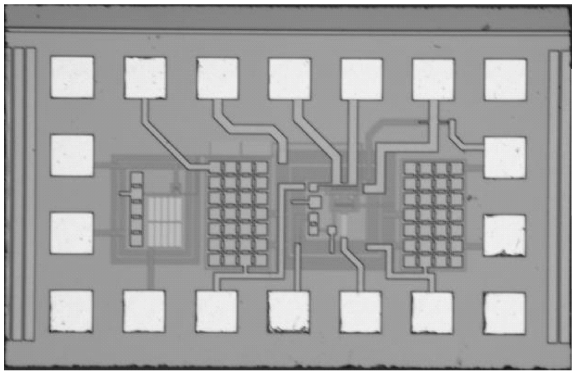

Fig. 4. Microphotograph of the LNA chip.

3. Simulated and measured results

In order to demonstrate that the proposed noise optimization technique is effective on inductively degenerated CMOS LNA, we design two LNA circuits. One is an LNA circuit with an ideal gate inductor at a fixed bias voltage, the other is an LNA circuit with a practical nonideal gate inductor at a fixed power dissipation. For the LNA with an ideal gate inductor, a center operation frequency of 1.8 GHz LNA is designed using the TSMC 0.25 μm CMOS process. First we calculated and obtained the main design parameters of LNA using the proposed concise formulae in Section 2.1. Then we simulated this kind of LNA circuit, and directly obtained the noise performance of the LNA circuit using an RF circuit simulator. The simulated results are shown in Fig. 3. The parameter S_{11} reflects the performance of input impedance matching of the LNA. In typical receiver design, in order to receive the energy of the input signal efficiently, the input impedance of the LNA should match the impedance of the antenna in the frequency band of interest. In general practical application, good impedance matching can be obtained when the $S_{11} < -10$ dB. As can be seen in Fig. 3, in addition to good impedance matching, the NF of the LNA with an ideal gate inductor under different power consumptions nearly coincides with NF_{min} at the frequencies of interest.

For the LNA with a practical nonideal gate inductor, a center operation frequency of 1.8 GHz LNA is designed and fabricated using the TSMC 0.25 μm CMOS process; a microphotograph of the LNA chip is shown in Fig. 4. In order to save layout area, we use single-ended circuit topology, the L_g and L_d are implemented using off-chip inductors, and L_S is the bondwire inductor. The simulation and measurement results are shown in Fig. 5. The parameter S_{21} in Fig. 5(a) is the S-parameter denoting the power gain of the circuit. According to the datasheet of the ceramic inductors (HI 1005 series), at a frequency of 1.8 GHz, the quality factor of the inductor is approximately between 20 and 30 when the inductor value is around over ten nanohenries. Considering the parasitic resistance in the input path, we use a quality factor of 20 for simulation. As can be seen in Fig. 5, the measured results are nearly consistent with the simulated results; a noise figure of 1.6 dB with a forward gain of 14.4 dB is achieved at a relatively low power consumption of 5 mW. In order to prove that the proposed optimization technique is consistent with the measured result, we calculate the noise figure according to Eq. (39) using a power consumption P_D = 5 mW, operation frequency of 1.8 GHz, a quality factor of the gate inductor Q_{Lg} = 20 and the process model parameters. The calculated noise figure is 1.5 dB, therefore denoting that the fabricated LNA circuit can achieve a low noise figure even at low power consumptions as expected theoretically. These measured results are consistent with those obtained by traditional computer simulation and step by step iteration methods. A comparison of this LNA with the published literature is summarized in Table 1. Our LNA provides the best noise performance at the lowest power level among the published literature listed in Table 1. Therefore, the above results demonstrate that the proposed novel noise optimization technique is effective and promising.

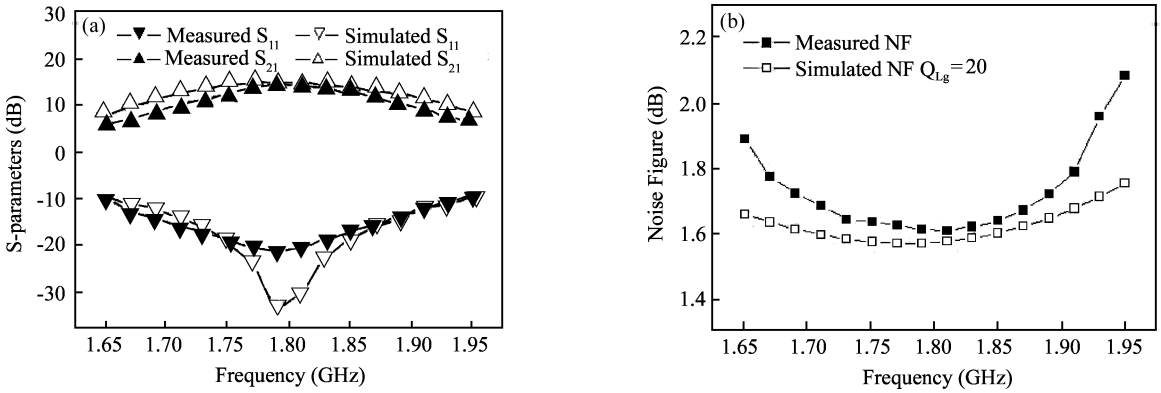

Fig. 5. (a) Simulated and measured S_{11} and S_{21} versus frequency; (b) Simulated and measured noise figure at fixed power dissipation of 5 mW.

Table 1. Performance comparison of LNA.

Parameter	Technology	Freq (GHz)	Gain (dB)	NF (dB)	Power (mW)
This work	0.25 μm CMOS	1.8	14.4	1.6	5
Ref. [13]	0.25 μm CMOS	1.9	16.6	2	11.5
Ref. [14]	0.5 μm CMOS	1.9	15	1.8	25
Ref. [15]	0.35 μm SOI CMOS	1.6	10.8	4.2	7.5
Ref. [16]	0.35 μm CMOS	2.2	8.6	1.9	8.1

4. Conclusion

A novel noise optimization technique was presented for inductively degenerated CMOS LNA circuits with an ideal gate inductor for a fixed bias voltage and a nonideal gate inductor for a fixed power dissipation. The proposed noise technique gave analytical formulae for the noise performance of the LNA circuits and design procedures by mathematical analysis and reasonable approximation methods. The designer can design CMOS LNA circuits with favorable noise factor just by hand calculations according to the proposed design formulae and the process model parameters. The design technique can reduce the simulation time, design cycle and design cost considerably. We designed an LNA circuit in the TSMC 0.25 μm CMOS process by the technique effectively and rapidly. The noise performance of the designed LNA circuit was measured by an RF noise figure analyzer. The test results demonstrated that the fabricated LNA circuit can achieve a low noise figure level and that the proposed novel noise optimization technique is effective and promising.

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