The Bipolar Field-Effect Transistor: XIII. Physical Realizations of the Transistor and Circuits (One-Two-MOS-Gates on Thin-Thick Pure-Impure Base)*

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Abstract: This paper reports the physical realization of the Bipolar Field-Effect Transistor (BiFET) and its one-transistor basic building block circuits. Examples are given for the one and two MOS gates on thin and thick, pure and impure base, with electron and hole contacts, and the corresponding theoretical current–voltage characteristics previously computed by us, without generation-recombination-trapping-tunneling of electrons and holes. These examples include the one-MOS-gate on semi-infinite thick impure base transistor (the bulk transistor) and the impure-thin-base Silicon-on-Insulator (SOI) transistor and the two-MOS-gates on thin base transistors (the FinFET and the Thin Film Transistor TFT). Figures are given with the cross-section views containing the electron and hole concentration and current density distributions and trajectories and the corresponding DC current–voltage characteristics.

Key words: bipolar field-effect transistor theory; electron and hole surface and volume channels; electron and hole contacts; bulk, SOI, TFT, FinFET; one-transistor basic building block circuits

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1. Introduction

The word "bipolar" in transistor device physics and technology has meant the presence of two kinds of elementary electrical charges[1], with a dimension of elementary charge distribution that is nearly a point (a singularity with a very small dimension or negligibly small size relative to its surrounding), and each point charge is carried by a carrier. The negative charge is carried by an electron and the positive charge is carried by a hole. In the two-particle or particle-antiparticle physics (or mathematical physics-artifact-) the hole in free space or vacuum, is known as the positron in contrast to its particle pair, the electron, while in condensed matter, such as a semiconductor or a transistor made in a semiconductor, a hole is the missing electron in a macroscopically neutral background in space containing equal numbers of positive and negative charges. In transistor device physics, aside from two different charges and charge carriers, the word "bipolar" should have been also meant the presence of two kinds of electrical currents, each from one of the two different charges and their charge carriers, differentiated by the motion direction of the two charge carriers, i.e. the electron current opposite to the direction of the negatively charged electron motion and the hole current in the direction of the positively charged hole motion. The former, bipolar charges and only unipolar current (both electrons and holes affect the electron current while there are holes in the space charge distribution but no hole current) is infrequently recognized by device physicists and the latter, bipolar charges and also bipolar currents, in the same space location, infrequently recognized and theoretically analyzed, if ever observed in transistor physics. Thus, the usage of the words bipolar and unipolar seems to have been incompletely defined, employed and even understood. For examples, bipolar (p/n) junction transistor[2] and the unipolar junction-gate field-effect transistor[3], both with a bulk or volume conduction path, were invented by Shockley on paper via mathematical analysis of novel engineering-able and manufacture-able designs, to circumvent the surface conduction paths which were experimentally observed and explained by Bardeen and Brattain[1] in their point-contact geometry of two point contacts on a germanium base, and the surface conduction path was minimized by chemical treatment of the surface, in the production type-A transistor[1] that was volume produced for the historical first solid-state-electronic switching office of the American Telephone and Telegraph company[1]. The two volume-conduction-path transistors were named bipolar and unipolar by Shockley[2, 3] because of his simplifications of the device structure (physical realization) in order to get tractable analytical solutions. But they are actually bipolar transistors, namely both electron and hole charges and currents are present, which, if both are taken into accounted, would have made the mathematical analyses and solutions very complicated if not untenable. Similarly, the modern single MOS-gate on bulk silicon field-effect transistor, known

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as the bulk-MOSFET, with the minimum of three terminals in order to transfer the input signal to the output terminal with some processing on the signal (see next paragraph), first built and measured by Kahng and Atalla[4], contains both electron and hole charges in the modulation of the electron current, even without the hole current in its three-terminal geometry. Bipolarity was unambiguous and complete in the six-terminal field-effect transistor built and measured by Fu and Sah[5] which has a MOS gate on front surface of the p-type silicon base layer to create a surface inversion current pathway for the electrons and a p/n junction gate on its back surface to control the volume current pathway for the holes in the thin p-type silicon base layer, and which has both electron (n+S) and hole (p+S) source contacts on one edge of the p-type silicon base layer and both electron (n+D) and hole (p+D) sink (or drain) contacts on its other edge to source and drain-sink the electron and hole currents. Lately, with the nanometer technology advances, silicon field-effect transistors with two MOS gates on a nearly pure and thin silicon film, has been demonstrated, known as the FinFET[6−10]. Their physical structures contains only a source and a drain contact terminal as the electron or hole source and sink (drain), therefore they have the minimum of three terminals, so they are degenerate transistors with unipolar (electron or hole) current flowing through the two surface inversion pathways induced by the voltage applied to the two gate electrodes relative to the base film layer.

From these examples just described, it becomes evident that the Shockley volume-conduction-pathway BJT and JG-FET, and the Kahng–Atalla surface conduction-pathway MOS-FET, and the latest nanometer surface conduction-pathway FinFET, all with just the minimum three terminals, are degenerate forms of the complete transistor, while the Fu–Sah MOS-JG FET with six terminals is a complete transistor. Therefore, the definition of transistor from its originator, John R. Pierce, who was asked to name the newly invented device by Bardeen and Brattain for the Bardeen–Brattain point-contact transistor (device) and by Shockley for the Shockley BJT and JG-FET (devices), can be extended and generalized to name a device, any device, that gives a response to a stimulation (electrical, mechanical, optical, chemical, biological). In order to be measurable, both the stimulation (or the input) and the response (or the output) must have a reference. Thus, the signal translation device or the transistor must have a minimum of three terminals, the input and the output, and also the reference relative to which the input and the output must be referenced and measured. For distant input and output points, each might need its own reference, and the two references may need synchronization, if possible. In the solid-state device case, if there is only one charge carrier species, then three terminals is the minimum for a complete transistor. If there are two charge carrier species, then one more terminal, the fourth terminal, is needed to provide an input-output contact point for the second charge carrier species, with or without the second charge carrier current, and without the need of a reference of the second charge carrier, or with the sharing of a common reference by the two carrier specifies. When the fourth terminal is absent, completely so that there is no second charge carrier current at all or there is not a perfect switch that can change the second charge carrier number in the transistor, the transistor will still function with two carrier species present, but somewhat slower in order to redistribute, spatially, the second charge carrier species in the transistor. But in real transistors, there are always random-irreproducible pathways with long transit time and/or long generation-recombination-trapping times, called leakage pathways, which slowly redistribute the second charge carrier to a steady-state distribution. This may be used to store charge, such as the DRAM (Dynamic Random Access Memory) cell and the Charge Transfer Gate (CTG) if an input-output contact and open-close switch are provided for the second charge carrier species. And it could also degrade the transistor performance. The floated base SOI (Silicon on Insulator) FET is an example.

About 20 months ago in March 2007[10], we noticed the unusual variations of the electron and hole currents in the DC electrical current–voltage characteristics of the latest nanometer-dimension insulated-gate (SiO_2) silicon field-effect transistor, with the two-MOS-gates on a thin and nearly pure silicon film as the base[7], known as the FinFET[6−9]. We soon realized and reported[10] that its electrical current–voltage characteristics can only be correctly explained in terms of the simultaneous presence of both the electron and hole currents, although the individual electron and hole currents could not be observed (measured) since these double-gate FinFETs in Ref.[7] had only the minimum four terminals, two gates and a source and a drain. Our discovery of the existence of the bipolar currents in the FinFETs, motivated us to develop the bipolar theory and the computer calculation of the DC current–voltage and differential conductance–voltage characteristics of the complete transistor. The one and two MOS gate inputs are selected using the analytical theory to compute both electron and hole charges and currents. The calculations have reached sufficient accuracies but still sufficiently short computation times on a 64-bit Intel-dual-core Lenovo (T60) personal computer running the Windows XP-PRO 64-bit operating system using the Intel 64-bit FORTRAN and its IMSL and MKL subroutines. Our purpose and objective have been to provide the bench-mark solutions for the Compact Model Community to help hasten their development of their compact models for the complete MOSFET, especially the next generation compact model for the nanometer double-gate thin-base silicon MOSFET, the FinFET.

In the past 20-month efforts, we have reported[11−20] the computed direct-current current–voltage (DCIV) and derivative or differential current conductance–voltage (DCgV) characteristics of the bipolar field-effect transistors, BiFETs. In these reports, we have not included the physical realizations to show the solid and plane views of the transistors which we have visualized in March 2007 when we discovered the bipolar currents in the FinFETs reported by the IMEC+assignees[7], which we had presented[10] as the Late News at the WCM in May 2007, except the plane view of one of the two alternative donor (electron) and acceptor (hole) contacts of the CMOS

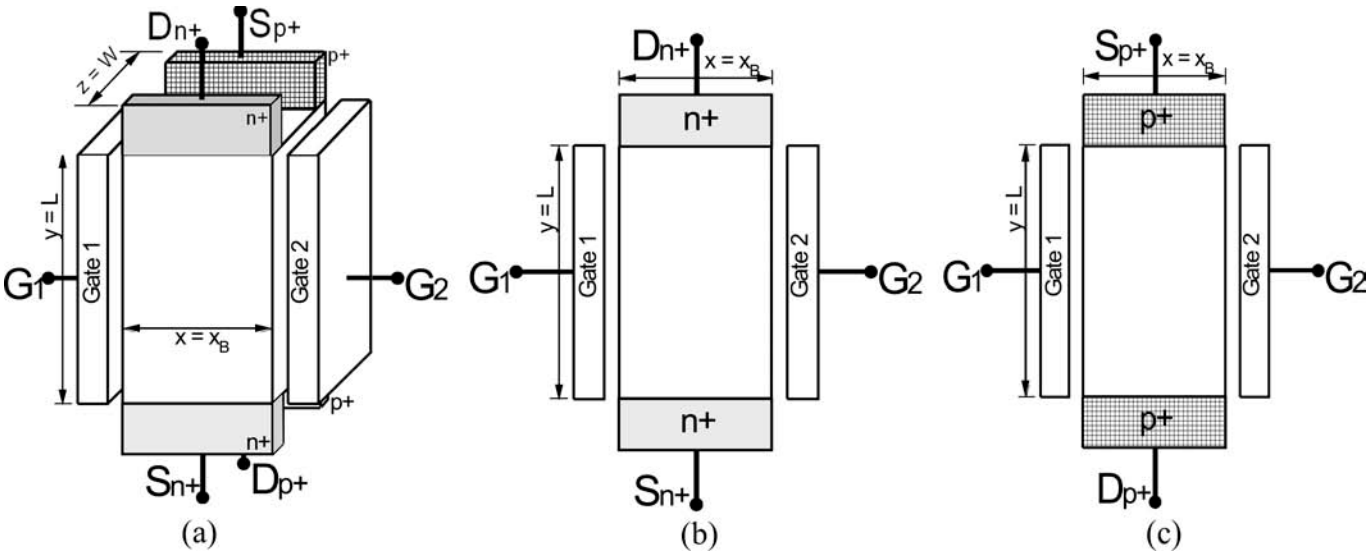

Fig.1. Physical realization of the double-gate thin-base six-terminal-minimum complete MOS field-effect transistor in rectangular solid geometry. Thickness = x_B (x-axis) Length = $y_L = L$ (y-axis), Width = $z_W = W$. (a) Three-dimensional (3-D) solid view for contacts along the thickness direction (x-axis). Contacts along the width direction (z-axis) not shown. See Ref.[20]. (b) Two-dimensional (2-D) projected plane view on the front plane ($x, y, z = 0$). (c) 2-D projected plane view on the back plane ($x, y, z = W$).

voltage inverter circuit we just reported three months ago in November, 2008[20]. Nevertheless, in the earlier reports[11–19], we did describe the natures of the contacts which were implied from the electrical boundary conditions we imposed at the contacts, such as the well-known electrical potential contact of the metal plate over an insulator for the gate, and the electron and holes, source and drain (sink) contacts to the silicon base-body-film volume in all three dimensions (3-D), using the implanted or diffused high donor concentration n+region for electron source and sink (drain) and high acceptor concentration p+region for hole source and sink (drain). The infinite sourcing-sinking (draining) rate electron–hole contact or infinite electron–hole recombination–generation velocity contact, or nearly zero-resistance linear ohmic contact, was also invoked, although its concise atomic and physical nature was dubious, as named by Bardeen as "patchy"[1], such as approximated by a very thin and very low tunneling potential barrier from patchy oxides or a metal/Si interface with very high concentration of electron-hole traps envisioned by Shockley[2]. Nevertheless, it was certainly increasingly clear to us[10] in terms of modern semiconductor device fabrication technology, that even a possibly highly manufacturable and reproducible contact technology can be had by mixing of lithographically defined n+ and p+ island regions or just a spatial mixing of donor and acceptor impurity atoms easily attainable by ion implantation or diffusion sources, characterized by critical atomic and geometrical dimensions. It is the purpose of this report to illustrate the physical realizations. The six-terminal minimum and physically symmetrical complete field-effect transistor with the two MOS gates will be the starting illustration. The degenerate transistors can then be simply illustrated by floating and/or connecting the six terminals in different combinations. The physical realization of the one-BiFET circuits will also be illustrated.

2. Physical Realization of the MOS-BiFET Device

The 3-dimensional (3-D) view of the complete MOSFET is shown in Fig.1 (a). It has two MOS gates on a rectangular silicon film of thickness, X_B, length $Y_L = L$ and width $Z_W = W$, to be called base. It has the six minimum number terminals or contacts, the two gate contacts and the four electrical current contacts, two on each of the two edges of the base. For the four current contacts, we shall use the well-understood and reproducibly fabricated electron and hole sources and sinks, to be denoted by the traditional symbols, n+S and n+D for heavily donor impurity doped (or implanted) or high donor impurity concentration source and drain contacts, similarly for the hole source and drain contacts, p+S and p+D. There are two device design innovation opportunities, one from the width of these source and drain contacts and the other from their spatial orientations. The 3-D view illustrated in Fig.1 (a) provides the electron and hole currents independently under both gates. For the source and drain contacts rotated 90 degree from the four shown in Fig.1 (a), we have the electron and hole currents physically separated, electrons under gate 1 and holes under gate 2, although each can also be dominated by both gates, just like that in Fig.1 (a) which have the electron and hole currents spatially together, electrons and holes both under gates 1 and 2. Basic Building Block circuits leveraging these geometries and orientations are described in section 3. Figures 1 (b) and 1 (c) show the 2-dimensional (2-D) front and back views. In the following discussions of physical realizations, the front view given in Fig.1 (b) will be used to show the electron densities and electron trajectories or electron current. The back view given in Fig.1 (c) will be used to show the hole densities and hole trajectories or hole currents. The logarithmic local concentrations of the electrons and holes are roughly given

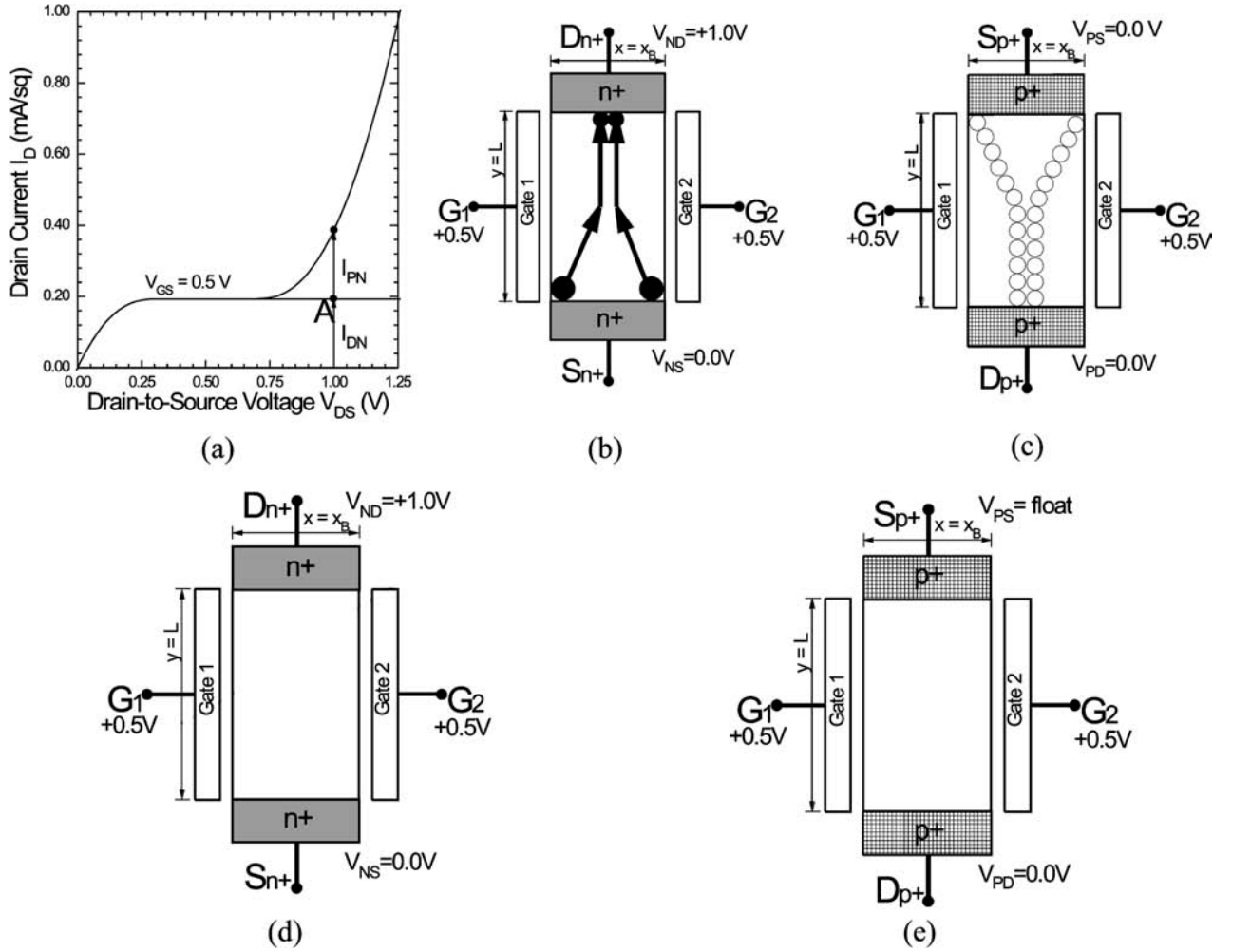

Fig.2. Two MOS gates (double gate) thin-base bipolar field-effect transistor (BiFET) with bipolar (electron and hole) charge distributions and unipolar (electron) current. (a) Output current–voltage characteristics, I_D–V_{DS}. (b) Front view of electron and (c) back view of hole charges and current densities distributions in the Uni-Current saturation range of the drain-source bias voltage. Charge and current density distributions are left blank in (d) and (e) which correspond respectively to (b) and (c) but with the hole source contact p+S ($y = L$) floating here, instead of grounded and shorted to p+D ($y = L$) in (b) and (c). The applied drain-source voltage is twice the applied gate-source voltage referring to the electron channel so that the boundary line or plan between the two sections (electron emitter section or hole collector section from $y = 0$ to $y = L/2$, and electron collector section or hole emitter section from $y = L/2$ to $y = L$) is located at $y = L/2$.

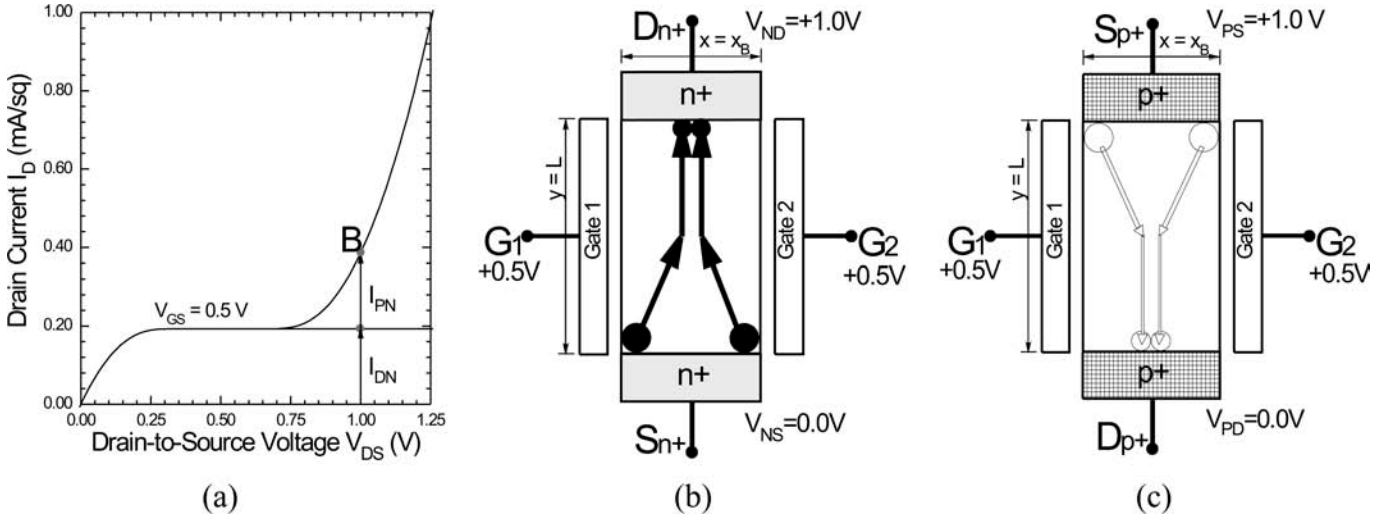

Fig.3. Two MOS gates (double gate) thin-base bipolar field-effect transistor (BiFET) with bipolar (electron and hole) charge distributions and bipolar (electron and hole) currents. The 3-part figure is similar to those of Figs.2 (a), 2 (b) and 2 (c), except the presence of both electron and hole currents or bipolar current here in contrast to Fig.2 with only electron current, by having here n+D ($y = L$) and p+S ($y = L$) tied together. (a) I_D–V_{DS} with curve B and operating point B. (b) and (c) Sketches of electron and hole charge densities and trajectories.

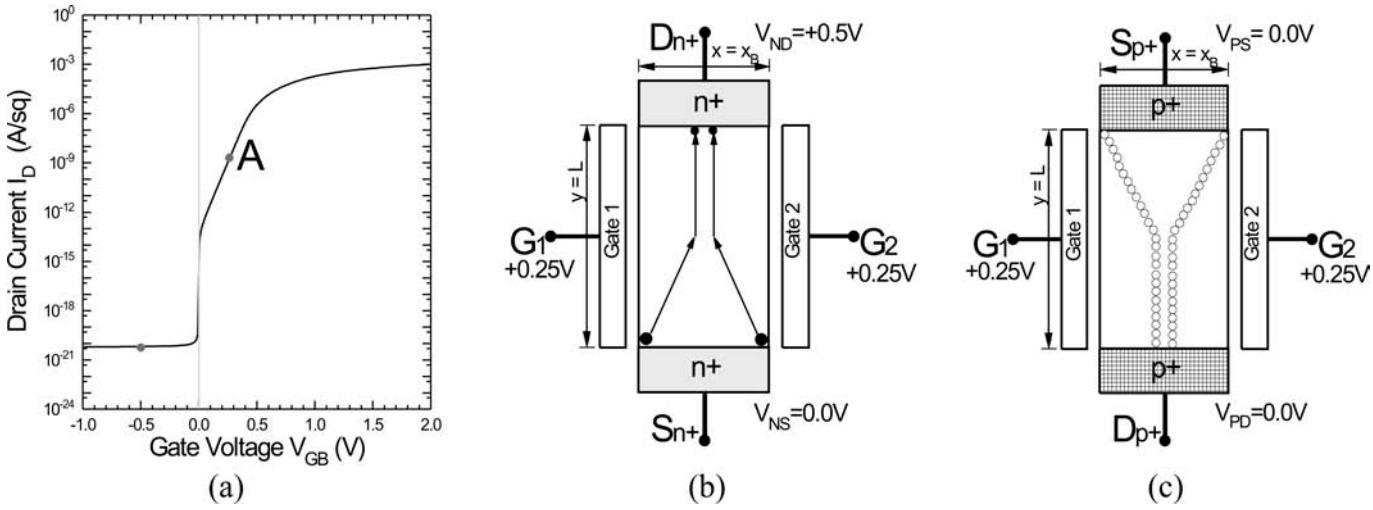

Fig.4. Unipolar current of the 2-Gate MOS BiFET same as Figs.2 (a), 2 (b) and 2 (c) except it is in the subthreshold range and (a) is the transfer characteristics while (b) and (c) are for the subthreshold point A in (a).

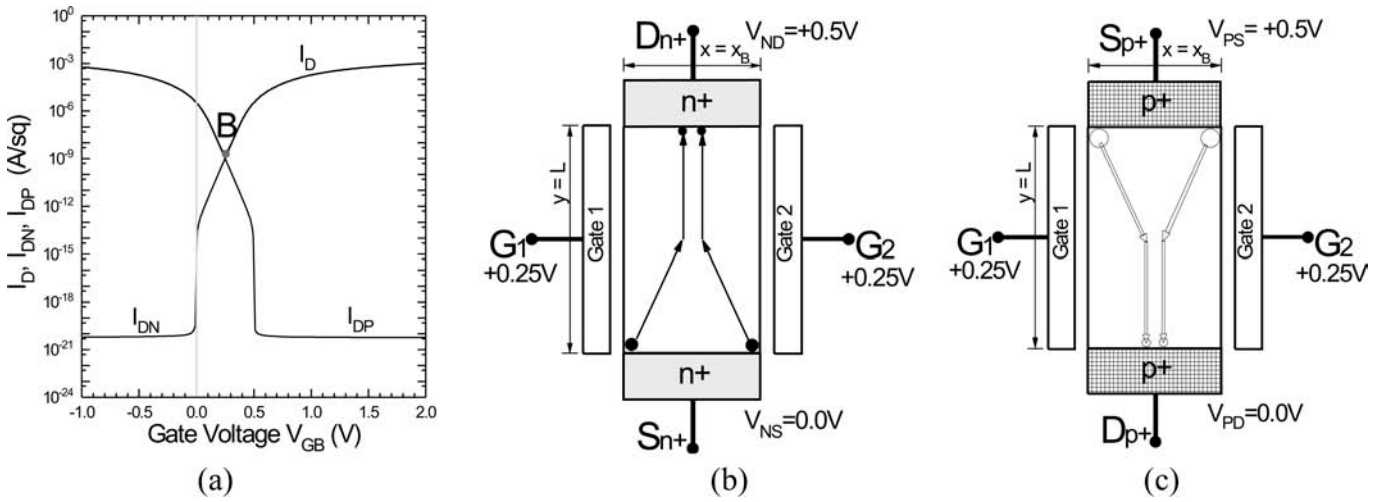

Fig.5. Bipolar current of the 2-Gate MOS BiFET. Similar to Figs.4 (a), 4 (b) and 4 (c) in the subthreshold current saturation range except it is here the Bipolar current with n+D and p+S at $y = L$ tied together to give the Bipolar current. The unique feature is the V-shaped I_D–V_{GS} which led us to discover the presence of both electron and hole currents, hence coined the bipolar field-effect transistor in March 2007.[10].

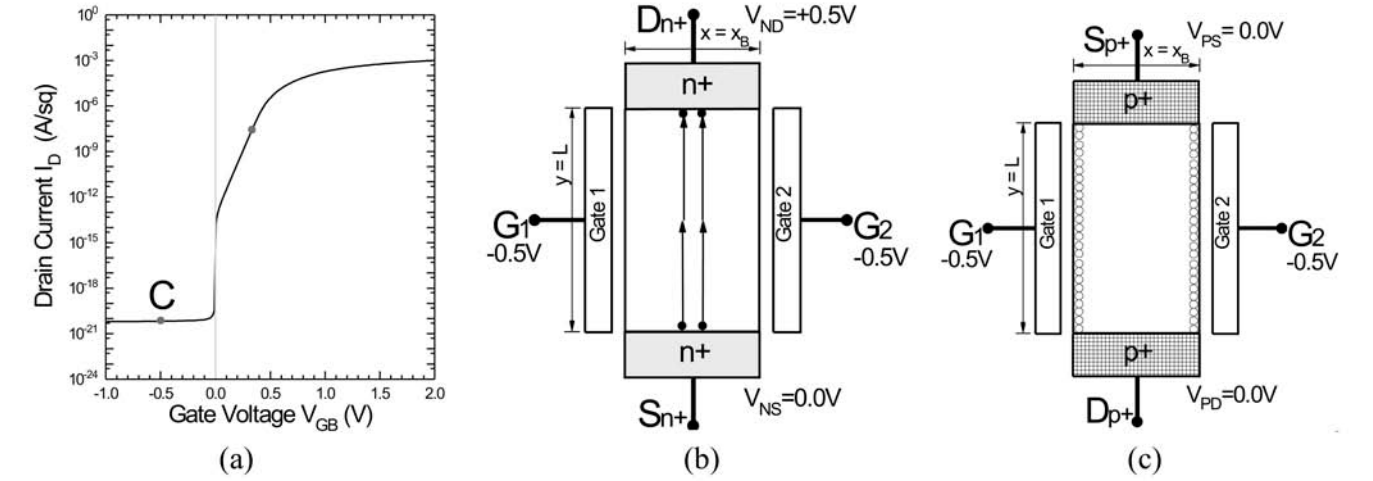

Fig.6. Unipolar current of the 2-Gate MOS BiFET. Similar to Fig.4, except it is here in the cut-off range or surface 'accumulation' range of the unipolar current (electron), therefore no electron surface channel current, only electron volume channel current as indicated by point C in figure part (a).

by the area or square of the diameter of the unfilled and filled circles. We also selected the simplest applied voltage configurations to illustrate the division of the physical length of the transistor into two electrical sections, the emitted section and the collector section, on account of the short channel condition $L/L_D \ll 1$ with the Debye carrier screen length L_D of nearly 25 μm for pure base at room temperature with the intrinsic carrier concentration of $n_i \sim 10^{10}$ cm^{-3}. The boundary between the two sections is at the half plane, or line, $y = L/2$, for $V_{DS} = 2V_{GS}$ with all the build-in potentials absorbed into the terminal voltages to make each the effective terminal voltage applied to that terminal. They also show the two kinds of channel locations, the surface channels (both inversion and accumulation) and the volume channel (either n-type from the n-type base, or p-type from the p-type base).

2.1. Double Gate BiFET

The high-current or strong inversion range of operation of the 2-gate thin pure-base bipolar MOSFET (FinFET) is illustrated in Figs.2 to 6. Figures 2, 4 and 6 are for the bipolar-steady-state-charge/unipolar-current mode of operation. Figures 3 and 5 are for the bipolar-steady-state-charge/bipolar-current mode of operation. The high current saturation (Unipolar) and parabolic rising (Bipolar) modes of operation are shown in Figs.2 and 3. The subthreshold and cutoff ranges of the unipolar and bipolar current modes of operation are shown in Figs. 4, 5 and 6. The other case, the bipolar-steady-state-charge/unipolar-current with a constant "minority" carrier charge in the base layer, is illustrated in the next section on physical realizations of Basic Building Block circuits, as the 1-BiFET DRAM cell.

The curve labeled A in Fig.2 (a) shows output current–voltage characteristics of the Bipolar FinFET, I_D–V_{DB}, with $V_{n+SB} = V_{p+DB} = 0$ as the reference; and only electron current and no hole current, $I_{DP} = 0$, so $I_D = I_{DN} + I_{DP} = I_{DN}$, that is, it is the BiFET with bipolar charges (as always dictated by nature) but unipolar (dictated by men) current. There are two different sets of DC steady-state electron and hole or bipolar charge concentration distributions and their corresponding DC steady-state electron current-density distributions, depending on the boundary conditions, namely, whether both the hole drain and source contacts, p+D and p+S, are grounded (hence tied with no circulating current for this case of BiFET with Unipolar Current) as shown in Figs.2 (b) and 2 (c), or one floated and the other grounded, as shown in Figs.2 (d) and 2 (e). Although there is no DC steady-state hole current, holes are still supplied and extracted through the grounded terminal p+D with p+S ground or floating to give the different steady-state hole distributions in the base volume and surface at different DC voltages applied to the six terminals. The I_D–V_{DB} curve labeled A in Fig.2 (a) was computed for both p+S and p+D grounded, shown in Figs.2 (b) and 2 (c), with the mathematical boundary conditions for the electrochemical potentials of the electrons and holes given by[21]

$$V_P(y = 0) = V_{BB} = 0, \quad V_N(y = 0) = V_{SB} \tag{1}$$

$$V_P(y = L) = V_{BB} = 0, \quad V_N(y = L) = V_{DB}. \tag{2}$$

The current–voltage characteristics of the single grounded hole contact, Figs.2 (d) and 2 (e), has not been computed, however, its I_D–V_{DB} and charge density and current density distributions are not expected to be very different from those of both grounded hole contacts shown in Figs.2 (a), 2 (b) and 2 (c), the latter two were sketches, nevertheless, it offers opportunities for contact geometry design innovations.

The bipolar-charge BiFET connected to give bipolar current also has the output or I_D–V_{DS} characteristics indicated by the curve labeled B in Fig.3 (a). The rise of I_D beyond the current saturation drain voltage of the UniFET theory, nearly parabolically with increasing drain-source voltage for pure base is the unambiguous and decisive signature of the onset and parabolic rise of the second carrier current. At the point B where $I_{DN} = I_{DP}$ and $I_D = I_{DN} + I_{DP}$, the electron and hole concentration distributions and also current densities are mirror image of each other as shown in Figs.3 (b) and 3 (c), as a result of our simplification assumption of complete symmetry, namely, equal electron and hole mobilities, diffusivities, density of state effective masses and threshold voltages.

The subthreshold and cutoff ranges are shown in Figs. 4, 5, and 6. Figures 4 (b) and 4 (c) are the sketched schematic plane view (x–y) assuming no variation in the z-direction of the electron and hole concentrations and current density trajectories for the BiFET in the Uni-Current mode or applied voltage configuration, namely, $V_{p+SB} = V_{p+DB} = 0$ so the hole current is zero. Figures 5 (a), 5 (b) and 5 (c) are for the BiFET subthreshold bipolar-current at the minimum, B, shown in the V-shaped current of the BiFET connected in the Bipolar Current configuration, that is, none of the minimum of six terminals are left not connected. Figures 6 (a), 6 (b) and 6 (c) are for the Unipolar turned-off current of the BiFET, labeled C on computed I_D–V_{DS} in the accumulation range.

2.2. Single-Gate BiFET

The single-gate BiFETs are illustrated by Figs. 7 to 11. These are the BiFETs for the traditional semi-infinite thick base MOSFET, known as the Bulk MOSFET, from the 1964 and 1966 MOST threshold–voltage models investigated by one of the authors, Sah, for the constant threshold–voltage model with a voltage-independent effective bulk-charge contribution to the threshold voltage, and with the voltage-dependent bulk-charge that accounts for the voltage-dependent threshold voltage. They are also the BiFETs for the SOI FETs (SOI—Silicon on Insulator) which has a finite base thickness.

Figures 7 (a), 7 (b) and 7 (c) are for grounded hole source and drain contacts, p+S and p+D, hence the BiFET-MOST and also BiFET-SOI with Unipolar current (Uni-Current).

Figures 8 (a), 8 (b) and 8 (c) are for BiFET-SOI with the n+D and p+S terminals connected and n+S and p+D terminals connected, hence the BiFET-SOI with Bipolar Current (Bi-Current). It excludes the BiFET-MOST of Figure 7 because the semi-infinite thick MOST or bulk MOSFET would have given infinite hole current. Note that Fig.8 (a) shows a

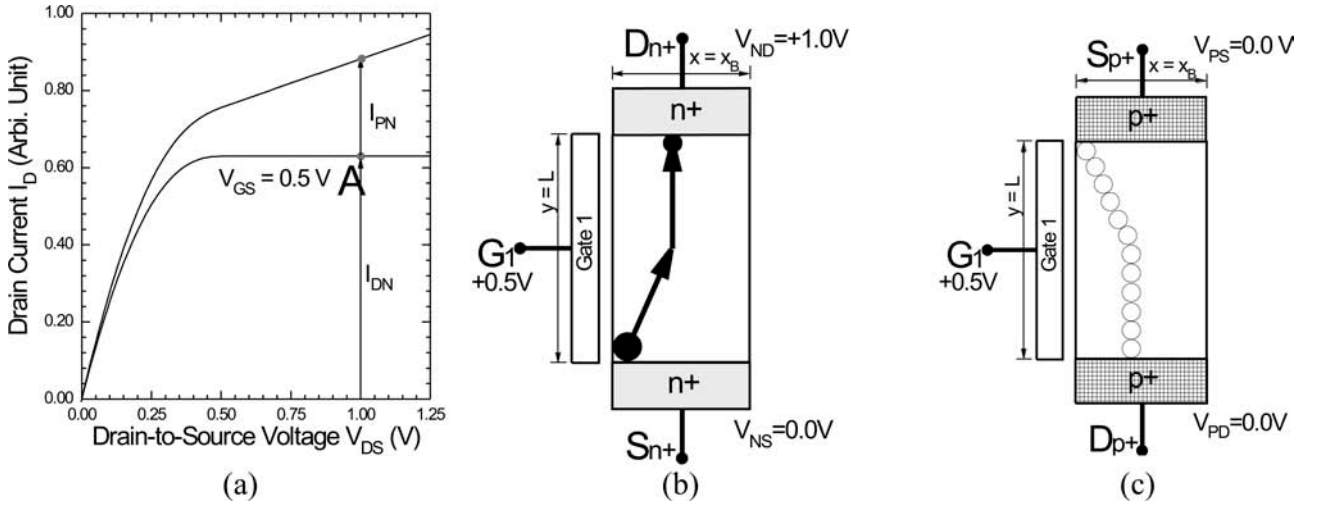

Fig.7. One-Gate Unipolar-Current (Uni-I) in the Single-Gate (1G) MOS BiFET for both the semi-infinite-thick-base Bulk-MOSFET and the thin-base Silicon-On-Insulator (SiO_2) SOI-MOSFET. (a) The output characteristics I_D–V_{DS} with curve labeled by point A for the Unipolar-Current and the upper not-labeled IV curve for the Bipolar-Current biases. (b) the front and electron and (c) the back and hole 2-D views of charge (bipolar) and current (unipolar) density distributions.

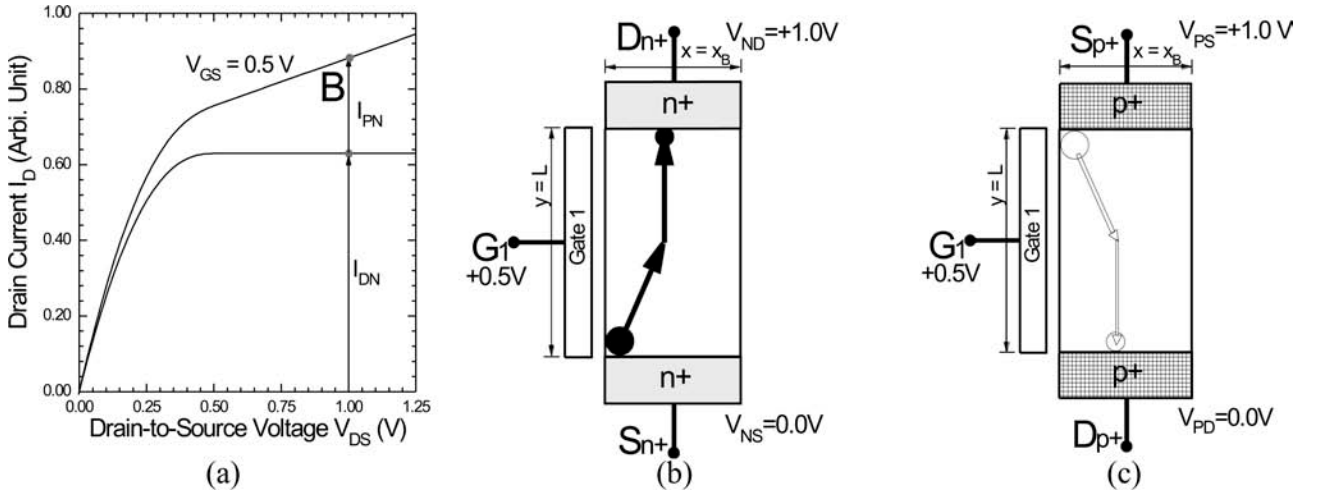

Fig.8. One-Gate Bipolar-Current (Bi-I) otherwise similar to Fig.7 for the upper I_D–V_{DS} labeled by operating point B in Part (a).

linear rise of the drain current with the drain voltage when the drain voltage is higher than the drain current saturation voltage of the Uni-Current case. This resistive component of the drain current comes from the hole current in the volume region of the p-type Si On the Insulator (SOI) transistor when p+S contact to the p-Si body-film is tied to n+D contact to the p-Si body film to have the same voltage applied to both terminals.

The three parts of Figs.9, 10 and 11 are BiFETs for the single-gate on nearly intrinsic base, with an acceptor impurity concentration in the base-body of $P_{AA} = 10^{10}$ cm^{-3}. Figures 9 and 11 are the Unipolar Currents of the BiFET of both the bulk MOST and the SOI transistor with a finite base thickness which accounts for the very high subthreshold and accumulation currents ($\sim 5 \times 10^{-10}$ A/sq) due to the thick electron surface inversion channel not limited by the p-Base thickness like the two-gate case presented earlier or the SOI transistor with thinner base. This is further indicated by the curve with the very low accumulation current ($\sim 10^{-17}$ A/sq at $V_{GS} = -0.5$ V) which has a $P_{AA} = 10^{15}$ cm^{-3}. Figure 10 is the Bipolar Currents of the BiFET for the SOI transistor with the n+D and p+S tied together. It shows the signature subthreshold transfer characteristics of V-shaped I_D–V_{GS} due to the presence of both electron and hole surface channels.

3. Physical Realization of the One-MOS-BiFET Circuit

Several one-transistor MOS-BiFET circuits will be described. The physical realization and the electrical characteristics will be given. These are the one transistor basic building block (1T-BBB) circuits with many of which interconnected, the integrated circuits are built of. All of these involve connecting the six terminals in special ways, some very simple, such as the CMOS, NMOS and PMOS voltage inverters, and some more complicated crisscross connections such as the SRAM.

3.1. DRAM Cell and Photodetector

The simplest physical realization of a basic building block circuit function by one MOS BiFET transistor is the dynamic random access memory cell, DRAM. The 6-terminal 2

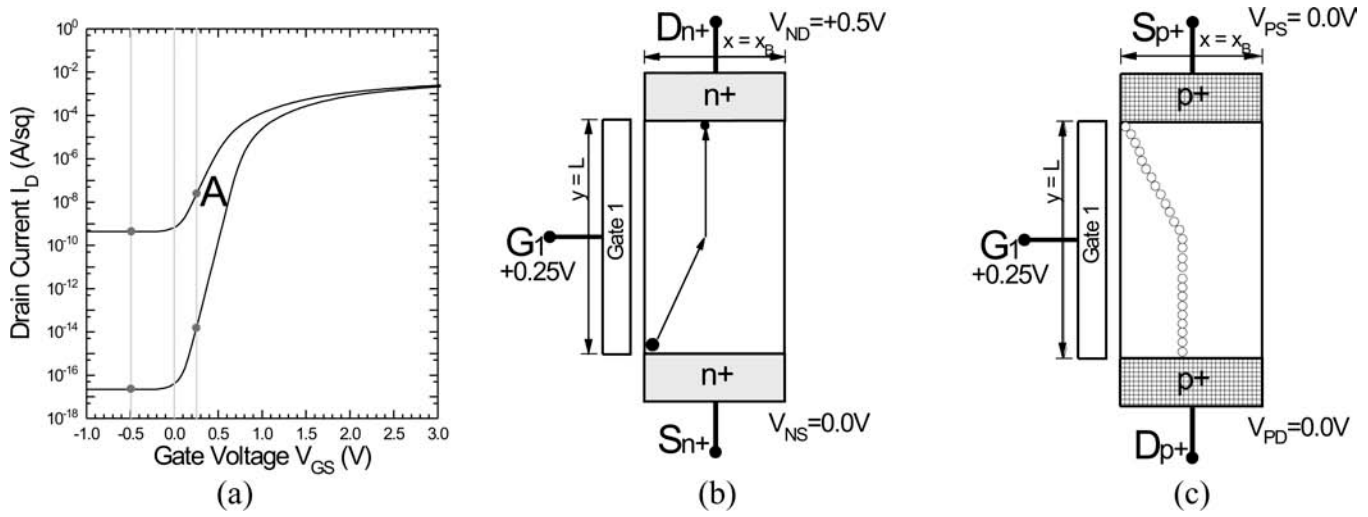

Fig.9. 1-G MOS BiFET with Uni-I similar to Fig.7 except biased into the subthreshold range indicated by curve A and point A in part (a) of the transfer characteristics. The base is nearly pure, at acceptor concentration of $P_{AA} = 10^{10}$ cm^{-3}, while the lower curve is for $P_{AA} = 10^{15}$ cm^{-3}. [10]

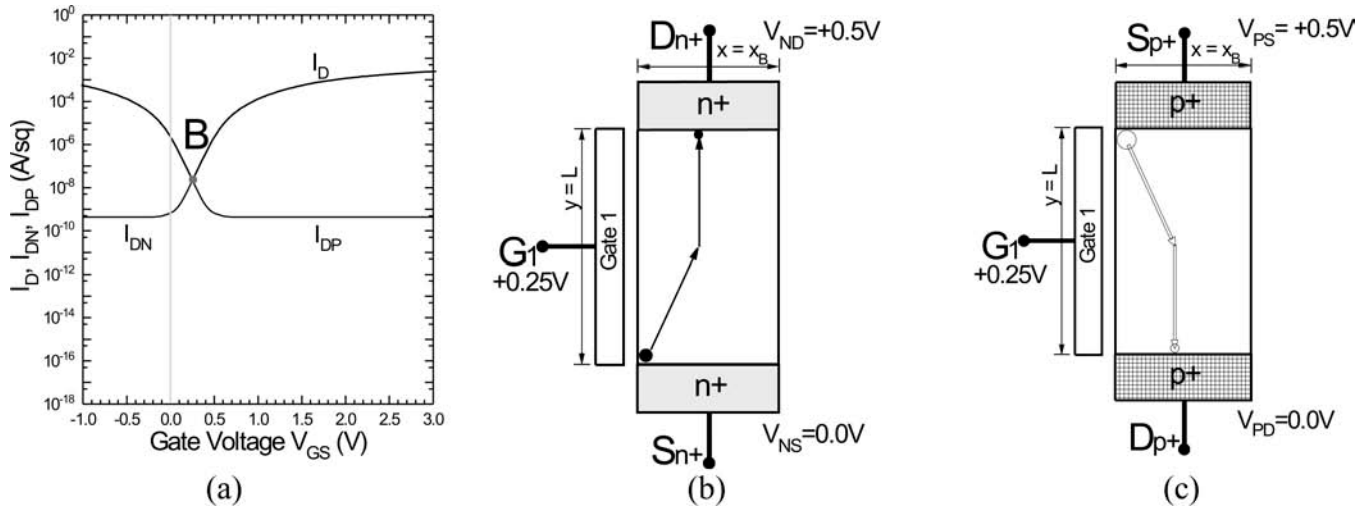

Fig.10. 1-G MOS BiFET with Bipolar Current (Bi-I) with the V-shaped I_D–V_{GS} at the minimum point B in Part (a).

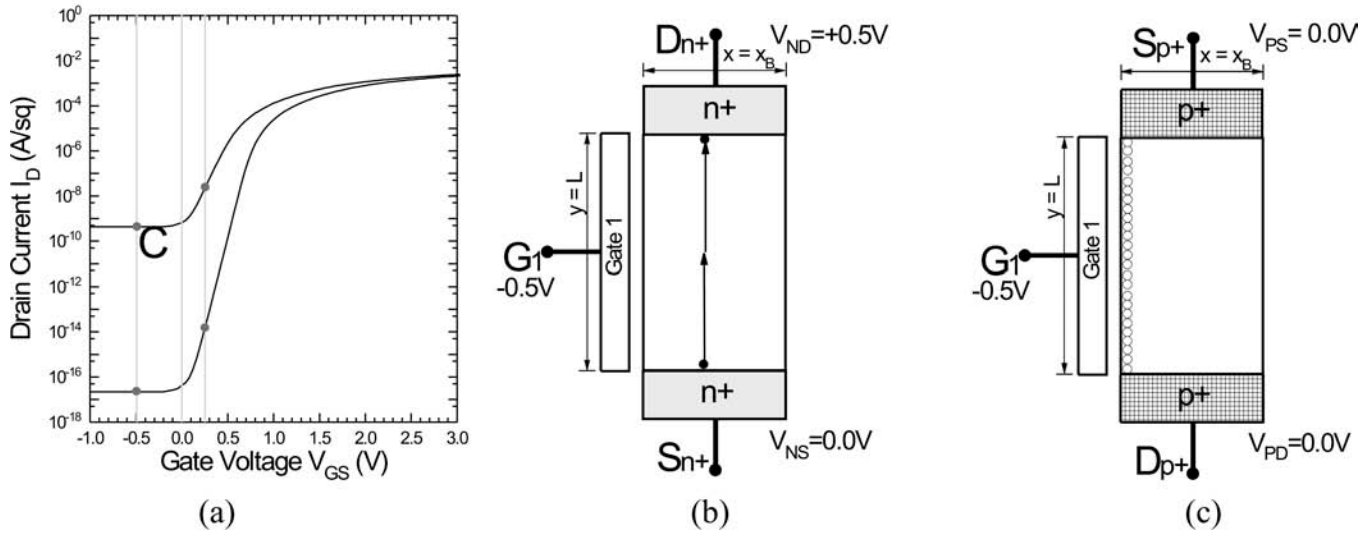

Fig.11. 1-G MOS BiFET with Unipolar Current (Uni-I) in the surface electron depletion range with hole volume channel current dominant, indicated by point C in the I_D–V_{GS} transfer characteristics of Part (a).

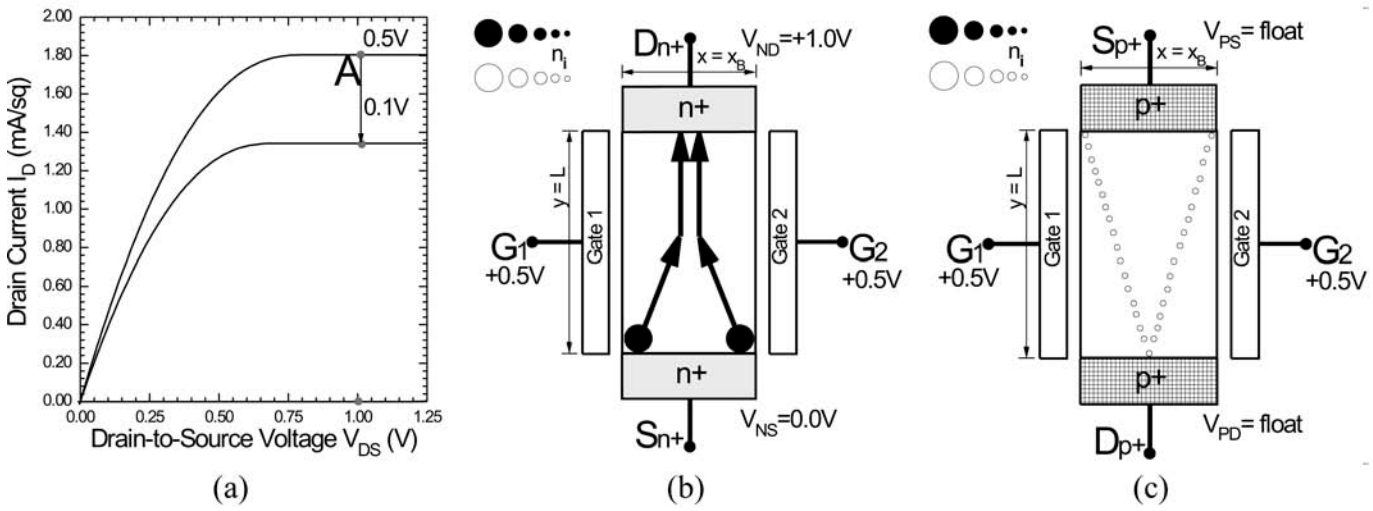

Fig.12. DRAM and Photodetector circuit realized by one BiFET without hole charge stored at point A in Part (a).

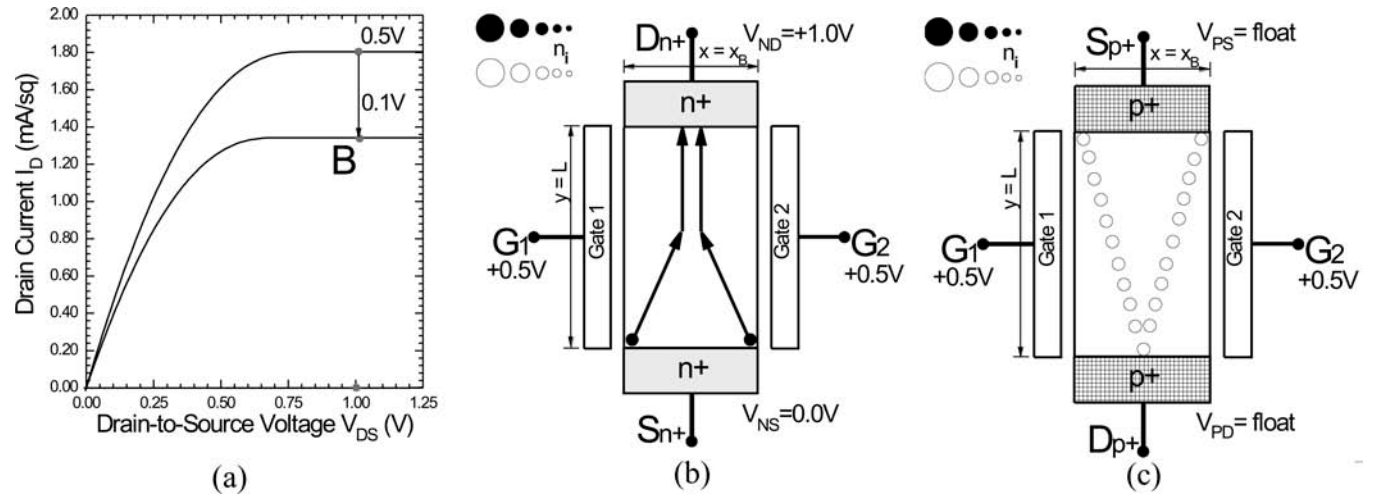

Fig.13. DRAM and Photodetector circuit similar to Fig.12, with intermediate hole charge stored to give a gate threshold shift of 0.1 V resulting in lower drain current at point B in Part (a).

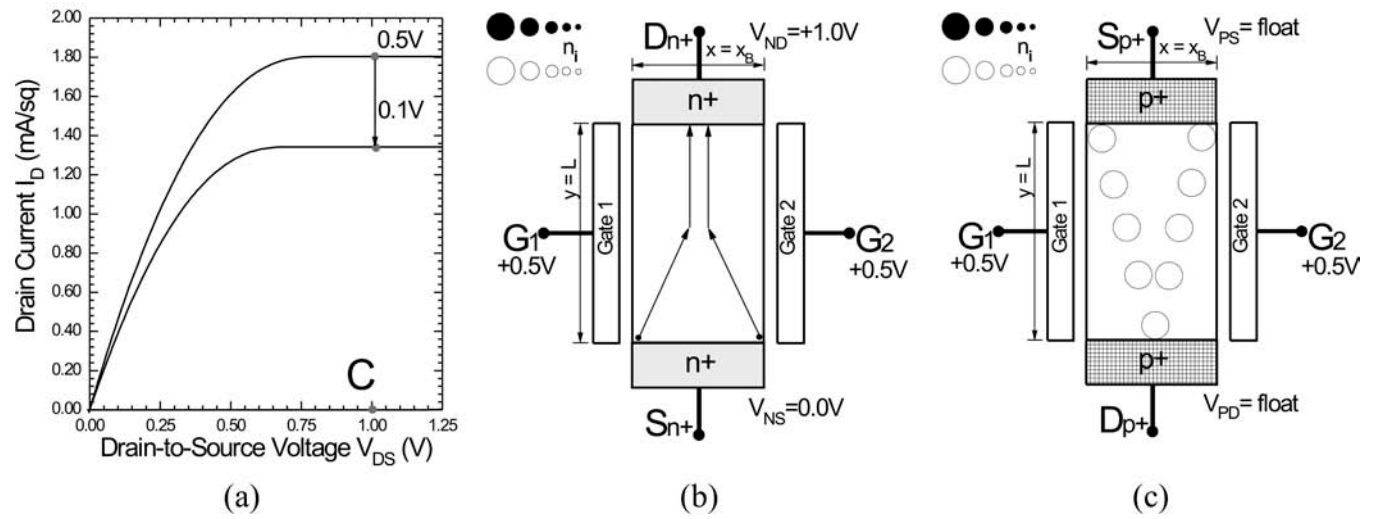

Fig.14. DRAM and Photodetector circuit similar to Fig.13, with large hole charge stored to give a gate threshold voltage shift resulting in nearly zero drain current ar point C in Part (a).

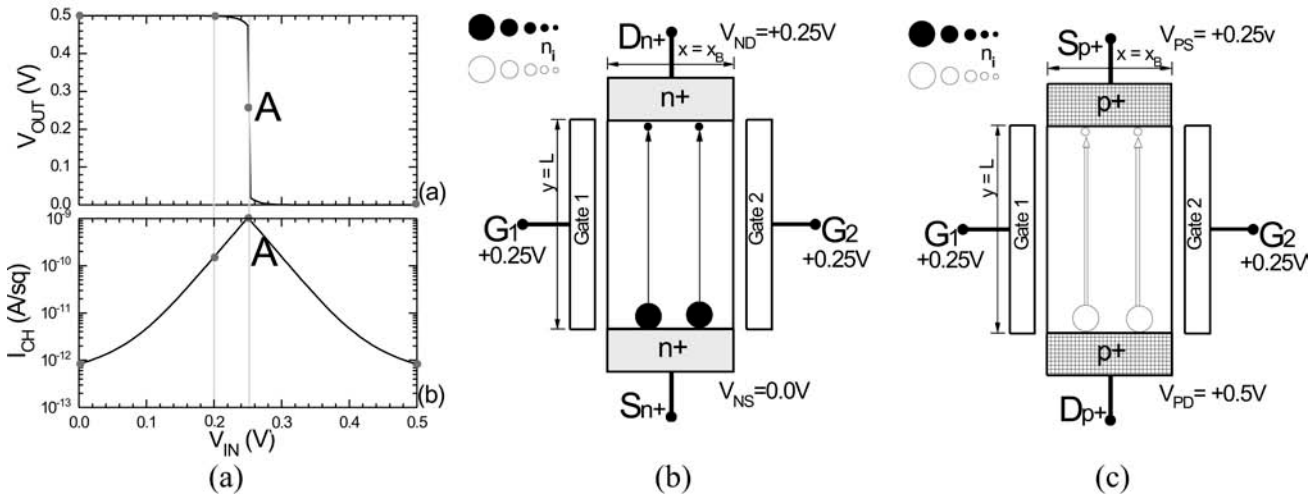

Fig.15. CMOS voltage inverter realized in one MOS BiFET at the switching point A in Part (a). [20]

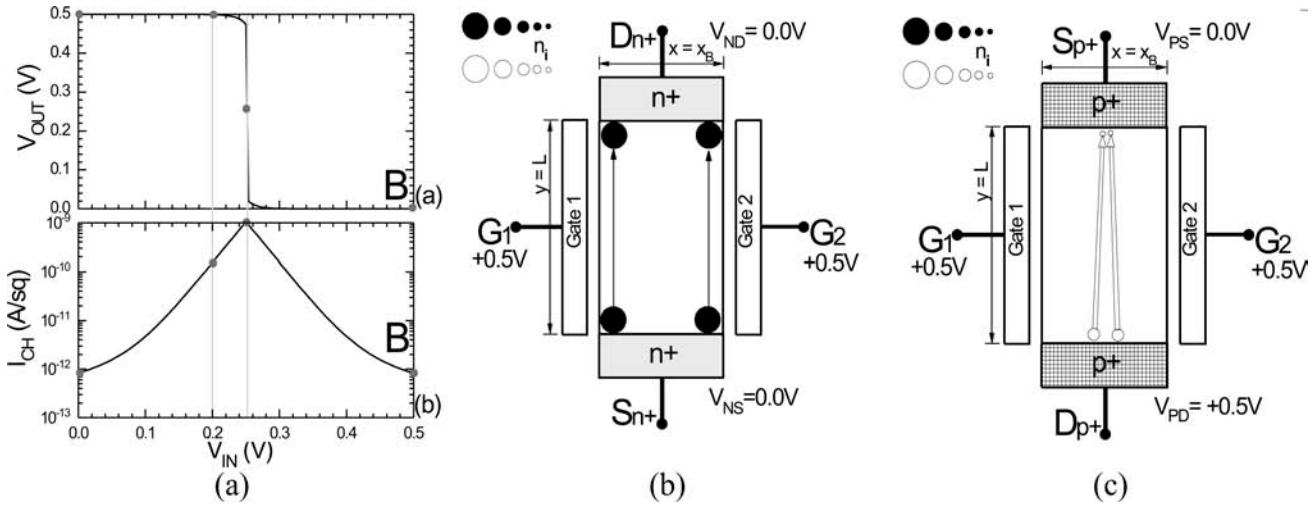

Fig.16. CMOS voltage inverter realized in one MOS BiFET at the quiescent point B in Part (a). [20]

MOS-gate BiFET with the two hole or two electron contacts to the base floating, will provide the two states, by setting the charges stored in the floating base to two values to represent the digital memory states of one and zero. The dynamic limitations (noise, thermal generation-recombination rate and alpha-cosmic ray upset) come from the amount of charge that can be injected into the floating base and the leakage of the stored charge through various leakage paths. The three parts of the three figures, Figs.12, 13 and 14, give the characteristics of such an 1T-DRAM cell made of one 6-terminal MOS BiFET. The two p+ contacts need to be floated. Only one gate is needed. The three figures represent the off and on states and an intermediate state of the BiFET. The cross-section views of figures (b) for electrons and (c) for holes give the local values of the electron and hole concentrations and current densities.

These can also be viewed as models for a photodetector to detect lights with energy larger than the silicon energy gap (~1.2 eV) and for monitoring and estimating the fluctuation and noise in the floating base application of the MOS BiFET.

3.2. The CMOS Voltage Inverter

The physical realization of the traditional two MOS UniFETs (one nMOST and one pMOST, and both must be inversion surface channel type) CMOS voltage inverter with 1-transistor MOS BiFET was theoretically analyzed by us and recently reported[20]. The schematic cross sectional views at four operating points are given by the three parts, (a), (b) and (c) of four figures, Figs.15, 16, 17, and 18. All of these are self-explanatory. The operating point of each bias configuration is labeled alphabetically, A, B, C, and D on the VV and IV curves of figure's part (a). One unique feature, used in our analytical solution and computation of the IV and VV characteristics was the peak current point, labeled A in the VV and IV curves of Fig.15 (a). Figures 15 (b) and 15 (c) shows that the local electron and hole concentrations are equal at all points in the base. Since this is the pure base case, therefore, it means electrical neutrality at all points in the base of the transistor or flatband.

The description just made for the CMOS voltage inverter using one MOS BiFET with narrow pure base can be readily extended to the RNMOS, RPMOS, NMOS and PMOS voltage inverters. For example, the resistance load NMOS inverter is attained using a p-type base as the resistance load with the upper p+ contact shorted to the top n+D contact and the lower

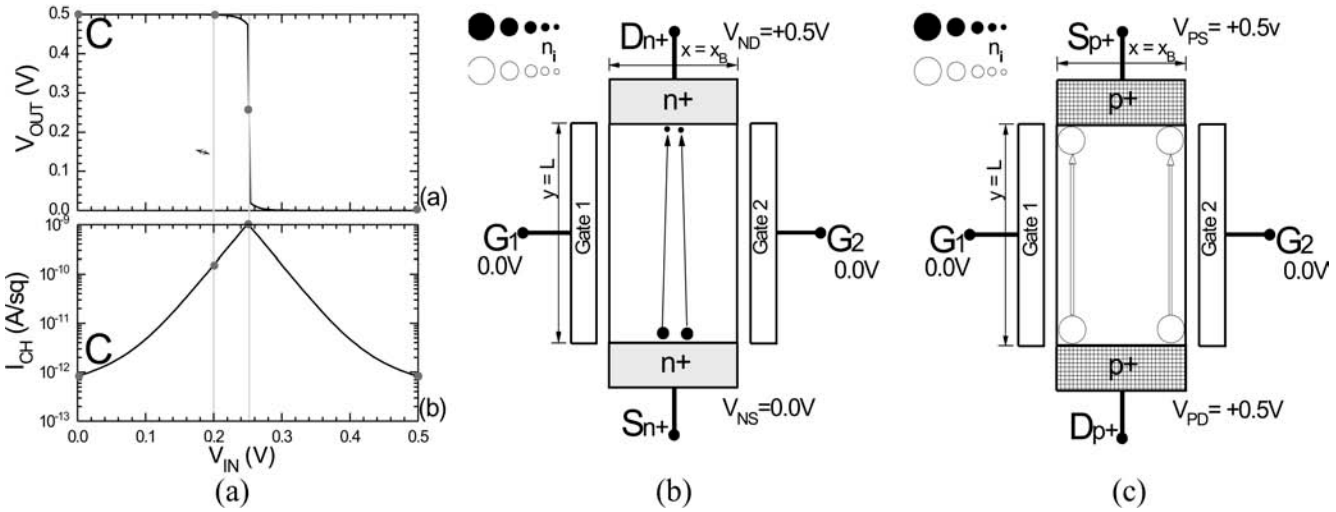

Fig.17. CMOS voltage inverter realized in one MOS BiFET at the quiescent point C in Part (a). [20]

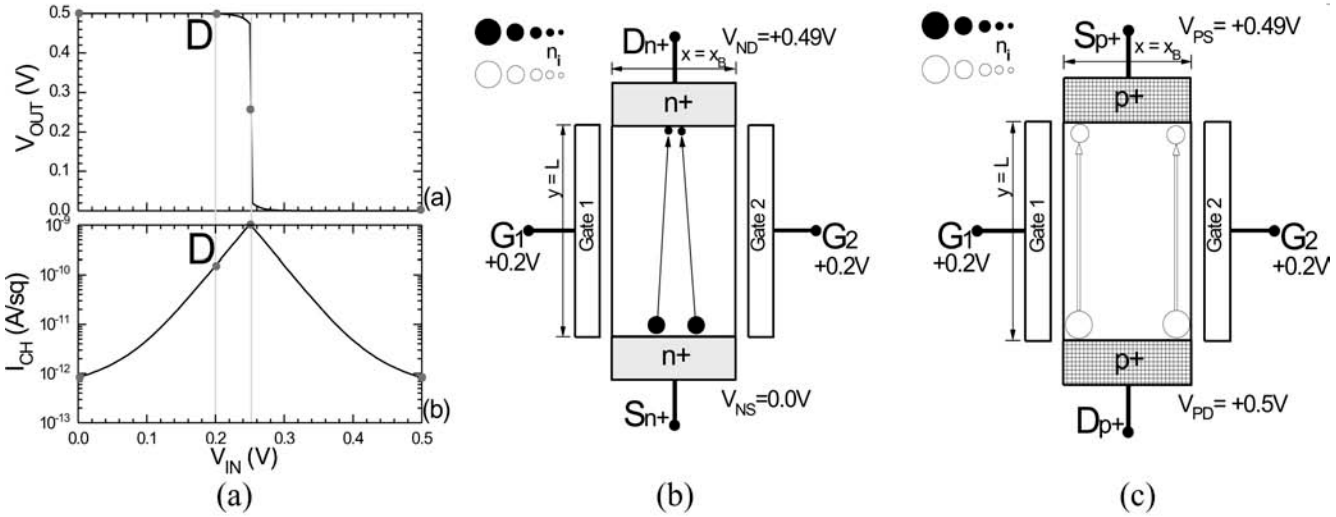

Fig.18. CMOS voltage inverter realized in one MOS BiFET at point D before switching in Part (a). [20]

p+ contact connected to a positive power supply while the lower n+ contact is grounded.

4. Summary

We have presented in this paper the physical realizations of the 2-Gate and 1-Gate MOS BiFETs (the Bulk, SOI, TFT and FinFET) and several 1-transistor basic building block circuits (DRAM, Photocell, CMOS, RNMOS, NMOS). For each we also sketched the electron and hole concentrations and electron and hole current densities.

Acknowledgment

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