A 2.4-GHz low power dual gain low noise amplifier for ZigBee*

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Abstract: This paper presents a fully differential dual gain low noise amplifier (DGLNA) for low power 2.45-GHz ZigBee/IEEE 802.15.4 applications. The effect of input parasitics on the inductively degenerated cascode LNA is analyzed. Circuit design details within the guidelines of the analysis are presented. The chip was implemented in SMIC 0.18-μm 1P6M RF/mixed signal CMOS process. The DGLNA achieves a maximum gain of 8 dB and a minimum gain of 1 dB with good input return loss. In high gain mode, the measured noise figure (NF) is 2.3–3 dB in the whole 2.45-GHz ISM band. The measured 1-dB compression point, IIP_3 and IIP_2 is –9, 1 and 33 dBm, respectively. The DGLNA consumes 2 mA of current from a 1.8 V power supply.

Key words: CMOS low noise amplifier; input parasitics; low power; noise figure; ZigBee; IEEE 802.15.4
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1. Introduction

Wireless sensor networks have recently seen significant growth in many applications because of their advantages of low power and low cost, ranging from remote sensing, security surveillance, healthcare, and environmental monitoring. ZigBee/IEEE 802.15.4 is one of the most promising protocols suitable for it, which defines three radio bands (868 MHz/915 MHz/2.45 GHz). This paper refers to the third band, because this band is the only ISM (industrial, scientific, and medical) bands worldwide[1]. Although ZigBee/IEEE 802.15.4 has established many strategies to guarantee low power operation, such as the modulation scheme, the ad-hoc network organization scheme, and the power management mechanism, it still imposes stringent power design constraints for sensitive RF and analog circuits.

As the first active module in an RF receiver, the LNA plays an important role in the whole system[2]. An inductively degenerated common-source LNA (CSLNA) can achieve a good input match and a low noise figure via setting the inductors and input MOSFET gate-source capacitor to resonate at the required frequency. In addition, many studies have explored noise optimization techniques[3, 4], which makes it a good choice for a narrow band application. However, analysis of input parasitics is negligible in these studies. Chandrasekhar *et al.*[5] applied the electro-static discharge (ESD) protection and input parasitics to the design of the LNA only with the assumption of single gate inductor matching, which limits the value of the parasitic capacitance, as well as the maximum achievable ESD protection. This paper examines this effect with an additional matching network from the viewpoint of low power design, which not only makes the ESD design more versatile, but also makes the measurement more robust with regard to parasitics in the case of practical use; even for mass production. What is more, both the Spectre assistant design method in the circuit set-up phase and the advanced design system (ADS) assistant strategy in the measurement phase are first explored to make the design flow more efficient.

2. Required LNA performance

Since one of the significant features of ZigBee is low power, the direct conversion receiver architecture becomes the most attractive candidate for it. As shown in Fig. 1, the RF signal received by the antenna is first amplified by the LNA to suppress the noise of the subsequent stages, and is then converted from 2.45 GHz to the DC field. The fixed gain amplifier (FGA) is set to restrain the large noise generated by the channel selecting low pass filter (LPF). The automatic gain control (AGC) circuits ensure that the receiver can fully satisfy the dynamic range of the standard, and the analog-to-digital converter (ADC) converts the signal to a digital field to facilitate digital signal and protocol processing.

During the design of a front-end, one of the most important considerations is how to distribute the large gain among various blocks to achieve the required system dynamic range, noise figure, and linearity, where the specifications of LNA take very important effects. According to the Friis equation, the receiver noise figure is dominated by the noise figure of the first stage, assuming that the gain of the first stage is large enough to suppress the noise of the following stages. The noise figure of the receiver is determined by the sensitivity, the signal bandwidth and the signal to noise ratio for the demodulation (SNR_{dm}) under a specific bit error ratio (BER), just as shown in Eq. (1). In respect of a ZigBee transceiver, as the direct spread spectrum scheme (DSSS) provides a 9 dB process gain, the SNR_{dm} is relaxed from 9.5 to 0.5 dB for O-QPSK modulation under a 1% packet error rate (PER). Therefore, the noise figure of the receiver is relaxed to about 20 dB considering a 5.5 dB implementation margin. Hence, a noise figure of not more than 3 dB is assumed for the LNA.

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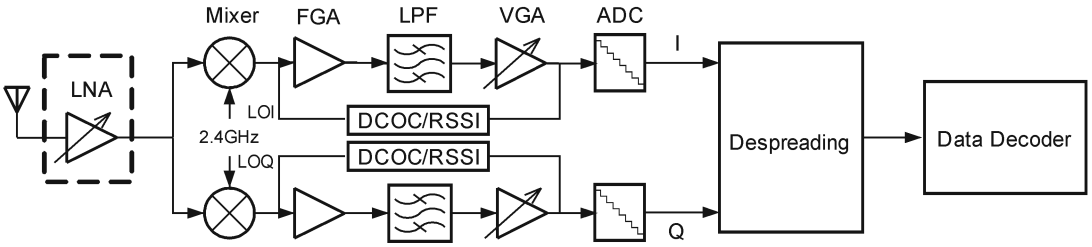

Fig. 1. Receiver architecture for ZigBee.

Table 1. LNA specifications.

Parameter	Value
Process	0.18 μm
Operating frequency	2.4–2.4835 GHz
Power gain S_{21}	$\geqslant$ 8 dB
Noise figure	$\leqslant$ 3 dB
1-dB compression point	$\geqslant$ –11 dBm
IIP_3	$\geqslant$ –1 dBm
Power dissipation	$\leqslant$ 3.6 mW

$$\begin{aligned} \mathrm{NF} &\leqslant \mathrm{Sensitivity} - \mathrm{KTB} - \mathrm{SNR_{dm}} \\ &= -85 - (-174 + 10\lg(2\times 10^6)) - 6 \\ &= 20\ \mathrm{dB}. \end{aligned} \tag{1}$$

It is suggested that the receiver input 1-dB compression point should be approximately 4 dB greater than the maximum input signal power level[6]. Assuming an extra 5 dB implementation margin, the 1-dB compression point for the receiver is –11 dBm under a maximum input signal power level of –20 dBm[1]. As the third-order intercept point (IIP_3) of a third-order system is approximately 10 dB greater than the 1-dB compression point[2], a minimum receiver IIP_3 of –1 dBm is suggested.

With regard to the power gain, there is a trade-off between the receiver noise figure and the linearity. Specifically, LNA gain cannot be increased without limit while meeting the front-end linearity requirement. The specifications of the LNA are summarized in Table 1.

3. Low power DGLNA design principle

3.1. CSLNA input match analysis

In the case of a low power CSLNA design, the gate-source capacitance of the transistor is usually very small，on the order of 100 fF, which is very sensitive to parasitics either from the packages or the ESD pads. As a result, it may greatly affect the input matching, the noise figure, and even the linearity of the LNA[5]. This behavior can be modeled as a capacitor C_p, parallel between the gate of the g_m-cell and the ground, as shown in Fig. 2(a). L_s is the inductor for source degeneration, and L_g is the inductor added in series to provide a resonance at the center frequency. C_p can be expressed as

$$C_P = C_{miller} + C_{ESD} + C_{pad} + C_{pkg}, \tag{2}$$

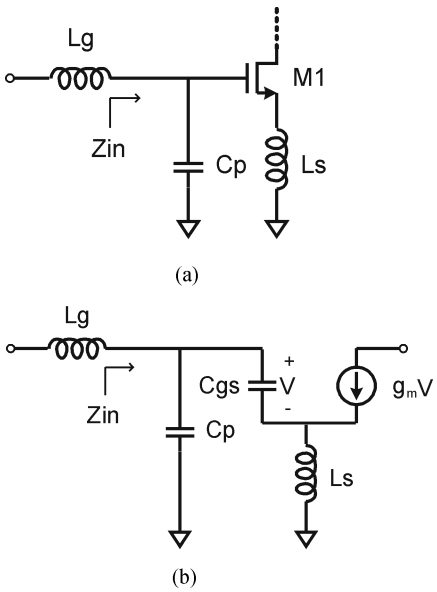

Fig. 2. (a) LNA topology used for analysis; (b) Small signal model used for analysis.

where C_{miller}, C_{ESD}, C_{pad}, and C_{pkg} stand for the capacitors resulting from the Miller effect, the ESD protecting transistors, and the package, respectively. Figure 2(b) shows the small signal model used to calculate the input impedance. Ideal inductors are used here to simplify the analysis. The real part of the input impedance including the effects of the parasitic capacitor can be expressed as

$$\mathrm{Re}(Z_{in}) = \frac{\omega_T L_s}{(1 + r(1 - C_{gs}\omega^2 L_s))^2 + (rC_{gs}\omega\omega_T L_s)^2}, \tag{3}$$

where $r = C_p/C_{gs}$ is called the parasitic ratio here. According to Eq. (3), the real part of the input impedance decreases as r increases under a given transistor M1 and bias condition. Figure 3 shows the dependence of $\mathrm{Re}(Z_{in})$ on r, which is divided into two regions in this paper. When $r \leqslant 2$, a $\mathrm{Re}(Z_{in})$ of 50 Ω can be easily satisfied. A careful choice of the ratio r or the source degenerated inductor L_s can make the impedance matching and noise matching occur at the same time, and the noise figure of the LNA is mainly limited by the noise figure of the device. Hence, this region is called noise figure limited region. Otherwise, when $r > 2$, both changes in r and L_s have little influence on $\mathrm{Re}(Z_{in})$, which implies a non-achievable match to 50 Ω under the assumption of single L_g matching. Since this is mainly caused by the small C_{gs} owing to the critical power consumption, this region is called the power limited region.

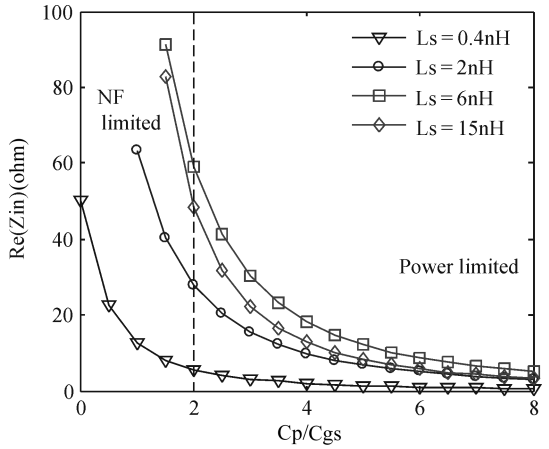

Fig. 3. Dependence of Re(Z_{in}) on r at C_{gs} = 100 fF, f = 2.45 GHz, and f_T = 20 GHz.

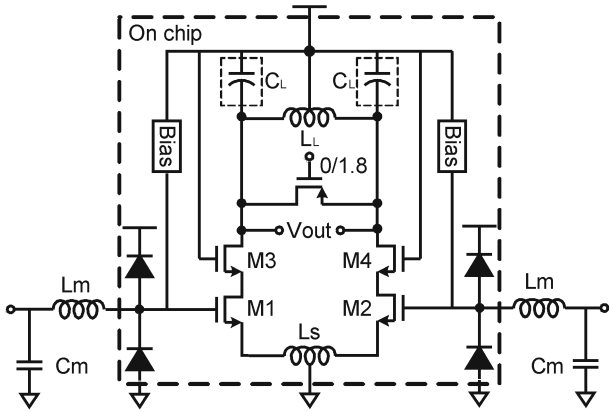

Fig. 4. Schematic of the proposed LNA.

From the analysis above, we can find that the parasitic capacitor brings a new trade-off between L_s and C_{gs} to the LNA design with the assumption of single L_g matching. When r is very small, that is to say, when C_p can be ignored or is comparable to C_{gs}, a small L_s can be chosen to achieve 50 Ω matching. However, in low power applications, a parasitic capacitor of about 500 fF, commonly including in the ESD pad and the package, can bring the LNA into a power limited region easily. This makes 50 Ω matching impossible with a single gate inductor L_g, just as analyzed. So an off chip matching network is needed as an assistant in the design.

3.2. CSLNA circuit design

The schematic of the LNA with dual gain is shown in Fig. 4. Fully differential architecture is used to restrain the common noise both from the power supply and the ground. Cascode topology is used to reduce the Miller effect, to improve the stability and the reverse isolation[8]. The source degenerated inductor L_s is put here to ease input impedance matching to the source[6]. The loaded LC tank provides a selective gain in the ZigBee receiving band. A voltage-controlled resistor, realized by the pMOS, allows reduction of the LNA gain in the presence of strong signals. ESD protection diodes are also used in the input and output ports. In order to make the design more robust, an off chip two element network set up by the inductor L_m and the capacitor C_m is used both for input matching and for noise figure minimization.

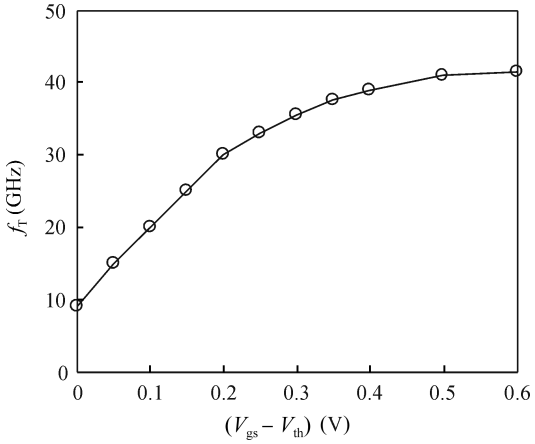

Fig. 5. Simulated f_T versus $V_{gs} - V_{th}$ at V_{ds} = 1 V, V_{th} = 0.48 V, W/L = 40/0.18.

Since the power gain and the noise figure are mainly decided by the input transistors M1 and M2, they are carefully sized. As the characteristic frequency f_T is usually selected to be at least 10 times higher than the working frequency, a f_T of about 30 GHz is first determined.

The unit-current gain frequency f_T of the MOS transistor can be approximated as

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{1}{2\pi}\frac{3}{2n}\frac{\mu}{L^2}(V_{gs} - V_{th}), \tag{4}$$

where n is the sub threshold gate coupling coefficient, which is 1.3 in SMIC technology, μ is the electron mobility, and V_{gs}–V_{th} is the gate–source overdrive voltage of M1. From Eq. (3), it is concluded that the designer can control f_T mainly via V_{gs} and the channel length L. As a minimum transistor length is always used for higher f_T, it depends only on the over drive voltage. Figure 5 illustrates the simulated result of the MOS device with W/L = 40/0.18 as a function of $V_{gs} - V_{th}$. So, an overdrive voltage of about 200 mV is selected to achieve a f_T of 30 GHz. Then W = 47 μm is almost determined according to the I–V curve of the MOS saturate region.

The transistor width of M1 is also evaluated by the technique of power-constrained noise optimization (PCNO)[3] by

$$W_{opt} \approx \left(\frac{2}{3}\omega_0 L C_{ox} R_s Q_{L,opt,PD}\right)^{-1}, \tag{5}$$

where $Q_{L,opt,PD}$ is the input quality factor of the input circuit. The transistor size calculated by Eq. (5) is much larger than the one determined by V_{gs}–V_{th}. That is to say, the W decided by V_{gs}–V_{th} implies a much larger $Q_{L,opt,PD}$ according to Eq. (5). However, from the contours of the constant noise figure relating to $Q_{L,opt,PD}$ and the power consumption in the PCNO technique[3], we can find that, under a certain power level, the larger the $Q_{L,opt,PD}$, the less it deteriorates the noise figure. In other words, transistor sizes smaller than the optimized one will cause a much lower increase on the noise figure of the amplifier. Hence, W/L = 40/0.18 is finally chosen with the consideration of higher linearity while not degrading the noise figure that much.

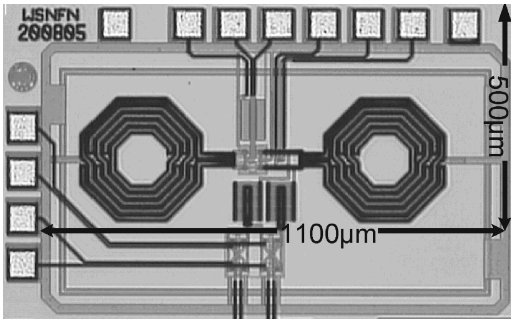

Fig. 6. Micrograph of LNA.

Cascode devices M3 and M4 have the same aspect ratio as the input pair. Inductors are implemented as a single differential spiral with the central tap tied to the power supply or ground, which make it immune to the parasitic inductance by the bonding wires. The size of L_s is chosen according to Eq. (3) under the assumption of C_p = 200 fF. As it has dropped into the power limited region, the off chip matching network is prepared for assistance. The inductor L_L is selected to maximize the gain, which resonates with the load capacitance C_L, including the capacitance of the cascode transistor M2, the input capacitance of the succeeded mixer, and the one owing to the ESD protection and the pad.

4. Measurement and discussion

An LNA circuit with ESD protection was fabricated in SMIC 0.18-μm RF/Mixed signal CMOS technology. Figure 6 shows a micrograph of the chip with an area of 1100 × 500 μm^2 (with pad). The measurement is performed with a chip-on-board (COB) package. When preparing for the circuit measurement, setting up the matching network is one of the most important tasks. Because the input impedance (Z_{in}) of the circuit on chip is usually more capacitive than the simulated one owing to either the ESD protection or input parasitics, L_m and C_m are employed to transform it into typical 50 Ω (as shown in Fig. 4). First, L_m is used to oscillate the imaginary part of the Z_{in}, making Z_{in} on the Smith chart go upwards along the resistance circle until it arrives at the unit conductance circle. Second, C_m is used to compensate the real part of Z_{in} to 50 Ω, making Z_{in} then go downwards along the unit conductance circle until it arrives at the desired 50 Ω.

However, the above scheme is only effective for the ideal case. Since the wave length in Rogers 4350 is only 7.3 cm at 2.45 GHz with a PCB thickness and a line width of 20 mil and 30 mil respectively, a signal trace with a length more than 10% of this will cause a transmission line effect[7]. In addition, the RF characteristic of the discrete components in the input signal path including the balun, the inductors, and the capacitors of the matching network will also cause a great change in the ideal matching scheme. Therefore, it should be carefully considered, especially for a higher frequency.

In order to evaluate these effects, getting off-chip two-element matching more quickly, the post simulation results of the LNA, the models of the off-chip devices and the traces on the PCB are all put into ADS for combined S parameter simulations. The traces on the PCB are modeled as micro-strip lines and all the discrete components are selected from Murata and TDK, whose components have complete model files for evaluation and simulation. Then, just after one try, both the input and output of the LNA is well matched to 50 Ω. The designed differential LNA draws 2 mA from a 1.8 V supply. The S parameter measurements performed on Agilent E5071B are shown in Figs. 7 and 8. The measured S_{11} and S_{22} are less than –10 dB in the whole ZigBee frequency band, and the reverse isolation is less than –15 dB. The LNA has a measured high gain of 8 dB and low gain of 1 dB. The noise figure in the high gain mode measured with E4440A is 2.3–3 dB in the expected band as shown in Fig. 9. The linearity performance are shown in Figs. 10~12. And the measured 1-dB compres-

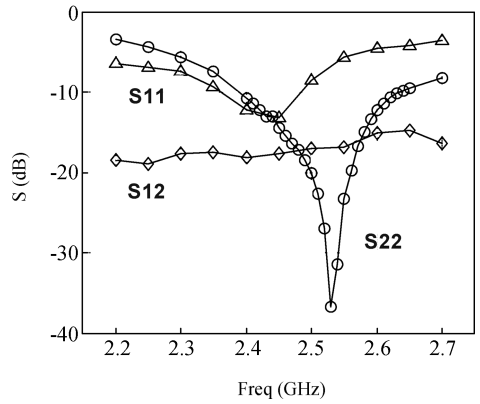

Fig. 7. Measured S_{11}, S_{12}, and S_{22} in high gain mode.

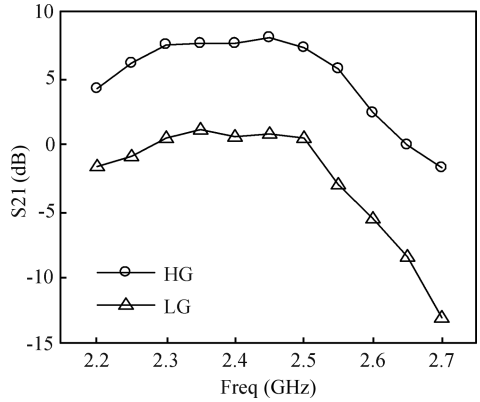

Fig. 8. Measured power gain in high gain (HG) and low gain (LG) modes.

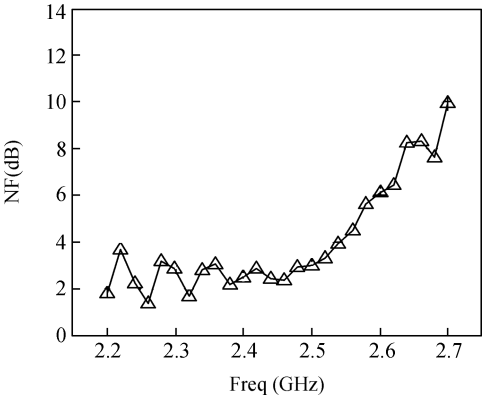

Fig. 9. Measured noise figure in HG mode.

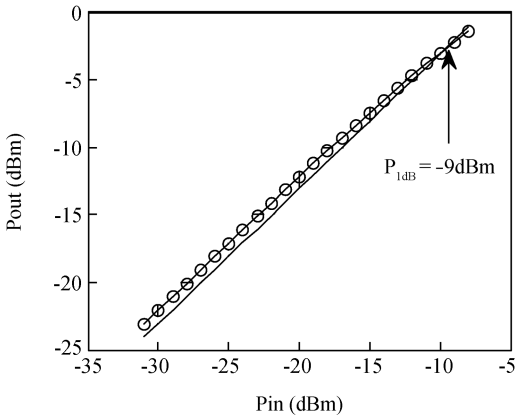

Fig. 10. Measured 1 dB compression point in HG mode.

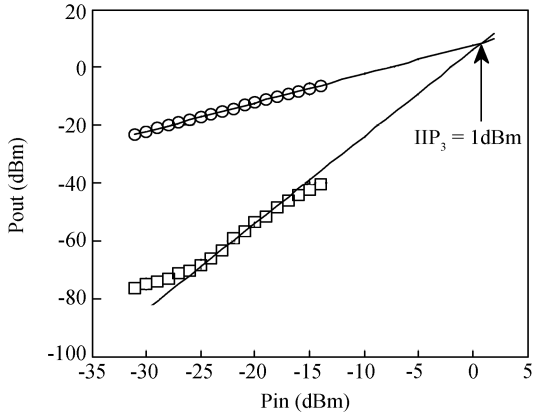

Fig. 11. Measured IIP_3 in HG mode.

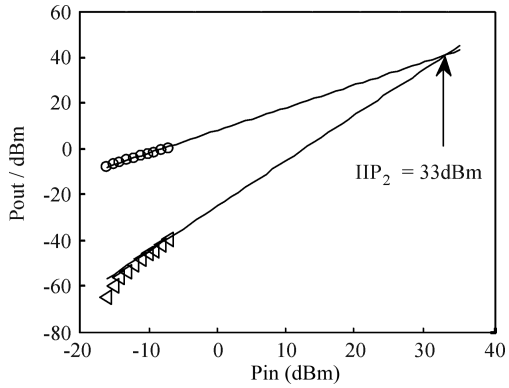

Fig. 12. Measured IIP_2 in HG mode.

sion point, IIP_3, and second-order intercept point (IIP_2) is –9, 1 and 33 dBm, respectively. Table 2 gives the measured results compared to recently published work.

5. Conclusion

In this paper, the effect of input parasitics on input matching of the inductive degenerated cascode LNA is analyzed in detail. It is shown that this effect becomes severe especially in the consideration of a low power design. Combined with the assistance of Spectre and ADS, the flow both for design and measurement becomes much more efficient. The measurement results show that it can fully satisfy the demands of the ZigBee/IEEE 802.15.4 receiver.

Table 2. Summary of measured results and comparison to results from the literature.

Reference	Ref. [9]	Ref. [10]	Ref. [11]	This work
Process (μm)	0.18	0.35	0.18	0.18
Frequency (GHz)	2.1	2.05	2.4	2.4
S_{21}(dB)	29.8	11	10.1	8
NF (dB)	4.5	5.3	2.9	2.3
IIP_3 (dBm)	–11.6	N/A	4	1
Power (mW)	1.1	26.4	11.7	3.6

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