A VCO sub-band selection circuit for fast PLL calibration

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Abstract: A novel voltage controlled oscillator (VCO) sub-band selection circuit to achieve fast phase locked loop (PLL) calibration is presented, which reduces the calibration time by measuring the period difference directly and accomplishing an efficient search for an optimum VCO sub-band. The sub-band selection circuit was implemented in a 0.18 μm CMOS logic process with a PLL using an 8 sub-band VCO. The measured calibration time is less than 3 μs in a VCO frequency range from 600 MHz to 2 GHz. The proposed circuit consumes 0.64 mA at most.

Key words: PLL; VCO; calibration
DOI: 10.1088/1674-4926/30/8/085010 **EEACC:** 1280

1. Introduction

A phase locked loop (PLL) often requires fast locking and a wide tuning range to cover the desired frequencies and to accommodate process, voltage, and temperature variations[1, 2]. As supply voltage scales down, the tuning gain of the voltage controlled oscillator (VCO) is increased, and large tuning gain degrades the phase noise and spur performance of a PLL[3]. A way to solve this problem is to use a VCO with multiple overlapping discrete frequency bands[4, 5]. However, this method requires an extra circuit to select a proper VCO sub-band, and the calibration time adds to the intrinsic PLL setting time. To achieve fast calibration, a novel VCO sub-band selection circuit is proposed in this paper.

2. Operating principle and circuit design

The proposed VCO sub-band selection circuit is applied in a PLL using the open-loop calibration method as shown in Fig. 1. This circuit measures the period difference between input signal (REF) and feedback signal (FB) by detecting their phase relationship. First, REF and FB are divided by 4. As illustrated in Fig. 1, eight phases whose frequency is 1/4 of the REF are generated, and a signal out of the phase selector is selected by the rising edge of FBc. The selected REFc has a phase lagging behind that of FBc by 45° to 90° to increase the comparison accuracy and prevent the following charge pump from working in the dead-zone region[5]. A calibration period includes period comparison and a reset process. This circuit works in the comparison state and the reset state alternately, and the calibration frequency is 1/2 the FBc frequency. If an N divider is applied in the PLL and the VCO output frequency is $f_{\rm VCO}$, the FBc frequency will be $f_{\rm FBc} = f_{\rm VCO}/(N \times 4) = f_{\rm VCO}/4N$ and the calibration frequency will be $f_{\rm VCO}/(N \times 4 \times 2) = f_{\rm VCO}/8N$. The calibration time decreases as the VCO output frequency increases.

Figure 2 shows the period comparator and edge detector circuits. Edge detectors which detect rising or falling edges of the inputs are reset when the first edge comparison finishes, and they maintain this state until the next comparison cycle. Therefore, period comparison is performed by examining only one pair of rising and falling edges. The period comparator produces UP and DN pulses to control the charge pump. Then, as depicted in Fig. 3(a), the period difference between input signals is converted into a voltage variation of $V_{\rm C}$, which can be expressed as

$$\Delta V_C = -T_1 \frac{I_{\rm CP}}{C} + T_2 \frac{I_{\rm CP}}{C} = -(T_1 - T_2) \frac{I_{\rm CP}}{C} = -\Delta T \frac{I_{\rm CP}}{C}, \quad (1)$$

where $I_{\rm CP}$ is the charge/discharge current of charge pump, T_1 and T_2 are the time difference between the rising and falling edge of input signals, and ΔT is the period difference. When the frequency different between REFc and FBc is as large as shown in Fig. 3(b), $\Delta V_{\rm C}$ cannot be expressed by Eq. (1). In this situation the period comparison result is still correct, because the rising edge of REFc lags behind that of FBc by 45 ° to 90 °.

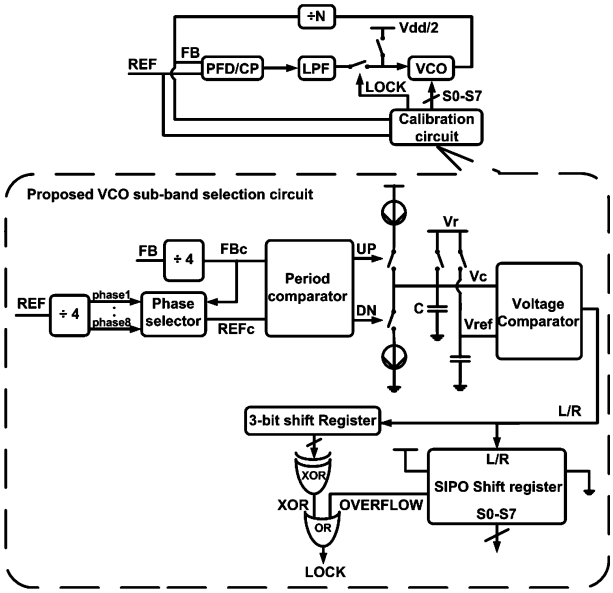

Fig. 1. Block diagram of PLL with VCO sub-band selection circuit.

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Received 8 January 2009, revised manuscript received 17 March 2009

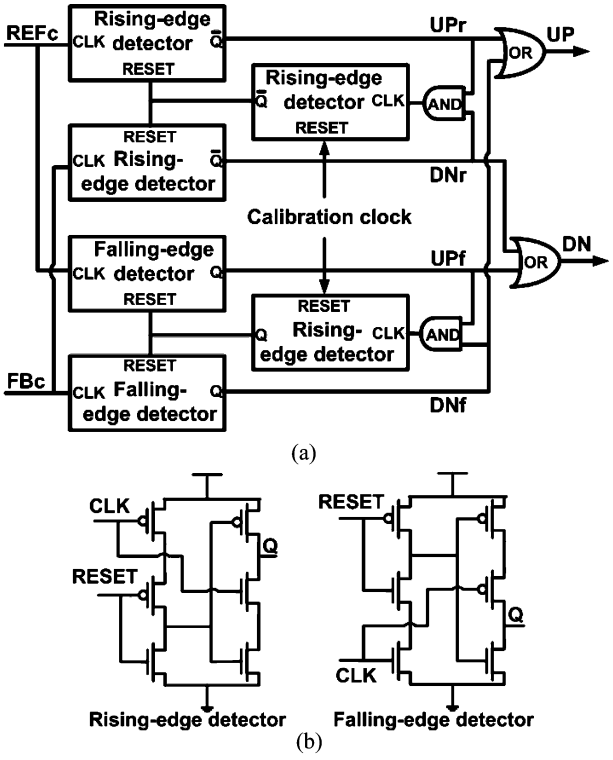

Fig. 2. (a) Period comparator; (b) Edge detectors.

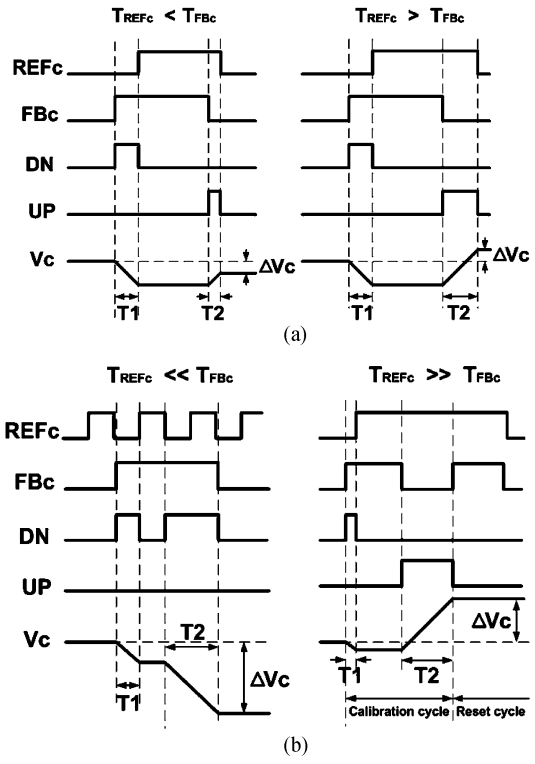

Fig. 3. Operation waveform.

The initial voltage of V_C and V_{ref} is set to V_r. If the frequency of FBc is less than that of REFc, V_C will be lower than V_{ref}, resulting in a low output of the voltage comparator. Otherwise its output is high.

The maximum charge or discharge time $\Delta T_{(max)}$ happens when the VCO works at the lowest frequency $f_{VCO(min)}$ and FBc frequency reaches its minimum value. Since $f_{FBc} = f_{VCO}/4N$, $\Delta T_{(max)} = 4N/f_{VCO(min)}$. Thus the maximum voltage variation on capacitor C is $I_{CP}\Delta T_{(max)}/C$. To reduce the mismatch between the charge and discharge current of the charge pump, the voltage variation should be limited to a value $\Delta V_{C(max)}$. The charge pump current and capacitor C are designed according to the following limitation:

$$\frac{I_{CP}\Delta T_{(max)}}{C} = \frac{4NI_{CP}}{Cf_{VCO(min)}} < \Delta V_{C(max)}. \quad (2)$$

The period comparison result is influenced by the current mismatch in charge pump and other nonideal effects. To make sure that the target frequency is covered by the selected VCO subband, enough frequency overlap is designed between neighboring VCO sub-bands. S0–S7 are the outputs of the serial-in parallel-out shift register in Fig. 1, and determine at which sub-band the VCO works. This register shifts according to the voltage comparator output L/R, and continues shifting to the left or the right until the current VCO sub-band can cover the input frequency. Therefore, L/R becoming different from the previous comparison cycle indicates that the VCO has already been set to a proper sub-band. The L/R signal is stored in a register after calibration starts. Since the initial value of L/R may cause some wrong operations, the L/R signal is stored in a register for three comparison cycles. From the above analysis, when XOR goes to high, the calibration should be finished. The OVERFLOW signal goes to high at the condition that the input frequency is covered by the lowest or highest VCO sub-band, and the LOCK signal can be set by either XOR or OVERFLOW to enable PLL closed-loop locking.

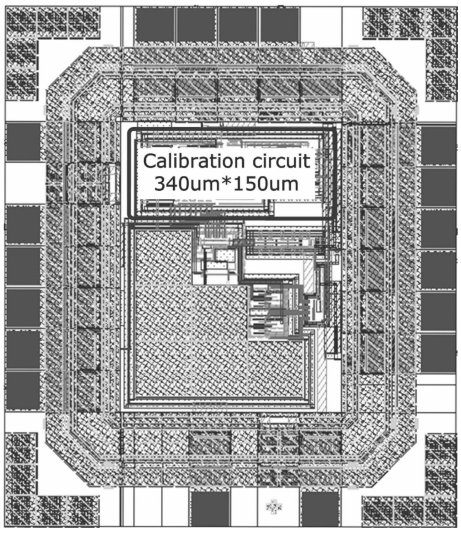

Fig. 4. Circuit layout.

3. Experimental results

The circuit has been implemented with a PLL in a 0.18 μm CMOS logic process, and Figure 4 is the layout. Measured calibration processes are shown in Fig. 5. Initially, the 8 subband VCO works at the middle sub-band (S0–S3 are high and S4–S7 are low) and the LOCK signal is set to high. The VCO output is divided by 32. The REF frequency is 18.75, 43.75 and 62.5 MHz. So the VCO target frequencies f_{target} are 600

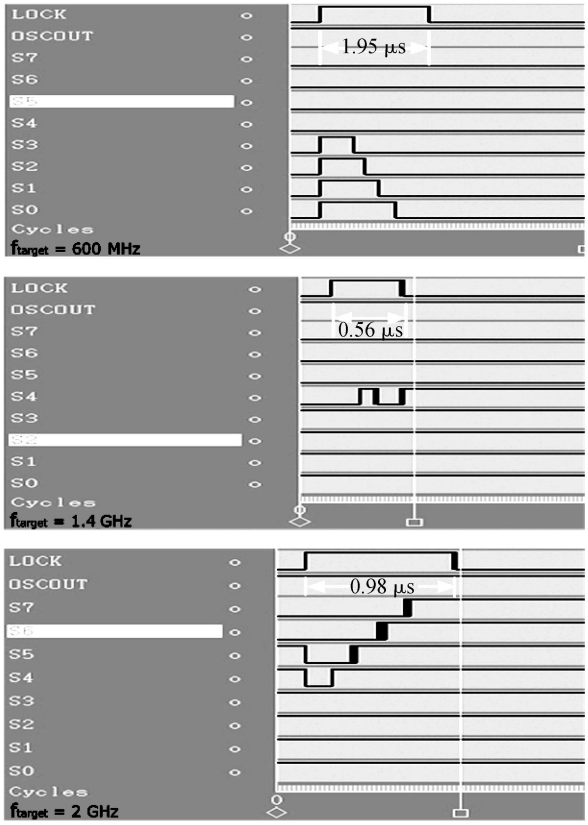

Fig. 5. Calibration processes.

MHz, 1.4 GHz and 2 GHz respectively, and these target frequencies are covered by the lowest, the middle and the highest frequency sub-bands. As illustrated in Fig. 5, when the VCO operates at proper sub-band the LOCK signal goes to low. The measured calibration times are 1.95, 0.56, and 0.98 μs. The maximum calibration time can be obtained when the VCO is calibrated from the lowest sub-band to the highest sub-band. The measured result is 3 μs with REF frequency stepping from 18.75 to 62.5 MHz. Other measured results are given in Table 1. As mentioned above, the calibration time of our design is proportional to the VCO output period. Thus if the proposed VCO sub-band selection circuit is applied in a PLL with higher output frequency, the calibration time will be further reduced.

Table 1. Measured results.

Parameter	Value
Process	0.18 μm CMOS
Supply voltage	1.8 V
Occupied area	340×150 μm^2
Circuit dissipation	0.64 mA
VCO tuning range	600 MHz–2 GHz
Amount of VCO sub-band	8
Calibration time	< 3 μs

4. Summary

A novel VCO sub-band selection circuit is described and analyzed in this paper. The calibration time is reduced by using a period comparator, to compare the frequency difference directly, and a logic control circuit, to search for the proper VCO sub-band efficiently. The experimental results demonstrate that the proposed VCO sub-band selection circuit can achieve fast PLL calibration.

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