A 2.8 ppm/℃ high PSRR BiCMOS bandgap voltage reference

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Abstract: A high-order curvature-compensated and high power-supply rejection ratio (PSRR) BiCMOS bandgap reference is presented. The circuit utilizes positive temperature characteristics of the saturation current I_{SS} and forward current gain β of the bipolar transistors to realize a low temperature coefficient (TC) as well as filter capacitors and level-shift structures to improve the PSRR. Implemented in 0.6 μm BCD process, the proposed voltage reference consumes a supply current of 28 μA at 3.6 V. A temperature coefficient of 2.8 ppm/°C, PSRR of more than 80 dB at low frequencies and a line regulation of 50 ppm/V from 3.6 to 5.5 V are easily achieved, which make it widely applicable in portable equipment.

Key words: saturation current; current gain; curvature compensation; level shift; filter capacitors
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1. Introduction

Precision voltage references play an important role in many applications such as data converters and power management. Insensitivity to temperature and power supply noise, as well as being able to operate at low voltage[1–3] is the key for high performance design. In order to reduce wide variation in temperature range, many high-order temperature compensation techniques have been developed, such as quadratic temperature compensation, exponential temperature compensation, piecewise-linear curvature correction, and temperature-dependent resistor ratio compensation[4–7]. The basic idea is to implement advanced mathematical functions to counteract the high-order temperature coefficients of the PN junction. However, these methods require precision matching of current mirrors, otherwise they will introduce an error voltage at the reference output. So the precision is controlled by process and layout. Referring to PSRR, the main techniques use cascodes or preregulation of the input voltage[8], which are tradeoffs with low voltage and low power design.

To consider minimizing the size and power as well as reducing the effects of process and layout, a new low TC and high PSRR bandgap reference is presented in this paper. The proposed circuit amplifies the saturation current I_{SS} to realize temperature compensation and makes use of filter capacitors and level-shift structures to greatly improve PSRR.

The paper starts with a brief analysis of the temperature dependence of the base–emitter voltage and then introduces methods to improve the TC and PSRR. Finally, measurement results as well as performance comparison with a conventional bandgap reference are presented.

2. Temperature dependence of the base–emitter voltage

It is well known that BJTs are commonly used to implement the bandgap voltage reference. The base–emitter voltage can be expressed by[9]

$$V_{BE} = V_G(T_o) + \frac{T}{T_o}[V_{BE}(T_o) - V_G(T_o)] - (\eta - m)\frac{kT}{q}\ln\frac{T}{T_o}, \quad (1)$$

where V_G is the bandgap voltage of silicon extrapolated at 0 K, k is Boltzmann's constant, η is a temperature constant depending on the technology, m is the order of the temperature dependence of the collector current, and T_o is the reference temperature.

From Eq. (1), the term $T\ln T$ indicates the nonlinear temperature-dependence factor of V_{BE}. First-order temperature compensation involves cancellation of the T term while high-order temperature compensation involves cancellation of high-order T terms.

3. Proposed BiCMOS bandgap reference

In order to eliminate effects of the input offset voltage of an op amp on the TC of the reference and meet the goals of low power supply voltage and low power dissipation, it is desirable to use a simple circuit configuration avoiding an operational amplifier.

3.1. Curvature compensation technique

There are some problems with traditional methods. For example, they need complex circuits, have large power consumption, and occupy significant chip area for curvature compensation.

The proposed idea is illustrated Fig. 1, where a compensation current I_{comp} is injected to node A and the reference voltage can be given by

$$V_{REF} = V_{BE1} + \frac{2(R_0 + R_1)\ln N}{R_2}V_T + I_{comp}R_0, \quad (2)$$

where N is the emitter-area ratio of Q1 and Q2, and V_T is the thermal voltage. The resistor ratio $(R_0 + R_1)/R_2$ is temperature

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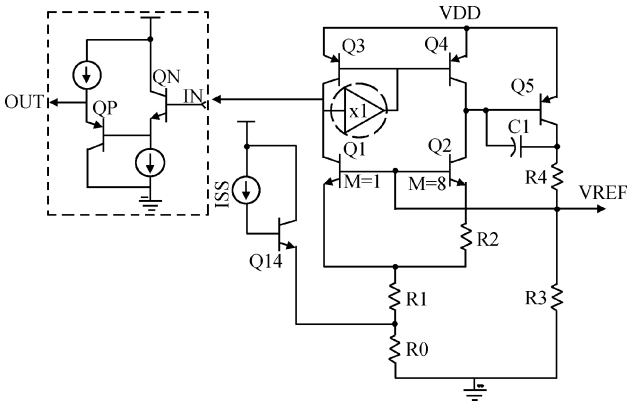

Fig. 1. Proposed compensation techniques.

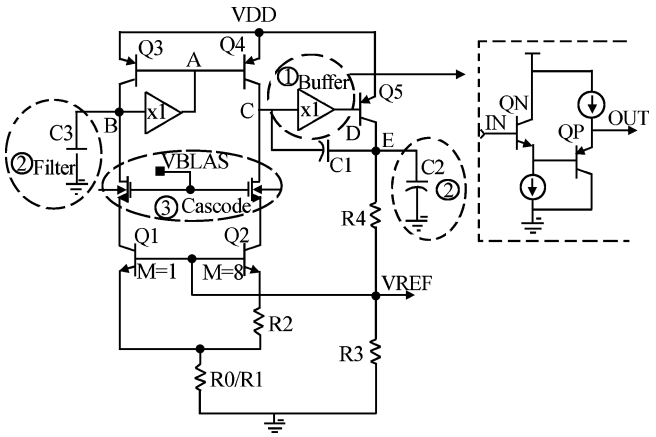

Fig. 2. Enhancement for increasing the PSRR.

independent because they are implemented by the same material.

The theory of $I_{\rm comp}$ is to amplify the small saturation current $I_{\rm SS}$ of a PN junction, which is formed by the base–collector junction. $I_{\rm SS}$ is related to the device structure by[10]

$$I_{\rm SS} = \frac{qA\overline{D}_{\rm n}n_{\rm i}^2}{Q_{\rm B}} = Bn_{\rm i}^2\overline{D}_{\rm n} = B^{'}n_{\rm i}^2T\overline{u}_{\rm n}, \tag{3}$$

where $n_{\rm i}$ is the intrinsic minority-carrier concentration, $Q_{\rm B}$ is the total base doping per unit area, $\overline{u}_{\rm n}$ is the average electron mobility, and A is the PN junction area. Here, the constants B and $B^{'}$ involve only temperature-independent quantities. $\overline{u}_{\rm n}$ and $\overline{D}_{\rm n}$ meet the Einstein relation $u_{\rm n} = (q/kT)D_{\rm n}$. The quantities in Eq. (3) that are temperature dependent are given by[9, 11]

$$\overline{u}_{\rm n} = CT^{-n}, \tag{4}$$

$$n_{\rm i}^2 = DT^3\exp\left(-\frac{V_{\rm G0}}{V_{\rm T}}\right), \tag{5}$$

where n is dependent on the doping level in the base and $V_{\rm G0}$ is the bandgap voltage of silicon extrapolated to 0 K. Here C and D are temperature-independent quantities. Combining Eqs. (3), (4) and (5) yields

$$I_{\rm SS}(T) = B^{'}CDT^{4-n}\exp\left(-\frac{V_{\rm G0}}{V_{\rm T}}\right) = ET^{\gamma}\exp\left(-\frac{V_{\rm G0}}{V_{\rm T}}\right), \tag{6}$$

where E is another temperature-independent constant and $\gamma = 4 - n$.

The temperature dependence of $\beta(T)$ is an exponential function of temperature, and an inverse exponential function of the emitter doping level. It can be expressed as[6]

$$\beta(T) = \beta_\infty\exp\left(-\frac{\Delta E_{\rm G}}{kT}\right). \tag{7}$$

There is a strong correlation between the distribution of β_∞ and $\Delta E_{\rm G}$. $\Delta E_{\rm G}$ is the bandgap narrowing factor of the emitter, proportional to the emitter doping level. As the device size scales down and the doping level increases, $\Delta E_{\rm G}$ tends to increase. Combining Eqs. (6) and (7) yields

$$I_{\rm comp} \approx \beta(T)I_{\rm SS}(T) = E\beta_\infty T^{\gamma}\exp\left(-\frac{qV_{\rm G0} + \Delta E_{\rm G}}{kT}\right). \tag{8}$$

Setting $\lambda = (qV_{\rm G0} + \Delta E_{\rm G})/k$ and using $e^x \approx 1 + x + x^2/2 + x^3/3$, $I_{\rm comp}$ can be expressed as

$$I_{\rm comp} \approx E\beta_\infty\left(T^{\gamma} - \lambda T^{\gamma-1} + \frac{\lambda^2T^{\gamma-2}}{2} - \frac{\lambda^3T^{\gamma-3}}{6}\right). \tag{9}$$

As we see from Eqs. (8) and (9), there are some differences from the traditional methods. First, the proposed method has a somewhat complicated function of temperature since the added exponential term has many higher-order terms in itself. Second, the compensation is affected by both η and $\Delta E_{\rm G}$ whereas the temperature characteristic of the traditional ones is constant over the variation of $\Delta E_{\rm G}$. Combining Eqs. (2), (8) and (9) yields

$$\begin{aligned} V_{\rm REF} &= V_{\rm BE1} + \frac{2(R_0 + R_1)\ln N}{R_2}V_{\rm T} \\ &\quad + E\beta_\infty R_0T^{\gamma}\exp\left(-\frac{qV_{\rm G0} + \Delta E_{\rm G}}{kT}\right) \\ &\approx V_{\rm BE1} + K_1T + K_2\left(T^{\gamma} - \lambda T^{\gamma-1} + \frac{\lambda^2T^{\gamma-2}}{2} - \frac{\lambda^3T^{\gamma-3}}{6}\right), \end{aligned} \tag{10}$$

where the TC of R_0 has been neglected. Here K_1 and K_2 are constants. From previous studies, the the TC of the reference can be optimized by R_0, R_1 and A.

Precision voltage references are generally degraded by device mismatches and process variation, so there are two points to consider. The first is current mirror matching. If we use only a pnp current mirror consisting of Q3 and Q4, the systematic gain error ε can be given by

$$\varepsilon \approx \frac{V_{\rm CE4} - V_{\rm CE3}}{V_{\rm A}} + \frac{1 + (I_{\rm S4}/I_{\rm S3})}{\beta_{\rm F}}, \tag{11}$$

where $V_{\rm A}$ is Early voltage. The first term in Eq. (11) stems from finite output resistance and the second term from finite $\beta_{\rm F}$. Therefore a buffer with CC–CC configuration has been used to cancel the effects of base currents and the second input stage has also been chosen as a pnp transistor to ensure $V_{\rm CE3} = V_{\rm CE4}$ as shown in Fig. 1. After optimization, the error is nearly zero.

Another important consideration is temperature trimming which involves two steps: one for linear temperature trimming and the other for high-order temperature trimming. The measurement starts by using parameters obtained from the simulation, then R_1 is trimmed until the TC is a minimum for

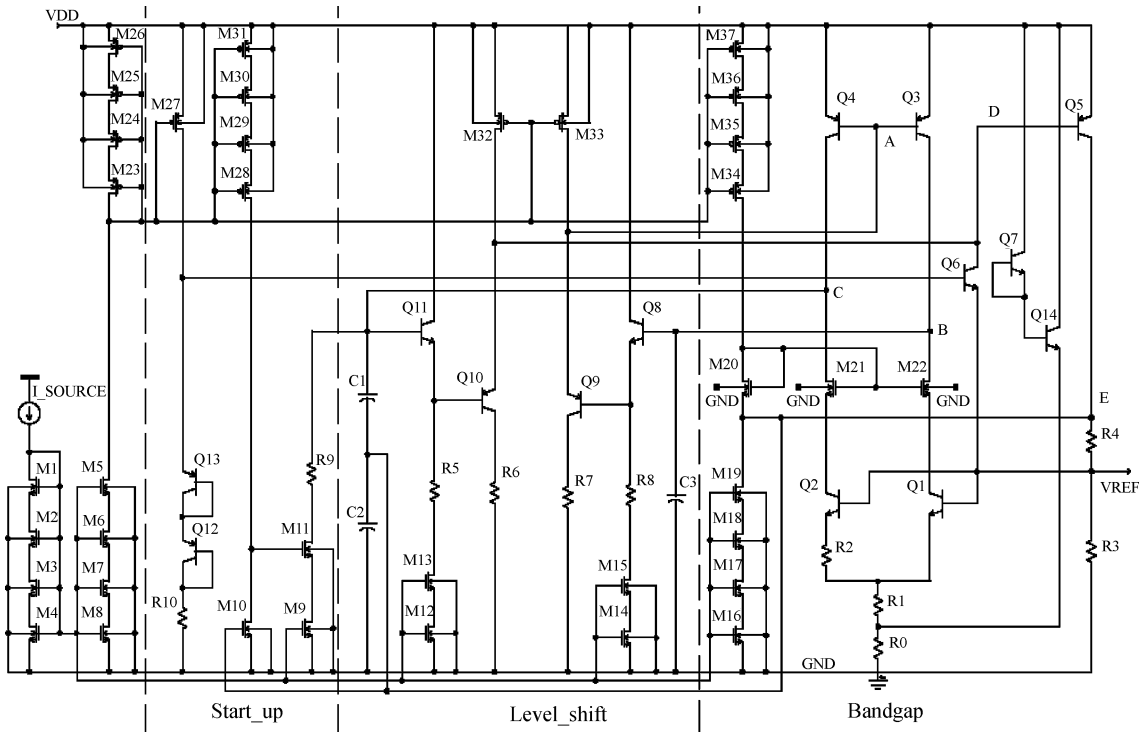

Fig. 3. Complete schematic of the proposed bandgap voltage reference.

particular R_0 and A. R_0 is then changed until a lower TC is obtained. The procedure is repeated until the minimum TC is achieved[12]. In the trimming procedure, two (minimum and maximum) temperature measurements are sufficient for linear trimming, while four temperature measurements evenly distributed in the considered range of temperature are sufficient for nonlinear trimming.

3.2. High PSRR performance

The PSRR of the reference in Fig. 1 is usually about 40 dB because there is no op amp in the feedback loop to contribute a high gain[13]. The main ideas to improve the PSRR are illustrated in Fig. 2.

(1) Increase the loop gain by means of a buffer. The CC–CC configuration with high current gain and input resistance is inserted between nodes C and D. Assuming $r_\pi \ll r_o$, after adding the buffer, the loop gain T_2 in low frequencies can be expressed as

$$\frac{T_2}{T_1} \approx \frac{r_{04}}{r_{\pi 5}}, \tag{12}$$

where T_1 is the loop gain of Fig. 1. The increasing impedance of node C results in a high loop gain compared to the initial one.

(2) Use capacitors to filter some noise. As we see in Fig. 1, there are mainly two paths where the supply noise can transfer to the output. One is from C_{BE3} and C_{BC1} to the output and the other is from C_{BE5} and C_1 to the output, so the filter capacitors can be added on nodes B and E in Fig. 2.

(3) Increase the effective impedance from sensitive nodes (the reference voltage) to the input supply voltage. For example, we use the cascode structure to isolate the noise of the supply voltage in Fig. 2. The MOS transistors are long-channel and large W/L devices to acquire a small overdrive and large output resistance.

4. Circuit realization

Figure 3 shows the complete circuitry of this BiCMOS bandgap voltage reference. In the design, high-R poly-silicon resistors are chosen to conserve area. Q7 and Q14 compose the compensation circuit, where the base and emitter of Q7 are connected together to produce I_{SS}. The bias circuit for M20 adopts self-cascode mirrors to meet the low supply voltage demand[14].

There are three poles to be considered for stability, because the filter capacitors are in the feedback loop. The dominant pole is $P_C \approx 1/g_{m5}(R_3+R_4)r_{o4}C_1$. The nondominant poles are $P_B \approx g_{m3}/C_3$ and $P_E \approx g_{m5}/C_2$, contributed by the filter capacitors. Although P_B and P_E restrict the bandwidth of the loop, this has a small effect on the reference because it usually works at low frequency.

5. Experimental results and discussion

The proposed circuit shown in Fig. 3 has been implemented in 0.6 μm BCD technology. The threshold voltage is about $V_{thn} \approx |V_{thp}| \approx 0.85$ V. The layout is shown in Fig. 4 where the active area of the circuit is $200 \times 234\ \mu m^2$. The simulation results are tabulated and compared to other references reported in Table 1.

The circuit is simulated in the temperature range –25 to 125 °C using a supply voltage of 3.6 V and different emitter areas of Q7 as shown in Fig. 5. When the temperature is higher than 100 °C, the compensation current I_{Q14} increases along with the increasing emitter area. The optimized value is three times larger than the smallest size. The temperature coefficient of 2.5 ppm/°C is easily obtained, which has some superiority compared to traditional ones.

The PSRR of the reference is shown in Fig. 6. The mea-

Table 1. Summary of the performance of the proposed voltage reference.

Parameter	Proposed	Rincon-Mora[2]	Lee[3]	Leung[4]	Song[1]
Technology	UMC 0.6-μm BCD	BiCMOS	BiCMOS	CMOS	CMOS
Threshold voltage (V)	$V_{thn} \approx \lvert V_{thp}\rvert \approx 0.85$	$V_t \approx 0.9$	—	$V_t \approx 0.9$	—
Supply voltage (V)	3.6 4 5.5	1.1 (min)	5	2 (min)	±5
Supply current (μA)	30 (max)	15 (min)	74	23 (max)	1200
Reference voltage (mV)	1255 ± 0.25	595	1264	1142	1192
Tempco (ppm/°C)	2.56 2.55 2.67	6.5	8.9	5.3	25.6
Line regulation	50 ppm /V	120 ppm/V	—	±1.43 mV/V	—
PSRR (dB) @ 27 °C	–85 @10 Hz, –81 @1 kHz, –46 @100 kHz	—	73	–20 @1 kHz	50

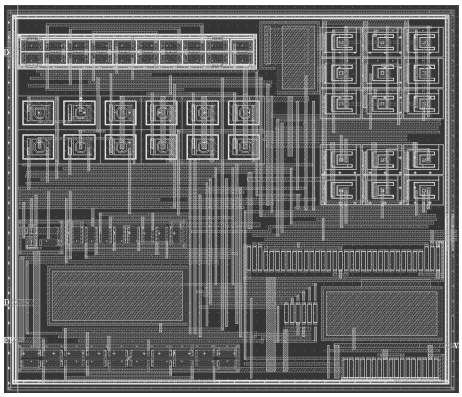

Fig. 4. Layout of the proposed bandgap voltage reference.

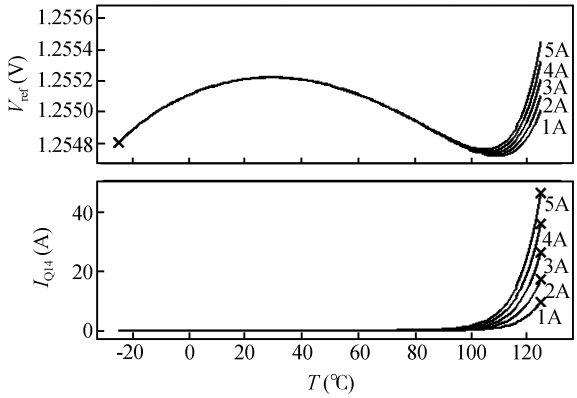

Fig. 5. Simulated TC of the proposed reference.

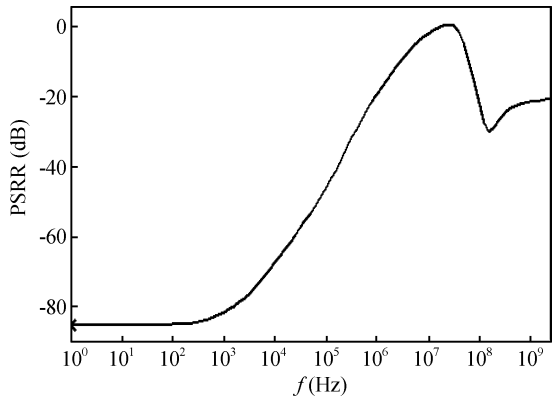

Fig. 6. Simulated PSRR of the proposed reference.

surement conditions are with a 3.6 V supply voltage and at room temperature. A larger than 80 dB PSRR has been achieved up to 1 kHz; when the frequency is at 100 kHz, and the PSRR is still larger than 45 dB. This will ensure a stable

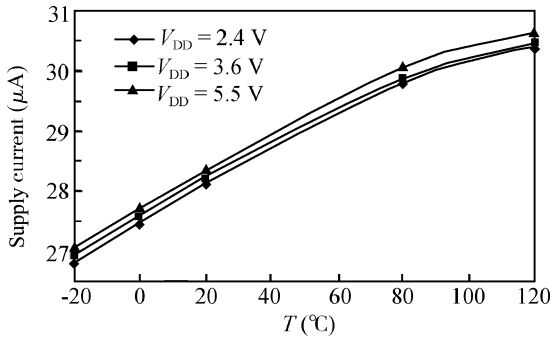

Fig. 7. Measured quiescent power.

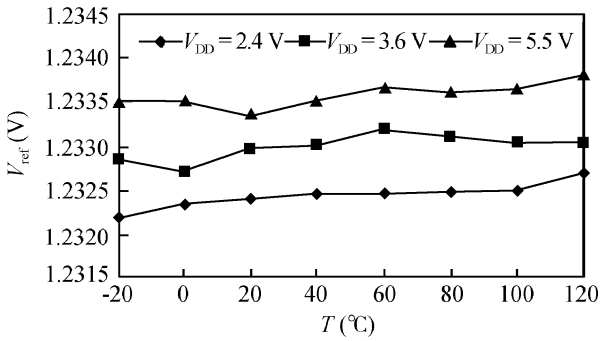

Fig. 8. Measured temperature dependence.

reference system against power supply ripple.

The measured supply current under different supply voltages and temperatures is shown in Fig. 7. The supply current under room temperature is nearly 28 μA. Greater reduction can be achieved by increasing the total resistance, but the tradeoffs are larger chip area and more coupling noise from the resistors.

Figure 8 shows the measured temperature dependence with supply voltages of 2.4, 3.6, and 5.5 V are 3.1, 2.8, and 2.6 ppm/°C, respectively. The measured mean value of the reference voltage is 1.2328 V, which is close to the simulated result of 1.255 V. The difference is mainly due to the bipolar transistor model provided by the foundry. It should be noted that there is only a small change on the temperature coefficients for the change of supply voltage from 2.4 to 5.5 V. This is due to the well-matched current branches and advanced compensation technology.

The measured supply dependence at 0, 27, and 100 °C is shown in Fig. 9. The line regulation is less than 0.3 mV/V in the range 0–100 °C. Further improvement can be realized by substituting the current mirror with degeneration for Q3 and Q4; however, this is a tradeoff for low supply voltage.

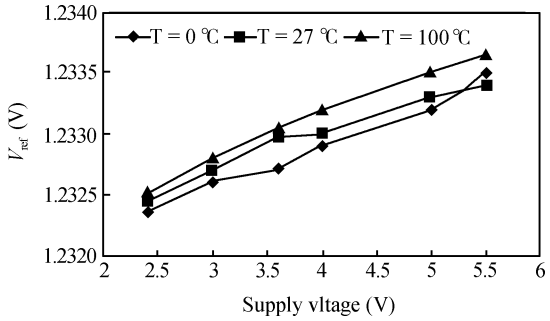

Fig. 9. Measured supply voltage dependence.

6. Conclusion

A 28 μA 2.8 ppm/°C voltage reference with high PSRR has been proposed. The compensation circuit is composed of only two npn transistors, the quiescent current of which is nearly zero at room temperature. This meets the requirement of minimizing the circuit area and power. At the same time, the technologies to improve PSRR and loop stability analysis have also been described. The proposed model is a good choice for small-area, low-power, high-precision and on-chip BiCMOS bandgap references.

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