Novel mixed-voltage I/O buffer with thin-oxide CMOS transistors

Yu Bo(俞波), Wang Yuan(王源)†, Jia Song(贾嵩), and Zhang Ganggang(张钢刚)

(Key Laboratory of Microelectronic Devices and Circuits, Institute of Microelectronics, Peking University, Beijing 100871, China)

Abstract: This paper presents a novel mixed-voltage I/O buffer without an extra dual-oxide CMOS process. This mixed-voltage I/O buffer with a simplified circuit scheme can overcome the problems of leakage current and gate-oxide reliability that the conventional CMOS I/O buffer has. The design is realized in a 0.13-μm CMOS process and the simulation results show a good performance increased by ~34% with respect to the product of power consumption and speed.

Key words: mixed-voltage I/O buffer; multi-power domain; thin-oxide; CMOS
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1. Introduction

The MOS transistor dimension and gate-oxide thickness have been scaled down to improve the circuit speed and the performance in an advanced CMOS process. For the requirements of low power and gate-oxide reliability, the core circuit voltage has also been scaled down, such as to 1.2 V, in a 0.13-μm CMOS process. However, the peripheral components or other ICs in an electronic system still operate at a higher voltage level, such as 2.5, 3.3, or 5 V. Hence, for a system to have a perfect performance, we need to solve the multi-power domain issue through the mixed-voltage I/O interface. The traditional I/O buffer is not suitable anymore, because it may cause problems of reliability, including the gate-oxide reliability, the hot-carrier degradation, and the undesirable leakage current paths.

The traditional I/O buffer is shown in Fig. 1, where the core power-supply voltage (V_{DD}) is 1.2 V. Obviously, when the I/O buffer is in the tri-state receive mode, where V_{DD} is 1.2 V, we can see clearly that this circuit has several main problems when the input signal at the PAD is 2.5 V. First of all, the gate terminal of the pull-up PMOS device MP0 is 1.2 V, so that the transistor MP0 was turned on and resulted in an undesirable leakage current path from the I/O PAD to the V_{DD}. Secondly, the parasitic drain-to-well PN-junction diode in the pull-up PMOS MP0 device was forward biased, and it also results in an undesirable leakage current path. Thirdly, the drain voltage of 2.5 V of the pull-down NMOS device MN0 is larger than the normal operation voltage, i.e., 1.2 V. Therefore, since the gate voltage is 0 V, the drain–gate voltage was higher than the normal operation voltage which induces hot-carrier degradation. In addition, the gate voltage of 2.5 V exceeds the normal operation voltage of 1.2 V in the inverter INV, causing serious gate-oxide reliability problems.

In order to overcome these problems, several techniques have been reported[1−3]. A dual-oxide (thin- and thick-oxide thickness) process has been developed to avoid the gate-oxide reliability problem[4]. A gate-tracking circuit, a stacked MOS structure, and a dynamic n-well bias circuit have also been reported to receive a high-voltage input signals without gate-oxide reliability issues.

In this paper, a novel mixed-voltage I/O buffer without extra dual-oxide CMOS process is proposed. Because it has the advantages of using the transmission gate (TG) as the dynamic switch and of a control circuit, this new mixed-voltage I/O buffer can avoid undesired damage caused by high voltages. This new mixed-voltage I/O buffer with a simplified circuit scheme can overcome the problems of leakage current and gate-oxide reliability, so that future layout designs can be easier and productivity can be increased.

2. Novel mixed-voltage I/O buffer

As shown in Fig. 2, a novel mixed-voltage I/O buffer with thin-oxide CMOS transistors is presented in this work. It was composed by the CMOS TG, which is formed of transistors MP1 and MN1, and the TG isolates the I/O PAD and driving component, which is formed by the pull-up PMOS device MP1 and the pull-down NMOS device MN1. In addition, the threshold voltage $|V_t|$ is ~0.3 V.

When the control signal OE is 1.2 V (logic "1"), the mixed-voltage I/O buffer is in the transmit mode. A control component composed of MP2, MN2, and MN3 turns the CMOS TG on. The output signal at the I/O PAD is almost less

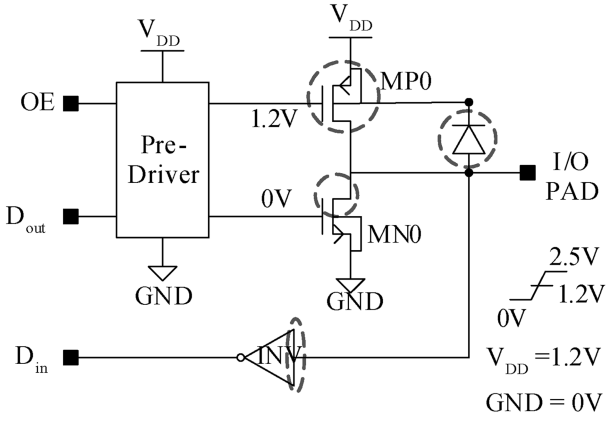

Fig. 1. Traditional I/O buffer.

† Corresponding author. Email: wangyuan@pku.edu.cn
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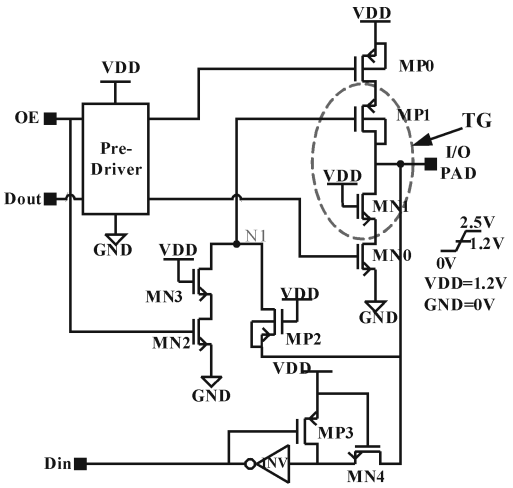

Fig. 2. Novel proposed mixed-voltage I/O buffer.

than 1.2 V, so MP2 is always kept off. Because the control signal OE is at a logic "1", the transistor MN2 is kept in the on-state. So, the GND signal transfers the source voltage of the transistor MN3 through the transistor MN2. Since the gate terminal of MN3 always connects with the V_{DD}, it will discharge the gate voltage of the transistor MP1 to 0 V. So, MP1 will not affect the normal work of MP0. The input signal Dout can transfer to the I/O PAD without any negative effect.

When the control signal OE is 0 V, the mixed-voltage I/O buffer works in the tri-state receive mode. When the input signal at the I/O PAD is 2.5 V and if the gate terminal of transistor MP2 is connected to V_{DD}, the gate terminal of MP1 is pulled up to 2.5 V. Hence, it transistor MP1 is kept off to avoid the undesirable leakage current path. For MP1 and MP2, the body terminal connects with the I/O PAD and the n-well is biased dynamically.

The proposed novel I/O buffer can mitigate the issue, as shown in Fig. 1, which increases the gate-oxide reliability in the tri-state receive mode. Hence, it can serve as an I/O buffer interface. The I/O buffer is formed by the thin-oxide device only, has a simpler circuit configuration, and a more convenient layout design. It also does not have a floating n-well.

3. Simulation results

In order to present a better description for the novel I/O buffer, we can simulate it like other typical circuit configurations were simulated[5, 6]. For the mixed-voltage I/O buffers, their output loadings are very large, which contain the I/O PAD, the bonding wire, the package pin, the PCB trace, etc. To complete the comparison, these mixed-voltage I/O buffers are simulated in a 0.13-μm process to compare their speed and power consumption performances under the condition of the same output loading, here 20 pF[6]. The reference circuits 1 and 2 are shown in Figs. 3 and 4, respectively.

The HSPICE simulation waveforms of the proposed mixed-voltage I/O buffer with a 20 pF load and a 50 MHz I/O signal[6] are shown in Figs. 5 and 6. The comparison of the power consumption, the speed, and the configuration of I/O buffer is shown in Table 1. In Table 1, the average power consumption is mainly referred to the dynamic power, and the

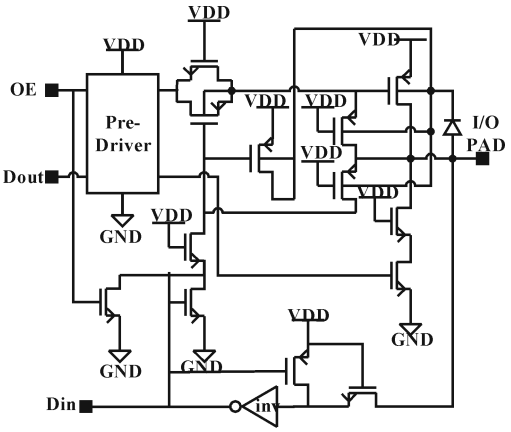

Fig. 3. Referential I/O buffer 1[5].

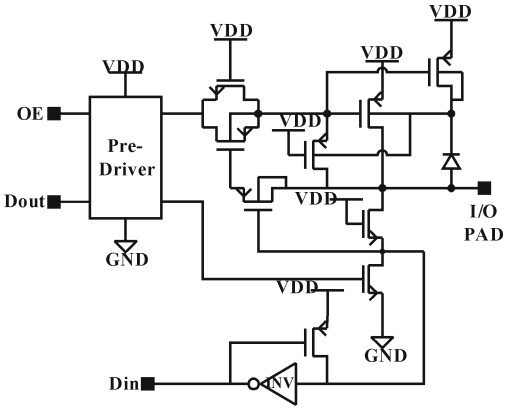

Fig. 4. Referential I/O buffer 2[6].

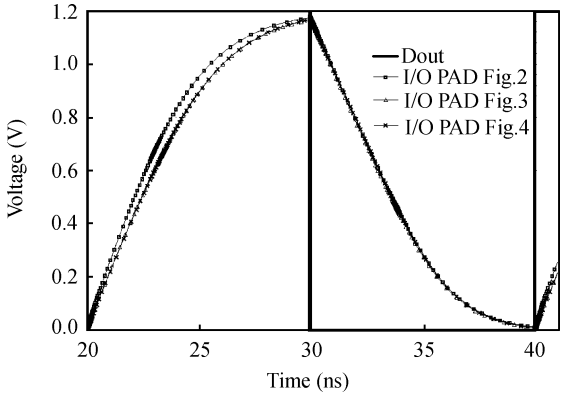

Fig. 5. Characteristics of Figs. 2, 3, and 4 in the transmit mode (20-pF load, 50-MHz I/O signal).

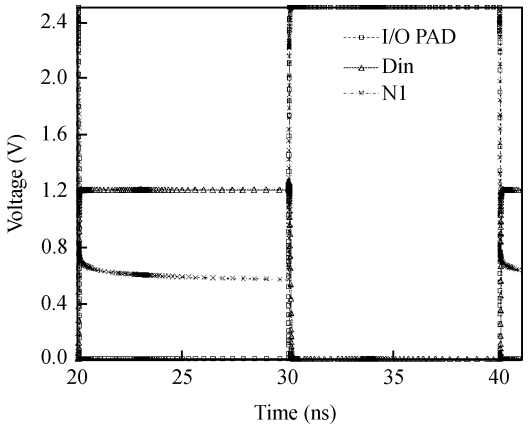

Fig. 6. Signal of Fig. 2 in the tri-state receive mode.

Table 1. Comparison of speed and power consumption.

Mixed-voltage I/O designs	Average power consumption at output load = 20 pF, frequency = 50 MHz (μW)	Delay time from Dout to I/O pad (ns)	Product of power consumption and speed (fW·s)	Subthreshold leakage issue
This work	2.33	2.85	6.64	No
Fig. 3[5]	4.11	3.03	12.45	Yes
Fig. 4[6]	3.28	3.06	10.04	No

delay time is defined as the average of rise time and the fall time, which are defined as the time from 1/2 Dout to 1/2 voltage of the I/O PAD. From the waveform of the I/O PAD in the transmit mode and from the comparisons in Fig.5, Fig.6, and Table 1, we can easily see that the characteristic of Fig. 2 is better. In Fig. 5, there is almost no difference for the fall time among Figs. 2, 3, and 4, because the pull-down units among these configurations are nearly the same. As shown in Table 1, the speed and power consumption in Fig. 2 is less than that in Figs. 3 and 4. Because of the same output loading (I/O PAD), which is much larger than the anodic parasitic capacitance, the dynamic power consumption is almost the same, which is decided by the power equation (1). So we need to exclude the power of the I/O PAD for a comparison of the power consumption. As shown in Fig. 6, we can see that the gate terminal of transistor MP1 is biased dynamically and the Din is a perfect input signal.

$$P = C_{\text{load}} V_{\text{DD}}^2 f. \tag{1}$$

4. Conclusion

Through the comparison above, the novel mixed-voltage I/O buffer in Fig. 2 has perfect characteristics in terms of speed, power consumption, sub-threshold leakage issue, and the complexity of future layout designs. Compared with Fig. 4, it is better by about ~34% in terms of speed and power consumption. A high reliability circuit always needs a simpler and more convenient mixed-voltage I/O buffer to interface other peripheral components, which can increase the productivity. The novel configuration has been verified successfully without the gate-oxide reliability problem in the 0.13-μm simulation and can be used in a scale-down process.

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