Ultra-low-voltage-trigger thyristor for on-chip ESD protection without extra process cost

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Abstract: A new thyristor is proposed and realized in the foundry's 0.18-μm CMOS process for electrostatic discharge (ESD) protection. Without extra mask layers or process steps, the new ultra-low-voltage-trigger thyristor (ULVT thyristor) has a trigger voltage as low as 6.7 V and an ESD robustness exceeding 50 mA/μm, which enables effective ESD protection. Compared with the traditional medium-voltage-trigger thyristor (MVT thyristor), the new structure not only has a lower trigger voltage, but can also provide better ESD protection under both positive and negative ESD zapping conditions.

Key words: thyristor; electro-static discharge; ultra-low-voltage-trigger; positive; negative
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1. Introduction

Electrostatic discharge (ESD) damage has become the main reliability issue for deep-submicron CMOS integrated circuit (IC) products. To overcome this ESD problem, on-chip ESD protection circuits are added around the input, output, and power pads of the CMOS ICs. Compared with traditional protection devices, thyristors are frequently used as ESD protection elements, as they have excellent protection capabilities[1−3].

The structure of a traditional medium-voltage-trigger thyristor (MVT thyristor) in a CMOS process is illustrated in Fig. 1. When a positive ESD pulse is zapping on the anode with the cathode grounded, the trigger voltage of the MVT thyristor mainly depends on the breakdown voltage of the N^+/P-well junction; generally, it is higher than the gate-oxide breakdown voltage[4]. So, this structure can not effectively protect the gate oxide of the internal circuits, and it is necessary to reduce the trigger voltage. On the other hand, when a negative ESD pulse is zapping on the anode with the cathode grounded, a forward biased diode formed by the P-well and the N-well with a low operating voltage (0.7 V) is used to discharge the ESD current. However, the protection level of the forward diode is lower than that of the forward thyristor.

To reduce the trigger voltage of the ESD protection structures, in some designs, ESD implantations have been added, and the ESD robustness can be significantly improved[5, 6]. However, the fabrication cost of an IC is also increased due to the additional mask layers and process steps.

In this paper, a new ultra-low-voltage-trigger thyristor (ULVT thyristor) ESD protection structure is proposed. Under both positive and negative ESD zapping conditions, the ULVT thyristor structure can be triggered with a low trigger voltage. Moreover, the new structure has no extra mask layers or process steps; so, no extra process cost is needed. This work has been successfully verified in GSMC's 0.18-μm CMOS process.

2. New ULVT thyristor ESD protection structure

In the typical 0.18-μm CMOS process, there are typically two kinds of devices: a 1.8-V core device and a 3.3-V I/O device. The cross-section view of the new proposed ULVT thyristor structure, in which a special NMOS is inserted, is shown in Fig. 2. The gate-oxide of this NMOS is the 3.3-V thick gate-oxide. However, in section "A", the 1.8-V N-type lightly-doped-drain (NLDD) and P-type halo (PHALO) implantations, which are always used in the 1.8 V thin gate-oxide NMOS, are implanted. The NLDD and PHALO implantations, which share the same mask, are normally used to overcome hot-carrier reliability problems and short channel effects. In the ULVT thyristor, this NLDD/PHALO junction is obtained simply by performing logic Boolean operations without an

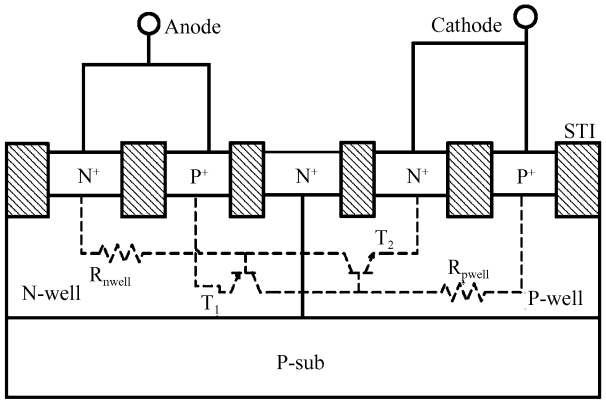

Fig. 1. Cross-section view of a traditional MVT thyristor in aCMOS process.

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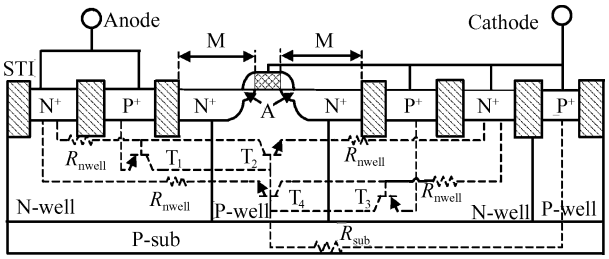

Fig. 2. Cross-section view of the newly proposed ULVT thyristor in a CMOS process.

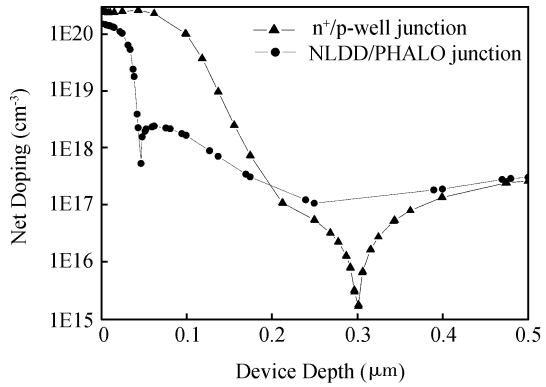

Fig. 3. TCAD simulation results for the net doping of NLDD/PHALO and N^+/P-well junctions.

extra mask.

By means of TCAD, the net doping of the NLDD/PHALO and N^+/P-well junctions are measured. The results are shown in Fig. 3. The former junction is much steeper and its doping concentration is much higher than the latter. Hence, the depletion-region width of the NLDD/PHALO junction is much smaller than that of the N^+/P-well junction under the same reverse-biased voltage. As the former junction will breakdown at a smaller voltage than the latter, it becomes the dominant junction for triggering.

When a positive ESD pulse is applied on the anode with the cathode grounded, the NLDD/PHALO junction quickly provides a leakage current into the P-well, even before the thyristor is triggered. This leakage current will lift the base potential of the parasitic NPN transistor (T_2) due to the voltage build-up over the substrate resistance. As the anode voltage rises up, T_2 will finally be turned on and the collector current of T_2 biases the parasitic PNP transistor (T_1). Subsequently, T_1 is also turned on. This initiates the positive feedback regeneration mechanism[7], which triggers the thyristor formed by T_1 and T_2.

When a negative ESD pulse is applied on the anode with the cathode grounded, the base/emitter junction of the parasitic NPN transistor (T_4) can easily be forward biased. As the potential difference between cathode and anode becomes larger, T_4 will be turned on. Subsequently, the positive feedback regeneration mechanism can easily trigger the thyristor formed by T_3 and T_4.

In the typical 0.18-μm CMOS I/O library, the I/O circuits also have two categories: one is for the 1.8-V IO pad and the other is for the 3.3-V IO pad. In the 3.3-V IO application, the

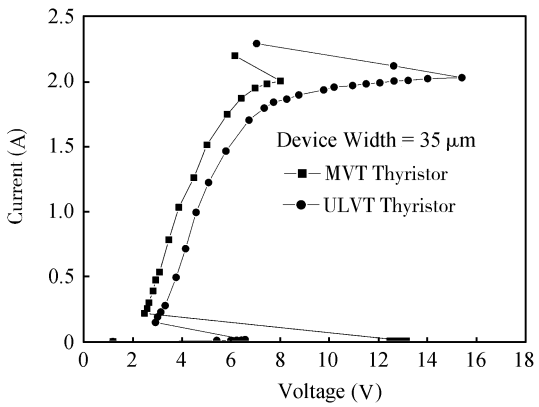

Fig. 4. TLP-measured *I–V* curves of the test structures under a positive ESD pulse.

pad always needs to accept a 3.3-V signal or a power supply. This ULVT thyristor can safely be used in it because the 3.3-V thick gate-oxide can sustain such a voltage under normal work conditions without gate-oxide reliability issues. On the other hand, in the 1.8-V IO application, the ULVT thyristor is also suitable, as it has a low trigger voltage to protect the thin gate-oxide of the internal circuits.

3. Experimental results and discussion

3.1. Transmission-line pulsing (TLP) measurement

The typical MVT thyristor and the newly proposed ULVT thyristor structures have been fabricated in GSMC's 0.18-μm CMOS process. Both devices have the same width of 35 μm. Using transmission-line pulsing (TLP) and under a positive ESD pulse, the ULVT thyristor has a lower trigger voltage (6.6 V) than the MVT thyristor (13.2 V), as shown in Fig. 4. As opposed to the MVT thyristor, a larger turn-on resistance is found in the curve of the ULVT thyristor. This is because that an equivalent N-well resistor is connected in series with the emitter of T_2, as shown in Fig. 2. This also makes the second breakdown voltage V_{T2} of the ULVT thyristor becomes larger than its trigger voltage V_{T1}. This feature is helpful for improving the ULVT thyristor's turn-on uniformity. In the actual application, this structure is always used in the 3.3-V IO design to protect the internal circuits. In this 0.18-μm CMOS process, the gate-oxide breakdown voltage of the 3.3-V device is about 11 V. As a result, the points in Fig. 4 having a voltage that is larger than the gate-oxide breakdown voltage are regarded as meaningless.

Under negative ESD zapping conditions, the TLP measured *I–V* curves of the two structures are shown in Fig. 5. In the MVT thyristor, the forward biased P-well/N-well diode is the only device to discharge the ESD current. However, in the ULVT thyristor, when the anode voltage is not low enough, the forward biased P-well/N-well diode is used to bypass the small ESD current. Subsequently, along with the decrease of the anode voltage, the thyristor, which is formed by T_3 and T_4, can finally be triggered to bypass the main ESD current. The trigger voltage of this reverse thyristor is also very low. This is because the base/emitter junction of the parasitic NPN (T_4)

Table 1. Test results for the newly proposed ULVT thyristor with different dimensions.

Device	ULVT thyristor width (μm)	M (μm)	Trigger voltage V_{T1} (V)	Holding voltage V_h (V)	Second breakdown current I_{T2} (A)	Corresponding I_{T2} per micron (mA/μm)
Device 1	35	1	6.57	2.92	1.98	56.6
Device 2	35	2	6.58	3.47	1.9	54.3
Device 3	35	3	6.68	4.05	1.81	51.7
Device 4	35	4	6.76	4.48	1.76	50.2

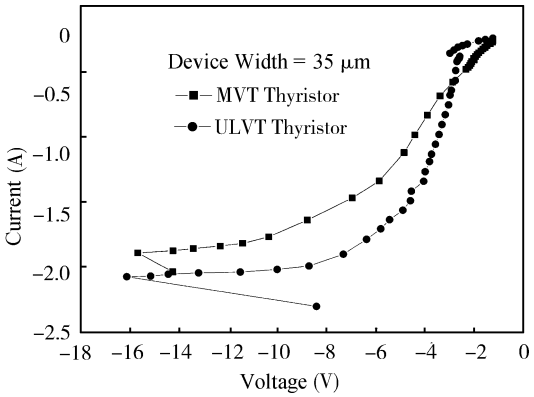

Fig. 5. TLP-measured I–V curves of the test structures under a negative ESD pulse.

can easily be forward biased under a negative ESD pulse. It can easily be found that the ESD protection level of the reverse thyristor is higher than the forward diode.

3.2. Holding voltage test with different dimensions

A relatively high and tunable holding voltage is desirable for ensuring latch-up immunity. Therefore, the influence of the parameter "M" (Fig. 2) of the new ULVT thyristor structure on its holding voltage has been studied. In the actual application, the anode of the ULVT thyristor is always connected with the IO pad or VDD, while the cathode is connected with ground. Also, there is a forward diode between the cathode and the anode formed by the P-well and the N-well. So, similar with the MVT thyristor, we will focus on the holding voltage test under the positive ESD zapping condition. It is found that the holding voltage is increased along with the increment of M, as shown in Table 1. The reason is that the current path becomes longer and the turn-on resistance increases. So, we can choose suitable devices for different power supply applications. In Table 1, it should be pointed out that the increase of M will alter the trigger voltage slightly. Meanwhile, when measuring the second breakdown current from the I–V curves, a point whose corresponding voltage is larger than 11 V is also ignored. It is found that increasing M will degrade the robustness of the device. However, this drawback can be minimized by using a multi-finger layout[8, 9].

4. Conclusion

In this work, a new ultra-low-voltage-trigger thyristor (ULVT thyristor) has been successfully verified in GSMC's 0.18-μm CMOS process. Experimental results have shown that the trigger voltage can be reduced significantly as compared to the traditional MVT thyristor. Furthermore, under a negative ESD zapping condition, the ULVT thyristor has a better ESD protection level than the MVT thyristor. Moreover, no extra mask layers or process steps are needed to form this structure. This ULVT thyristor has already been used in the input, output, and power clamp circuits design. And it provides a good ESD protection for the internal circuits.

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