A low-loss V-groove coplanar waveguide on an SOI substrate*

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Abstract: A novel low-loss 50-Ω coplanar waveguide with V-groove on an SOI substrate is proposed. Through a CMOS-compatible process and anisotropic etching of silicon, surface silicon is removed from the SOI. The measured results show that the V-groove coplanar waveguide causes about 50% less loss than the conventional one at a high frequency of up to 40 GHz.

Key words: SOI; coplanar waveguide; low loss; radio frequency

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1. Introduction

As the operation frequency and the integration are improved, RF circuits on low resistivity Si substrates perform poorer because of high energy losses and serious crosstalk through the substrate[1, 2]. With its smart structure, SOI offers many advantages over bulk Si CMOS technology, such as low power consumption, low crosstalk, and a low parasitic capacitance at high frequencies[3–5]. In order to obtain a good performance of the RF SOC, passive components should have a low loss and a low parasitic effect.

In recent years, passive devices on SOI substrates have got a considerable amount of attention and gained some development[6–10]. In Ref. [6], a 0.6 nH STP (single-turn, multiple metal levels in parallel) inductor with a peak Q of 52 was obtained at 5 GHz. In Ref. [7], a 20 pF high-density 3-dimensional vertical parallel plate (VPP) capacitor with a high Q of 22 at 1 GHz was obtained. In Ref. [9], the behavior of a 50-Ω thin film microstrip and a coplanar waveguide (CPW) on SOI substrates at high temperatures were researched.

CPWs are widely used as interconnects and matching networks in MMICs. It is important to design a low loss CPW to obtain high performance MMICs. In this paper, the substrate loss reduction is creatively achieved by removing the surface Si from the SOI substrate to realize a low loss CPW.

2. Design and simulation results

A conventional CPW with a 50-Ω characteristic impedance was first designed on an SOI substrate for comparison. The width of the signal line and the ground lines are 44 and 100 μm, respectively. The space between the signal line and the ground lines is 30 μm. The length of the CPW is 2 mm. As we know, a significant portion of the CPW line losses can be attributed to the substrate loss because of the impedance offered by the capacitive coupling between the signal line and the substrate. Except for that, the electric field mainly centralizes in the substrate under the gaps between the signal line and the grounds. If the Si can be removed where the electric field is strongest, the energy loss of the CPW can be significantly reduced. Figure 1 shows the profile of (a) a conventional CPW and (b) a V-groove CPW.

Figure 2 is the electric field of an conventional CPW on (a) an SOI substrate and (b) a V-groove CPW, simulated by HFSS. It is obvious that the largest magnitude of the electric field decreases from 1.77×10^6 to 1.61×10^6 V/m because of the absence of surface Si under the gap between the signal

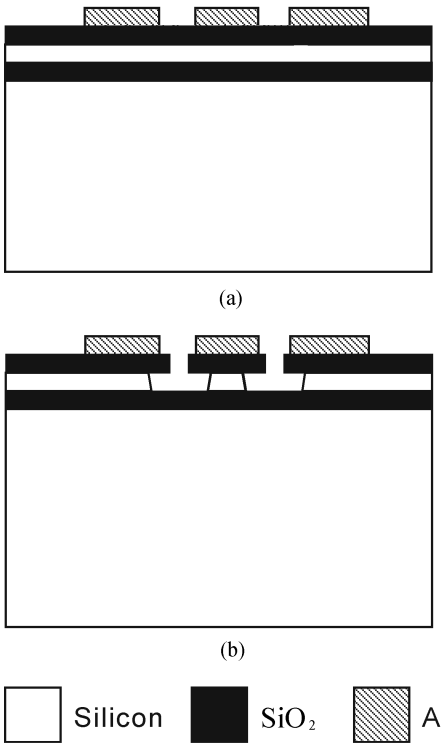

Fig. 1. Profile of conventional and V-groove CPW on an SOI substrate: (a) Conventional CPW; (b) V-groove CPW.

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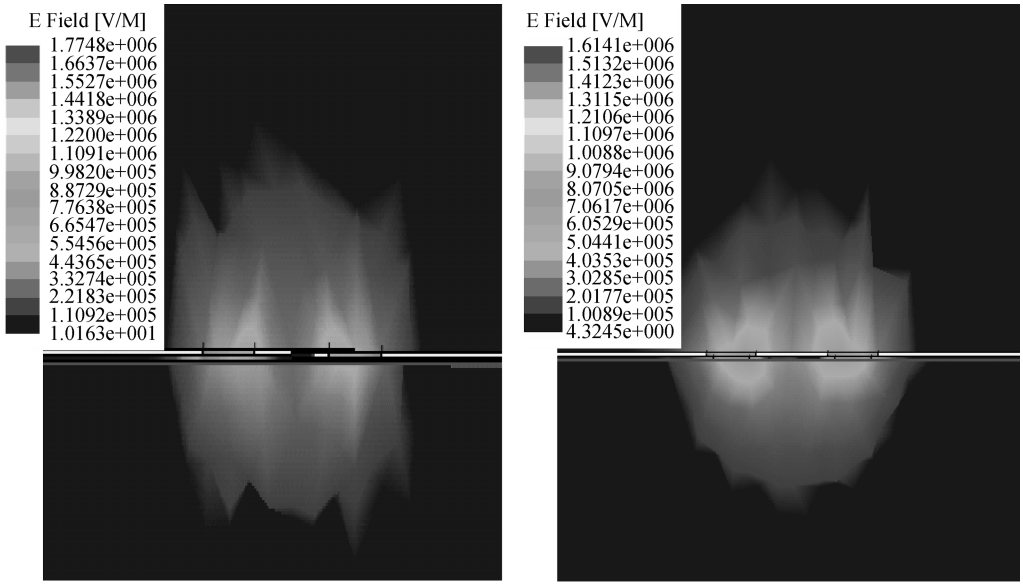

(a) (b)

Fig. 2. Simulation of electric field distribution: (a) Conventional CPW; (b) V-groove CPW.

Table 1. Parameters of adopted SOI substrates.

Sample No.	Thickness of surface silicon (μm)	Thickness of buried oxide (μm)
Sub-A	0.37	0.21
Sub-B	0.15	0.19

and the grounds. The substrate loss can be eliminated effectively. So a lower less energy loss in the substrate directly leads to a decrease of the total loss. That is because the introduction of a V-groove leads to the decrease of the effective dielectric constant in the region of the electromagnetic field concentration under the transmission line. The simplified effective dielectric constant ε_e is as follows,

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2}. \quad (1)$$

ε_r is the relative dielectric constant of Si.

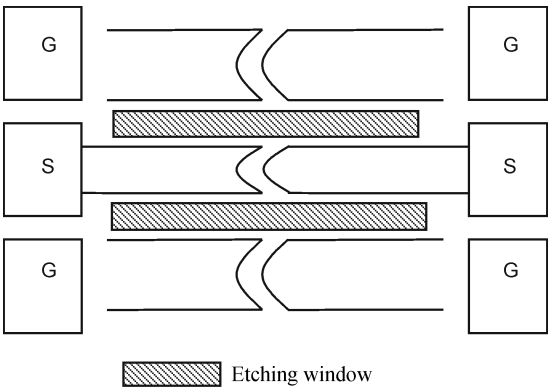

Fig. 3. Etching window to form V-groove CPW.

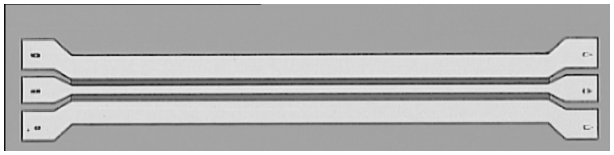

Fig. 4. Photo of fabricated V-groove CPW.

3. Fabrication and measurement results

In order to obtain valid results, the performance of the CPW was measured from two groups of SOI substrates with different parameters. The SOI substrates were realized by a SIMOX procedure from high-resistivity silicon (1225 Ω·cm $\leqslant \rho \leqslant$ 2275 Ω·cm). Table 1 lists the parameters of the substrates.

The fabrication process of CPWs on two sets of SOI substrates are as follows. 1 μm-thick SiO_2 was firstly deposited by PECVD. Then a 1.4 μm-thick Ti/Au layer was evaporated and electroplated. After being lithographed and etched, a conventional CPW was fabricated. To make the V-groove, the PECVD SiO_2 was etched in the gap between the signal and ground lines (Fig. 3). After that, sufficient wet etching in a 35% KOH solution completed the V-groove CPW utilizing anisotropic characteristics of silicon. Figure 4 is a photograph of the proposed CPW. Black rectangles between the signal and ground lines in the figure are the realized V-groove.

The transmission performance of the CPWs was measured at frequencies ranging from 50 MHz to 40 GHz by using an E8363B network analyzer and a Cascade on-wafer probe. Figure 5 shows the transmission performance of conventional and V-groove CPWs on the two different SOI substrates Sub-A and Sub-B. Figure 5(a) shows the S-parameters of the V-groove CPW on Sub-A. It shows excellent transmission characteristics in the whole frequency range. Figure 5(b) is the tested S_{21} comparison of the proposed and the conventional CPWs on Sub-A and Sub-B. On both substrates, the insertion loss of conventional CPWs is more than –4 dB; while the proposed CPWs have an insertion loss of about –2 dB, which is much better than for the conventional ones. At 20 GHz, the

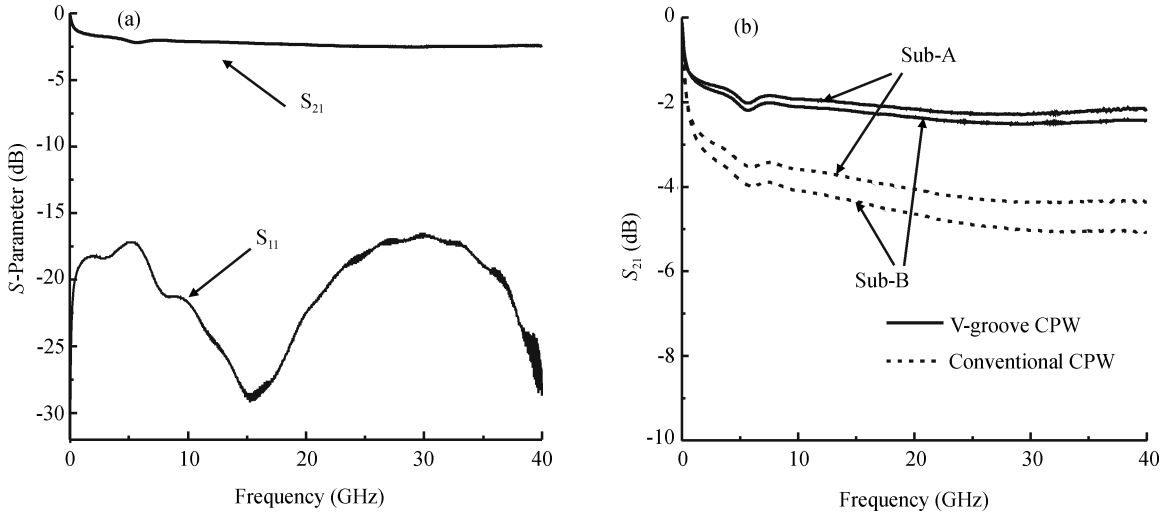

Fig. 5. *S* -parameter results: (a) *S* -parameters of V-groove CPW on Sub-A; (b) S_{21} comparison of V-groove and conventional CPWs on different substrates.

proposed CPW and the conventional CPW on Sub-A have an insertion loss of –2.16 and –4.06 dB, respectively. The proposed CPW and the conventional CPW on Sub-B have an insertion loss of –2.36 and –4.64 dB, respectively. Because Sub-A and Sub-B have different material parameters, the introduction of a V-groove does not change the substrates in exactly the same way. Thus, results on Sub-A and Sub-Bare slightly different from each other. The measurement results clearly show that the proposed structure has nearly a 50% improvement of the performance compared with the conventional CPW. The results have proved that the substrate loss is significantly reduced by removing the surface silicon of SOI substrates. The proposed new structure is excellent to reduce the insertion loss of transmission lines in radio frequencies.

4. Conclusions

In this paper, we proposed a novel low-loss 50-Ω coplanar waveguide with a V-groove on an SOI substrate to reduce the insertion loss of coplanar waveguides on SOI substrates at high frequencies. By removing the surface Si under the gaps between the signal and ground lines where the electric field is the strongest, a lower loss of CPW can be achieved. The fabricated 50-Ω new structure CPW on Sub-A shows an insertion loss less than 2.3 dB up to 40 GHz. This is nearly 50% lower than the conventional one. For further validation, we have fabricated the same CPWs on Sub-B with different substrate parameters. The same results are observed. The measurement results agree very well with simulation results. Furthermore, the process for a V-groove CPW is compatible with the conventional CMOS procedure. Therefore, the proposed new structure is very promising for reducing the insertion loss of transmission lines at high frequencies, and is very useful in RF circuits.

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