Modeling of self-heating effects in polycrystalline silicon thin film transistors

Deng Wanling(邓婉玲)[1,†] and Zheng Xueren(郑学仁)[2]

(1 Department of Electronic Engineering, College of Information Science and Technology, Jinan University, Guangzhou 510630, China)

(2 Institute of Microelectronics, South China University of Technology, Guangzhou 510640, China)

Abstract: An analytical DC model accounting for the self-heating effect of polycrystalline silicon thin-film transistors (poly-Si TFTs) is presented. In deriving the model for the self-heating effect, the temperature dependence of the effective mobility is studied in detail. Based on the mobility model and a first order approximation, a closed-form analytical drain current model considering the self-heating effect is derived. Compared with the available experimental data, the proposed model, which includes the self-heating and kink effects, provides an accurate description of the output characteristics over the linear, the saturation, and the kink regimes.

Key words: polycrystalline silicon thin film transistors; self-heating; surface potential

DOI: 10.1088/1674-4926/30/7/074002 **EEACC:** 2560B **PACC:** 7340N

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are getting more attractive for active matrix liquid crystal display (AMLCD)[1] and active matrix organic light emitting diode (AMOLED)[2]. Although there are similarities between poly-Si TFTs and their crystalline silicon counterparts, the polysilicon grain boundary traps and intra-grain defects introduce many significant differences, including a self-heating effect. As a result, it is important to accurately model their complicated characteristics to determine their precise circuit behavior.

Since poly-Si TFTs are fabricated on glass substrates with a small thermal conductivity, the power dissipation in the devices is increased, and therefore, the self-heating effect becomes serious and affects the TFT characteristics. As the device temperature rises by self-heating, the effective mobility at lower gate voltages initially increases while at higher gate voltage it decreases. Therefore, like SOI devices, high performance poly-Si TFTs exhibit a negative output conductance in the saturation current when operated at high gates and drain biases[3,4]. However at a low gate bias, the drain current monotonously increases as the temperature is increased[4,5]. Self-heating related reliability has also been investigated elsewhere[6,7]. However, the analysis of the correlation between reliability and self-heating is beyond the scope of the present work, as we focus on the electrical characteristics affected by self-heating.

In this paper, we study the effect of self-heating on the electrical characteristics. For the self-heating effect, an analytical model is established and applied to the fundamental relationship between the output current under the condition of self-heating and the operation bias. Accounting for the self-heating effect, a physical drain current model is developed and compared with the experimental data.

2. Basic drain current model

Because there is a mixture of grains and amorphous-like structures in polysilicon films and a large number of defects exist within the films, the basic assumption that we made is that a continuous density of states (DOS) with exponential tails at the grain boundaries is uniformly distributed throughout the film. This assumption is valid for small grains TFTs[1,8]. Also we assume there is an n-type poly-Si TFT.

A single exponential DOS distribution in the upper half of the gap is used. Therefore, the density of ionized acceptor-like traps is given by[1]

$$N_{\mathrm{TA}}^{-} = g_{\mathrm{c1}} \frac{\pi kT}{\sin(\pi kT/E_1)} \exp\left(\frac{E_{\mathrm{F0}} + q\psi - q\phi_{\mathrm{n}} - E_{\mathrm{C}}}{E_1}\right), \quad (1)$$

where g_{c1} is the states density, E_1 is the inverse slope of states, and E_{C} is the energy at the bottom of the conduction band.

Using the gradual channel approximation and an one-dimensional Poisson equation, the drain current expression I_{D0} without considering the self-heating effect is obtained as

$$I_{\mathrm{D0}} = \left\{1/[(1/I_{\mathrm{sub}})^m + (1/I_{\mathrm{inv}})^m]\right\}^{1/m}. \quad (2)$$

Here, I_{sub} is the subthreshold current, which was derived in our previous work[1], m determines how sharply I_{D0} changes from subthreshold to strong inversion, and I_{inv} is the drain current for the strong inversion region, which is modeled by

$$I_{\mathrm{inv}} = (M+1)I_{\mathrm{inv0}}, \quad (3)$$

† Corresponding author. Email: dwanl@126.com

Received 16 January 2009, revised manuscript received 20 February 2009

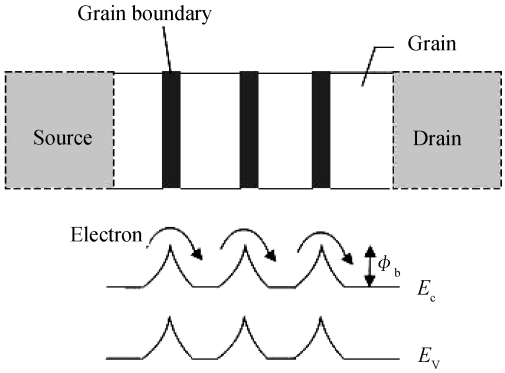

Fig. 1. Schematic diagram of the channel of a poly-Si TFT showing the electrons passing through the grains and across the grain boundaries.

$$I_{\text{inv0}} = \frac{W}{L}\mu_{\text{eff}}\left\{g(\psi_{\text{sL}}) - g(\psi_{\text{ss}}) - \phi_{\text{t}}\left[Q_{\text{i}}(\psi_{\text{sL}}) - Q_{\text{i}}(\psi_{\text{ss}})\right]\right\}, \quad (4)$$

$$g(\psi_{\text{s}}) = \frac{-qb_2}{(b_1)^{2-\frac{2\phi_{\text{t}}}{\phi_{\text{eff}}(\psi_{\text{s}})}}}\frac{\phi_{\text{eff}}(\psi_{\text{s}})}{3\phi_{\text{eff}}(\psi_{\text{s}}) - 2\phi_{\text{t}}}\left[(V_{\text{G}} - V_{\text{fb}} - \psi_{\text{s}})^{3-\frac{2\phi_{\text{t}}}{\phi_{\text{eff}}(\psi_{\text{s}})}}\right], \quad (5)$$

$$Q_{\text{i}}(\psi_{\text{s}}) = qb_1\left(\frac{V_{\text{G}} - V_{\text{fb}} - \psi_{\text{s}}}{b_2}\right)^{2-\frac{2\phi_{\text{t}}}{\phi_{\text{eff}}(\psi_{\text{s}})}}, \quad (6)$$

$$b_2 = \frac{\sqrt{2q\varepsilon_{\text{si}}n_{\text{i}}\phi_{\text{t}}}}{C_{\text{OX}}}\exp\left(\frac{E_{\text{F0}}/q}{2\phi_{\text{t}}}\right), \quad (7)$$

$$M = A_{\text{i}}\left[V_{\text{DS}} - (\psi_{\text{sL}} - \psi_{\text{ss}})\right]\exp\left[\frac{-B_{\text{i}}}{V_{\text{DS}} - (\psi_{\text{sL}} - \psi_{\text{ss}})}\right], \quad (8)$$

where M is the modeled multiplication factor, and ψ_{sL} and ψ_{ss} are the surface potentials at the drain and source, respectively. The deduction of I_{inv} is similar to that of I_{sub}. An evaluation of the parameters in Eqs. (1)–(8) can be determined by referring to our previous work[1].

3. Modeling of the self-heating effect

In poly-Si TFTs, the substrate, typically a glass, has a very poor thermal conductivity. This results in a higher temperature in the channel and a significant self-heating effect. Some researchers have discussed the relationship between the effective mobility and the temperature[9]. It has been reported that the value of the mobility is strongly affected by the temperature.

Figure 1 shows the electron movement of a n-channel poly-Si TFT during the electrical conduction in the presence of grain boundaries. For simplicity, we assume that the polysilicon is composed of a linear chain of crystallites called grains and the associated grain boundaries (GB). The grain boundary region has a very high defect density and results in a potential barrier (ϕ_{b}) formation[10]. Applying Mathiessen's rule, the effective mobility μ_{eff} model can be written as

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{GB}}} + \frac{1}{\mu_{\text{G}}}, \quad (9)$$

where μ_{GB} is the carrier mobility across the grain boundary and μ_{G} is the mobility for a carrier passing through the interior region of the grain.

At a low or moderate gate bias ($V_{\text{G}} < V^*$), the potential barrier height at the GB is high, which causes the mobility to be small. Therefore, at low or moderate gate voltages, μ_{GB} is the dominant term of μ_{eff}, and we get

$$\mu_{\text{eff}} \approx \mu_{\text{GB}}. \quad (10)$$

At the GB, the carriers have to hop over the barriers. As the temperature rises, the barrier height is lowered, and therefore, the mobility of polysilicon increases[5, 11]. Seto's[10] experimental data shows that for doping concentration less than 1×10^{19} cm^{-3}, the mobility decreases exponentially with $1/kT$. Analogous results were also obtained by Voutsas[9]. Thus, the temperature dependence of the mobility can be modeled as

$$\mu_{\text{GB}} = \mu_{\text{GB0}}\exp\left[-\frac{\chi}{k}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right], \quad (11)$$

where T is the temperature increment induced by self-heating, T_0 is the ambient (room) temperature, μ_{GB0} is the room temperature values of μ_{GB}, and χ is a characteristic energy. Moreover, μ_{GB0} has a physical form of

$$\mu_{\text{GB0}} = \mu_0\exp\left(-\frac{\phi_{\text{b}}}{kT_0/q}\right), \quad (12)$$

$$\phi_{\text{b}} = \left[(V_{\text{G}} - V_{\text{i}})^2 + V_{\text{Q}}^2\right]^{\frac{1}{2}} - (V_{\text{G}} - V_{\text{i}}), \quad (13)$$

where μ_0, V_{Q}, and V_{i} are treated in this paper as mobility fitting parameters.

Using Taylor's approximation formula, the exponential term of Eq. (11) becomes

$$\exp\left[-\frac{\chi}{k}\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \approx 1 - T_{\text{GB}}\left(\frac{1}{T} - \frac{1}{T_0}\right). \quad (14)$$

The approximation of Eq. (14) is valid because the value inside the square brackets is smaller than one. Here, $T_{\text{GB}} = \chi/k$.

The temperature increase induced by self-heating in the device can be expressed as

$$T - T_0 = I_{\text{D}}V_{\text{DS}}R_{\text{th}}, \quad (15)$$

where I_{D} is the drain current, and R_{th} is the thermal resistance of the device. R_{th} is strongly dependent on the substrate materials and the TFT structure[5, 11]. It is obvious that the glass substrate is very important for the self-heating[12]. Since it acts as a thermal insulator and, therefore, contributes significantly to the heating of the poly-Si film. The value of R_{th} can be approximately calculated as[12]

$$R_{\text{th}} = (\pi k_{\text{glass}})^{-1}\ln[16d_{\text{glass}}/(\pi L)], \quad (16)$$

where k_{glass} and d_{glass} are the thermal conductivity and the thickness of the substrate (glass), respectively.

Substituting the temperature dependence of the mobility into the basic I–V model Eq. (2) and using Eq. (15), the

Table 1. Parameters for simulation*.

Symbol (units)	TFTs in Fig. 2
W (μm)	10
L (μm)	10
t_f (μm)	0.2
R_{th} (K/W)	1×10^4
C_{OX} (F/cm^2)	2.93×10^{-7}
g_{c1} (cm^{-3}eV^{-1})	1×10^{20}
E_1 (eV)	0.12
E_{F0} (eV)	0.01
V_{fb} (V)	–2.5
T_{GB} (K)	280
β_1 (K^{-1})	4.3×10^{-3}
μ_0 (cm^2/(V·s))	350
θ_1 (V$^{-1/3}$)	0.1
θ_2 (V^{-2})	1×10^{-4}
V_Q (V)	0.05
V_i (V)	–0.8
A_i (V^{-1})	0.4
B_i (V)	10
m	4

* The value of the poly-Si thin film thickness t_f of Fig. 2 was not stated in Ref. [4], so we present a typical value.

drain current including self-heating when the gate bias is low or moderate is obtained by

$$I_D = I_{D0}\left(1 + \frac{T_{GB}}{T_0}\frac{I_D V_{DS} R_{th}}{I_D V_{DS} R_{th} + T_0}\right). \quad (17)$$

Solving Eq. (17), one obtains

$$I_D = \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \quad (18)$$

where

$$a = V_{DS} R_{th}, \quad (19)$$

$$b = \left[T_0 - I_{D0}\left(1 + \frac{T_{GB}}{T_0}\right) V_{DS} R_{th}\right], \quad (20)$$

$$c = -I_{D0} T_0. \quad (21)$$

As the gate voltage increases, the potential barrier height decreases. When the gate bias is large enough, the mobility saturates. If the gate bias further increases, similar to the mobility behavior in the single-crystal counterpart, the mobility degradation caused by scattering occurs. Iñiguez *et al.*[8] have plotted the relationship between the effective mobility and the gate bias, and a peak value of μ_{eff} can be seen from that plot. When $V_G > V^*$, since the barrier height is sufficiently lowered, the electron mobility inside the grain, which is affected by scattering, starts to dominate. As a consequence, μ_G is the dominant term of Eq. (9). Similar to a single-crystal MOSFET, μ_G decreases as the temperature is increased. In this case, the temperature dependence of the mobility can be approximated as[3]

$$\mu_{eff} \approx \mu_G = \mu_{G0}\left[1 - \beta_1(T - T_0)\right], \quad (22)$$

$$\mu_{G0} = \frac{\mu_0}{1 + \theta_1 (V_G)^{1/3} + \theta_2 (V_G)^2}, \quad (23)$$

where β_1 is a temperature coefficient, and θ_1 and θ_2 are the mobility degradation parameters.

Using Eqs. (3) and (22), the drain current including self-heating is given by

$$I_D = \frac{I_{inv}}{1 + \beta_1 I_{inv} V_{DS} R_{th}}, \quad (24)$$

where I_{inv} replaces I_{D0} because when the gate bias is high enough the device operates in the strong inversion region.

For different bias conditions, the value of V^* determines which component, either μ_{GB} or μ_G, is the dominant term of the effective mobility. If μ_{GB} dominates, the main scattering mechanism is grain boundary scattering. On the other hand, if μ_G dominates, the main scattering mechanism should be phonon scattering and surface roughness scattering. Therefore, V^* can be extracted from the plot of effective mobility versus gate voltage. We roughly estimate V^* as the gate voltage at which the mobility tends to its maximum.

4. Results and discussion

As indicated in the previous sections, the self-heating effect of poly-Si TFTs has been analytically modeled. The model derived above has been implemented into BSIMProPlus using the Model Wizard[13] tool. BSIMProPlus is an efficient and accurate SPICE model extraction software, and supports various models for CMOS, SOI, bipolar, TFT, and so on. The Model Wizard tool can generate C source code files and a project file for the model engine. To verify the proposed models, a comparison with available experimental data has been completed. The parameters of the TFTs used in the simulation are listed in Table 1.

The validation is achieved by comparing our model with experimental data[4] with W/L = 10 μm/10 μm. The devices were fabricated using excimer laser annealing (ELA) or solid-phase crystallization (SPC) on quartz substrates. A 12 nm thick gate oxide was grown in an electron cyclotron resonance (ECR) N_2O-plasma at 400 °C, 2 mTorr, and a microwave power of 600 W. The gate and source/drain regions were doped by ion implantation with a dose of 5×10^{15} cm^{-2} and annealed at 900 °C in N_2. Finally, all the TFTs were hydrogenated in an ECR H_2-plasma at 300 °C for 1 h[4].

As shown in Fig. 2, the model simulation results match the experimental data well. When measured at high V_G and the operation of TFT enters into the saturation region, the device output characteristic present a negative output conductance in the saturation current due to self-heating, which is more severe at higher V_G. Furthermore, when the simulation switches off the introduced self-heating factor, as shown by the dotted line in Fig. 2, the drain current model cannot explain the negative output conductance in the saturation. When measured at low V_G, the negative output conductance disappears, and the

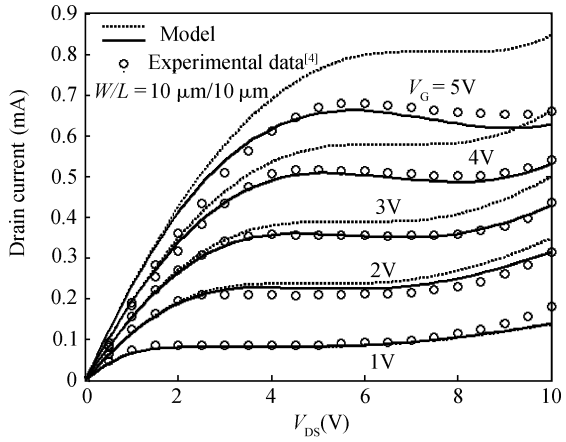

Fig. 2. Comparison of drain currents between model results and experimental data[4] with W/L = 10 μm/10 μm. The continuous lines are best fitted when considering self-heating effects using values for parameters given in Table 1. The dotted line is the simulation without accounting for the self-heating effect.

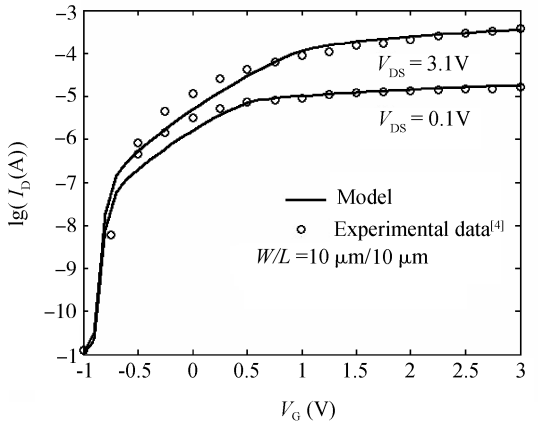

Fig. 3. Comparison of I_D–V_G characteristics between model results and experimental data[4] with W/L = 10 μm/10 μm.

drain current exhibits an increase with V_{DS}. When V_{DS} is not high enough to make impact ionization take effect, this behavior can be explained by self-heating as the mobility increases with increasing temperature. As a result, V^* can be deduced from Fig. 2 and it is about 1.5 V.

As shown in Fig. 2, when the applied V_{DS} is further increased and the device operates in the kink regime, the kink effect becomes significant and the drain current keeps rising with increasing V_{DS}.

Figure 3 depicts the I_D–V_G characteristics at different drain voltages. A good fit to the experimental data is also observed.

5. Conclusions

In this paper, by taking the self-heating effect into account, an extended I–V model for poly-Si TFTs was developed and verified. The proposed model accounts for the dependence of the effective mobility on the temperature, and uses the relation between the mobility and the temperature to model the self-heating effect. The combined model accurately reproduces the output characteristics of poly-Si TFTs. Moreover, the model is suitable for the use in device and circuit simulations.

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