Effect of chemical polish etching and post annealing on the performance of silicon heterojunction solar cells*

Jiang Zhenyu(蒋振宇), Dou Yuhua(豆玉华), Zhang Yu(张瑜), Zhou Yuqin(周玉琴)†, Liu Fengzhen(刘丰珍), and Zhu Meifang(朱美芳)

(Graduate University of the Chinese Academy of Sciences, Beijing 100049, China)

Abstract: Amorphous/crystalline silicon heterostructure solar cells have been fabricated by hot wire chemical vapor deposition (HWCVD) on textured p-type substrates. The influence of chemical polish (CP) etching and the post annealing process on the solar cell performance have been studied. The CP treatment leads to a reduction of stress in the i-layer by the slight rounding of the pyramid peaks, therefore improving the deposition coverage and the contact by each layer, which is beneficial for the performance of the solar cells. An optimized etching time of 10–15 s has been obtained. A post annealing process leads to a considerably improved open voltage (V_{oc}), filled factor (FF), and conversion efficiency (η) by restructuring the deposited film and reducing the series resistance. An efficiency of 15.14% is achieved that represents the highest result reported in China for an amorphous/crystalline heterostructure solar cells based on the textured p-type substrates.

Key words: HIT solar cells; chemical polishing; post annealing; HWCVD

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1. Introduction

Heterojunctions with intrinsic thin-layer (HIT) solar cells consisting of an intrinsic amorphous silicon layer inserted between the hydrogenated amorphous silicon (a-Si:H) emitter layer and the crystalline silicon (c-Si) wafer are a promising alternative to conventional c-Si solar cells[1,2]. The main advantages of HIT solar cells are: (3) a low temperature process (< 200 °C) to fabricate the device and (2) excellent interface passivation between the emitter and the wafer. Sanyo has achieved the world's highest conversion efficiency of 22.3% for solar cells fabricated by plasma enhanced chemical vapor deposition (PECVD) on an n-type Cz wafer[1]. However, HIT solar cells prepared by hot-wire chemical vapor deposition (HWCVD) technique have some advantages compared with those prepared by PECVD, such as no plasma instability, no ion bombardment during the deposition process, and a higher concentration of atomic hydrogen treatment, which is beneficial for the passivation of the a-Si:H/c-Si interface[3,4]. The highest conversion efficiency of 18.7% has been reported for the solar cells prepared by HWCVD on p-type Cz silicon wafers by NREL[5]. This result shows a relatively lower conversion efficiency than Sanyo's; however, it is possible to further improve the conversion efficiency of the solar cells fabricated by HWCVD based on its advantages mentioned above.

The random texturization of c-Si wafers, which can maximize the light absorbed into the solar cells, is always achieved by chemical anisotropic etching using alkaline solutions. However, the presence of surface alkaline contamination is responsible for the low lifetime of minority carriers after alkaline texturing, while the sharp pyramid peaks might account for an insufficient coverage and contact by each layer, consequently leading to a degradation of the solar cell performance. Hence, a CP treatment, which consists of HNO_3, CH_3COOH, and HF, has been introduced after pyramidal texturing. It either serves to reduce the surface alkaline contamination or to reduce the stress in the i-layer by the slight rounding of the pyramids peaks[6]. After the solar cell was fabricated, a low temperature annealing (< 200 °C, in vacuum) also benefited solar cells whose emitter are amorphous. This is probably due to either the restructuring of the deposited film or the redistribution of Na ions at the a-Si/c-Si interface during the annealing process[6].

In this work, we fabricate HIT solar cells by HWCVD and study the influence of the CP etch and the post annealing process on the solar cell performance. In order to study the effect of CP etching and annealing on the device performance, an observation for the surface morphology and the elemental composition analysis by SEM, surface reflectance, and minority carrier lifetime measurements have been conducted after the CP treatment. Moreover, the diode factors and series resistance have been obtained from dark and photo *I–V* measurements.

2. Experimental details

Si(100) wafers (Cz, p-type, 1–3 Ω·cm) were cleaned by the standard RCA process. Before texturization, the saw dam-

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† Corresponding author. Email: yqzhou@gucas.ac.cn

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Table 1. Deposition conditions for the thin films.

Type	T_s (°C)	T_f (°C)	H_2 (sccm)	SiH_4 (sccm)	PH_5 (sccm)	Pressure (Pa)
(i)a-Si:H	150	1780	2	2	–	2, 5
(n)a-Si:H	150	1780	2	2	0.02	2, 5

age was removed in a 20wt% NaOH solution at 75 °C for 10 min. Then the samples were textured in 15 wt% $Na_3PO_4 \cdot 12H_2O$ together with 0.4% isopropyl alcohol at 80 °C for 30 min. After rinsing in boiling RCA Ⅱ solution (H_2O : HCl : H_2O_2 = 6 : 1 : 1) for 10 min, the CP etching was carried out by the solution consisting of HNO_3 : CH_3COOH : HF = 30 : 10 : 4. The CP etching time (t_{CP}) varied from 0 to 120 s. Measurements of wafer surface reflectance and the minority carrier lifetime (using a WT-2000 wafer scanner) were conducted following the CP etching.

Following the surface treatment, wet-chemical oxide layers on etched Si surfaces were prepared by boiling a solution of H_2SO_4 : H_2O_2 (1 : 1) for 10 min. Before deposition, the c-Si surface was cleaned by removing the wet-chemical oxides using a 2% HF treatment for 30 s until it became hydrophobic and was immediately transferred to the chamber of the deposition system. Atomic hydrogen treatment of the c-Si surface was done before depositing the films. Thereby, the c-Si surface was hydrogenated in 20 sccm H_2 for 30 s at a process pressure of 10 Pa combined with wire heating at 1850 °C. All the thin silicon films were deposited by HWCVD under the deposition conditions summarized in Table 1.

The heterojunction silicon solar cells were fabricated following the structure of Ag-grid/ITO/(n)a-Si:H/(i)a-Si:H/(p)c-Si/Al. The thickness of doped (n)a-Si:H layers was 12 nm, whereas the (i)a-Si:H layer was about 5 nm thick. After the Si film was deposited, an ITO layer of 80 nm was deposited by reactive thermal evaporation. The ITO layer has a sheet resistance around 50 Ω and serves to collect the current and also as an antireflection coating. Then, a grid of Ti/Ag with 20% shadowing was thermally evaporated through a shadow mask on top of the front ITO layer. Evaporated aluminium was used for the rear contacts. Finally, we annealed the cells under 1×10^{-4} Pa at 200 °C for 2 h. *I–V* characteristics of solar cells were measured at 300 K under AM 1.5 conditions.

3. Results and discussion

3.1. Effect of CP etching

The coverage of the silicon thin films on a pyramid surface is crucial in obtaining a high quality device; however, the sharp peak of the pyramids tends to suppress the conformation of a uniform thin films coverage. Therefore, CP etching was introduced to smoothen the pyramids and, hence, to improve the coverage of the silicon films as well as the performance of the solar cells[4].

Investigations were undertaken to understand the cause of the improvement on solar cells after CP etching. Figure 1 shows the SEM images of the textured wafer surfaces after CP treatment. t_{CP} varies from 0 to 120 s. The average angle for the top of a pyramid is monotonously increased from 72.52 ° to 92.34 ° when increasing t_{CP}, as listed in Table 2, indicating the slight rounding of the pyramid peaks. On the one hand, the slight rounding of the pyramid peaks might account for a better coverage of the silicon films, and, on the other hand, it may increase the reflectivity of the surface, hence, reducing the light absorption of solar cells. Figure 2(a) shows the reflectance of textured wafers as a function of the incident wavelength for different t_{CP}. The average reflectivity (from 400 to 1100 nm) of a wafer surface increases slightly in the beginning from 10.10% (t_{CP} = 0 s) to 11.45% (t_{CP} = 5 s), then decreases, reaching its lowest value of 10.90% for t_{CP} = 10 s. It then gradually increases and reaches its maximal value of about 35.19% for t_{CP} = 120 s, which is near to that of the polished wafer. The lifetime of minority carriers shows a dramatic decrease from 3.2 μs (t_{CP} = 0 s) to 1.67 μs (t_{CP} = 5 s), and then reaches a value of 1.80 μs for t_{CP} = 10 s, as shown in Fig. 2(b). The reason for the dramatic decrease in the minority carrier lifetime after the CP etching needs further investigation.

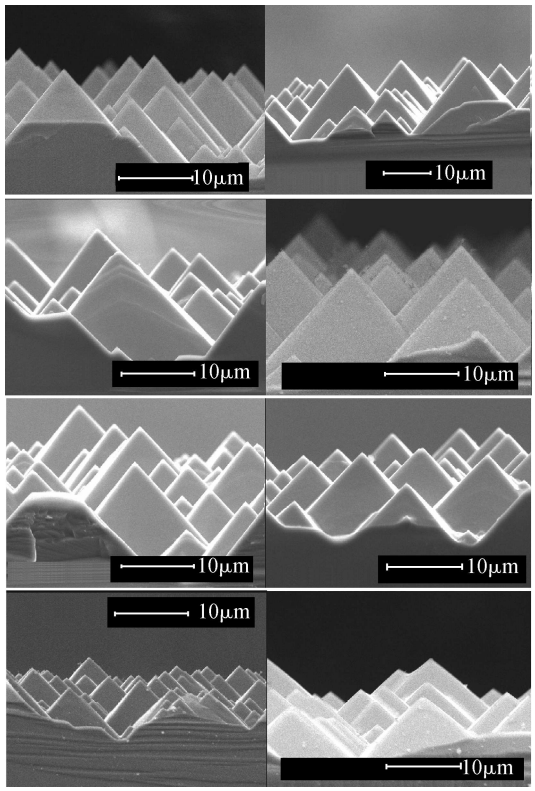

Fig. 1. SEM images of textured wafers. CP etched times are 0, 5, 10, 15, 20, 30, 60, and 120 s, respectively.

Dark *I–V* measurements were undertaken to analyze the electrical properties of the solar cells. The dark current density–voltage characteristics of these solar cells could be fitted according to the following double-diode equation:

$$J = J_{01}\left[\exp\frac{q(V - JR_s)}{n_1 kT} - 1\right] + J_{02}\left[\exp\frac{q(V - JR_s)}{n_2 kT} - 1\right] + \frac{V - JR_s}{R_p}, \quad (1)$$

Table 2. Average angle for the top of pyramid peaks and elemental composition for wafers with different t_{CP}.

t_{CP} (s)	0	5	10	15	20	30	60	120
Average angle (°)	75.52	76.58	78.65	80.31	82.04	82.85	86.35	92.34
O (%)	1.90	3.38	5.21	2.92	1.49	3.48	2.37	3.17
Na (%)	0.63	0.49	0.73	0.73	0.66	0.84	0.66	0.57
Si (%)	97.47	96.13	94.06	96.35	97.85	95.68	96.97	96.36

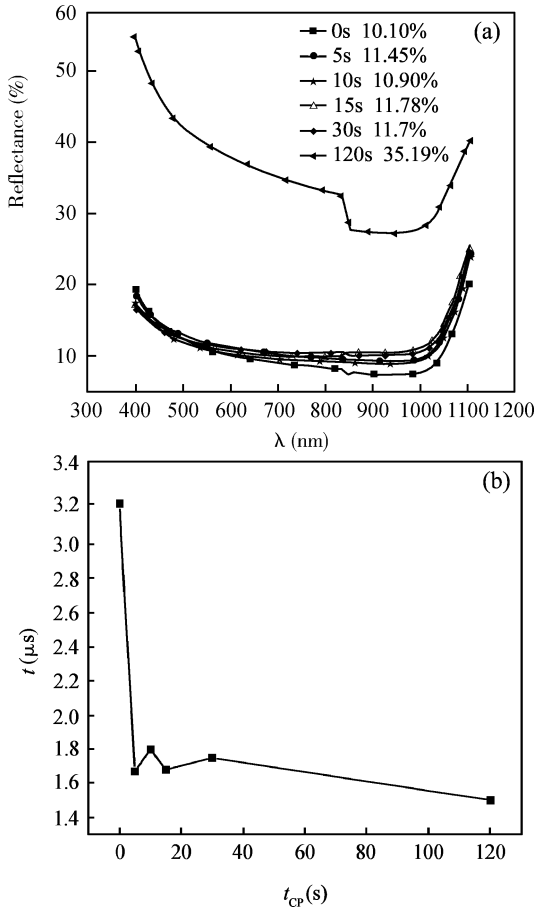

Fig. 2. (a) Reflectance as a function of incident wavelength of textured wafers for different t_{CP}. The percentage numbers are the average reflectance from 400 to 1100 nm; (b) Minority carrier lifetime as a function of t_{CP}.

where J_{01}, J_{02} are the diffusion saturation current density and the generation–recombination saturation current density, n_1, n_2 are the diffusion diode factor and the generation–recombination diode factor, q is the electron charge, k is Boltzmann's constant, T is the temperature, R_s is the series resistance, and R_p is the shunt resistance. The first diode with $n_1 = 1$ expresses the diffusion process within the solar cell at room temperature, whereas the second diode comes to $n_2 = 2$, when the different recombination mechanisms are considered[7]. From the dark I–V curves, we can recognize four different voltage regions (Fig. 3): the first region is given by $V < 0.15$ V: the dark current is mainly determined by the shunt resistance R_p. The second region reaches from 0.15 to 0.45 V: the second term of Eq. (1) (generation–recombination compound) of the total current predominates. The third region

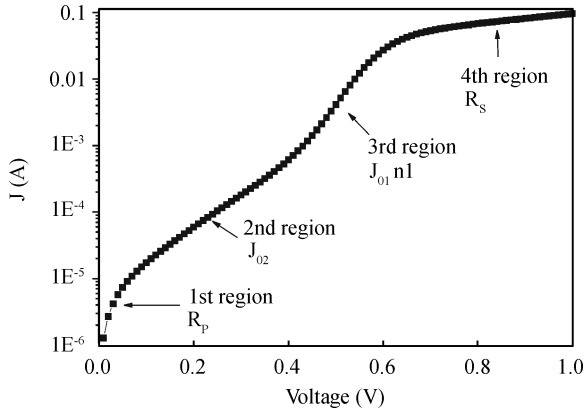

Fig. 3. Dark I–V curve with different regions.

Table 3. Ideality factor n_1, n_2 and saturated current I_{01}, I_{02} versus t_{CP}.

t_{CP} (s)	n_1	n_2	J_{01} (nA)	J_{02} (nA)	R_s (Ω)
0	3.46	3.43	1261	1243	3.83
5	2.03	2.03	343	343	4.85
10	1.73	2.58	61.7	998	2.19
15	1.69	1.85	52.1	122	2.48
20	1.93	1.98	417	462	10.47
30	2.17	2.05	604	480	4.18

is from 0.45 to 0.6 V: the first term in Eq. (1) of the total current (diffusion compound) is dominant. The fourth region extents from 0.6 V and over: the dark current is controlled by the series resistance R_s. So, by the curve fitting method, the parameters of the model can be extracted.

Table 3 shows n_1, n_2, J_{01}, J_{02}, and R_s versus t_{CP}. When t_{CP} = 10–15 s, J_{01} reached relatively lower values (61.7 and 52.1 nA), which is assorted with a relatively higher V_{oc} value (555 and 545 mV). Moreover, t_{CP} affected n_1 and n_2 as well, they became closest to ideality factor values ($n_1 = 1$ and $n_2 = 2$) when t_{CP} = 10–15 s. R_s also became the lowest when t_{CP} = 10–15 s.

Figure 4 shows the performance of solar cells fabricated on the wafers etched for different t_{CP}. When increasing t_{CP}, all parameters of solar cells first in creased and then decreased after $t_{CP} > 20$ s. The optimal t_{CP} is 10–15 s. The highest conversion efficiency of 12.36% is obtained for $t_{CP} = 15$ s.

Some studies have been reported to explain how CP etching affects the performance of solar cells[6, 8]. One explanation of the positive effect on the solar cell properties was that it was due to the removal of Na contamination on the surface of the wafers after CP etching, along with an elemental composition analysis detected by XPS[6]. However, our elemental composition analysis by SEM shows an irregular distribution of Na^+ contamination for the different t_{CP}, listed in Table 2, which cannot support the above explanation in this case. The other explanation for the decrease of the minority carrier lifetime after t_{CP} etching is to do with the exposure of the Si (100) surface and its relative difficulty in achieving a-Si growth[8]. However, a slight angular increase of pyramid peaks (seen in Table 3) seems insufficient to demonstrate the effect of Si (100) expo-

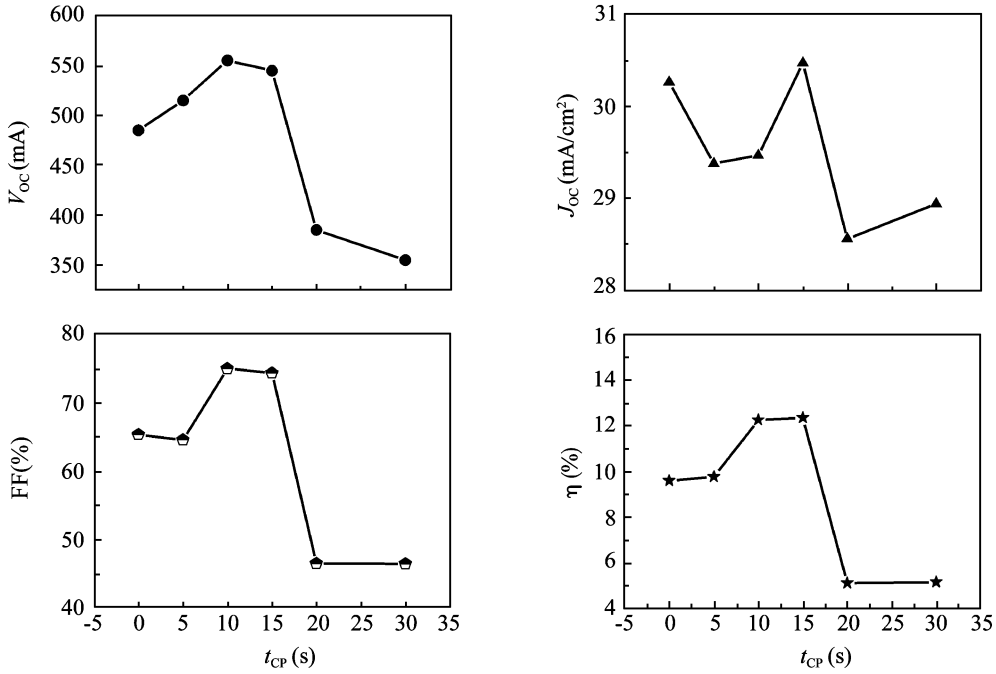

Fig. 4. Solar cell properties, such as V_{oc}, J_{sc}, FF, and η as a function of the CP etching time.

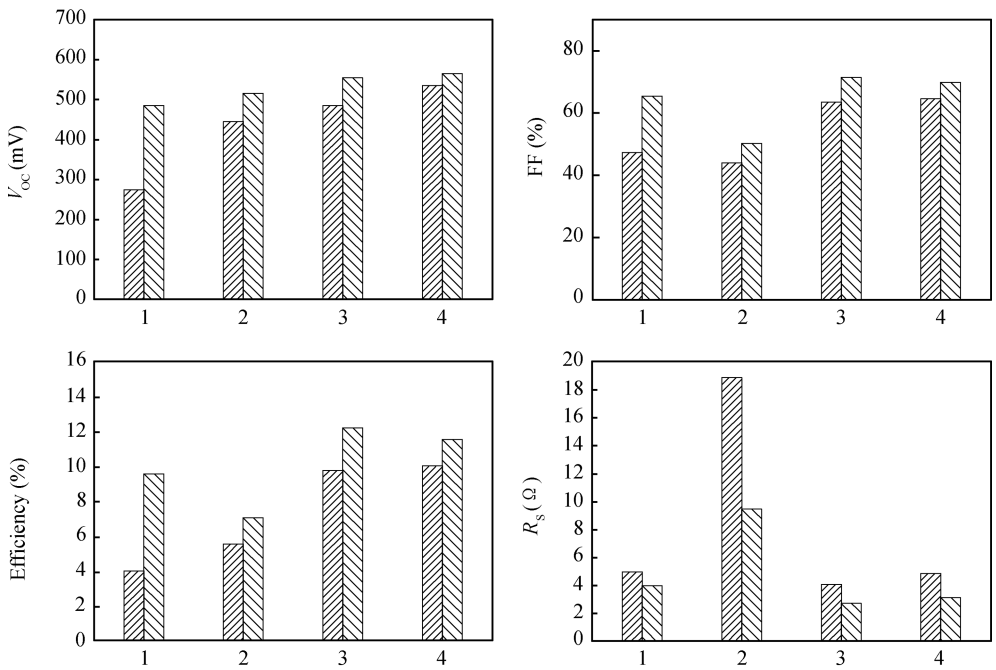

Fig. 5. In each panel, the left bars represent the as-prepared cells, and the right bars represent the annealed ones. Samples 1 and 3 have the same S_{av} of 2 μm, and samples 2 and 4 have a S_{av} of 4 μm. Samples 3 and 4 included 10 s of CP etching before deposition, while samples 1 and 2 did not. Subsequently, all of these samples were fabricated under the same conditions.

sure. Further investigations should be carried out to explain why 10–15 s is the optimal CP etching time.

3.2. Effect of annealing

A low-temperature post annealing process demonstrated a notable beneficial effect on amorphous emitter heterojunction solar cells[6]. In order to study the influence of the annealing process, two control experiment groups were set up. Samples 1, 3 and samples 2, 4 have different average pyramid sizes (S_{av}) of 2 μm and 4 μm, respectively. Samples 3 and 4 were subjected to 10 s of CP treatment before deposition, whereas samples 1 and 2 were not. Subsequently, all of these samples were fabricated under the same conditions.

Figure 5 shows the influence of the annealing process on the performance of solar cells. A considerable improvement of V_{oc}, FF, and η after annealing has been observed. Compared to sample 2, sample 1 shows a greater improvement in V_{oc}, FF, and η, which may indicate that textured silicon wafers with smaller pyramids are more easily improved than bigger ones after annealing. This tendency is also demonstrated by samples 3 and 4. In addition, J_{sc} only displayed a small difference (< 0.9 mA/cm^2) between the annealed ones and the as-prepared

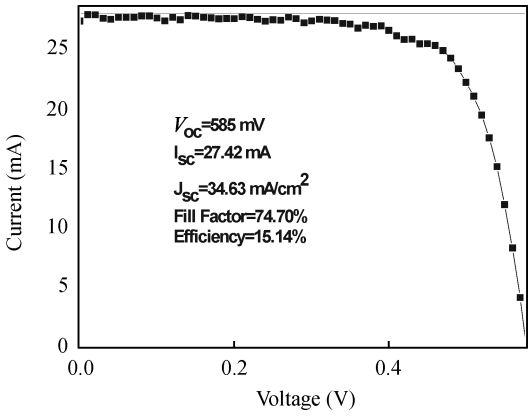

Fig. 6. *J*–*V* curve for the solar cell with the highest conversion efficiency.

ones. Moreover, R_s shows a notable lower value after annealing, due to either restructuring of the deposited film or a better contact by each deposited layer.

3.3. Device results

Using the CP treatment and the post annealing process developed in this study, cells fabricated on p-type Cz substrates under the optimal deposition conditions of each layer have achieved a conversion efficiency of 15.14%, as shown in Fig. 6.

4. Conclusions

In heterojunction solar cells, an appropriate preparation of the wafer surfaces prior to the a-Si deposition and an appropriate low-temperature post annealing makes it possible to achieve an excellent surface passivation. A short CP treatment upon textured p-type Cz crystalline silicon wafers served to smoothen pyramid peaks, hence, improving the deposition coverage and the contact of each layer, which is beneficial to the performance of the solar cells. Low-temperature post annealing processes reduced the series resistance by restructuring the deposited films, hence remarkably improving the performance of the solar cells. After introducing a CP treatment and low-temperature post annealing processes, we obtained optimized solar cells with a conversion efficiency of 15.14%, which is the best value for this type of solar cell reported in China so far.

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