An enhanced close-in phase noise LC-VCO using parasitic V-NPN transistors in a CMOS process*

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Abstract: A differential LC voltage controlled oscillator (VCO) employing parasitic vertical-NPN (V-NPN) transistors as a negative g_m-cell is presented to improve the close-in phase noise. The V-NPN transistors have lower flicker noise compared to MOS transistors. DC and AC characteristics of the V-NPN transistors are measured to facilitate the VCO design. The proposed VCO is implemented in a 0.18 μm CMOS RF/mixed signal process, and the measurement results show the close-in phase noise is improved by 3.5–9.1 dB from 100 Hz to 10 kHz offset compared to that of a similar CMOS VCO. The proposed VCO consumes only 0.41 mA from a 1.5 V power supply.

Key words: close-in phase noise; vertical-NPN; flicker noise; VCO
DOI: 10.1088/1674-4926/30/8/085004 **PACC:** 1230B; 2750D

1. Introduction

The sensitivity of a wireless receiver can be greatly degraded by "reciprocal mixing" or transmitter-to-receiver leakage, which is mainly caused by the phase noise of an oscillator[1]. In a typical phase locked loop (PLL), the voltage controlled oscillate (VCO) close-in phase noise can be filtered out by the close loop transfer function with a reasonably large loop-bandwidth. However, the VCO close-in phase noise would be dominant in an integer PLL because of a relatively small loop bandwidth for narrow band spacing applications, such as the 402–405 MHz medical implant communication service (MICS) and the Japanese personal digital cellular (PDC) band.

A bipolar junction transistor (BJT) has lower flicker noise ($1/f$ noise) than that of a MOS transistor, which is typically fabricated in BiCMOS technology for RF/mixed signal systems. While CMOS technology enables large scale circuit integration with significantly lower cost, it suffers from the $1/f$ noise problem. As verified in several recent studies on vertical NPN (V-NPN) transistors, deep n-well CMOS processes can take advantage of both BJT and MOS transistors[2,3].

In a typical differential LC-VCO, there are two main $1/f$ noise sources contributing to the phase noise. One is the tail current source, and the other is the negative g_m-cell. Some studies have revealed that the tail current source noise is an important contributor to the phase noise, whereas the $1/f$ noise of the g_m-cell does not account for the close-in phase noise[4]. So, Ku *et al.*[2] tried to reduce the close-in phase noise by using a vertical NPN transistor as the tail current source. However, recent research has shown that the phase noise contribution of the tail current source varies with the size of the switching transistor, and the reduction of phase noise in the close-in $1/f^3$ region is fundamentally limited by the $1/f$ noise of the switching transistor[5].

This paper presents a low close-in phase noise LC-VCO which exploits the advantages of V-NPN used as the g_m-cell. Measurement results for the DC and AC characteristics of the V-NPN transistors are shown. VCO circuit designs employing the V-NPN are described, with explanations of the phase noise of the tail current and the cross coupled transistors, and are compared to those of the MOS VCO. The measurement results are discussed in detail.

2. Characterization of the V-NPN

As verified in previous studies[2,6], a parasitic V-NPN with an emitter area of 2×2 μm^2 is fabricated in 0.18 μm CMOS technology. Figure 1 describes the cross-section including the V-NPN, NMOS and PMOS transistors. The latch-up effect in the CMOS process is prevented by techniques such as the deep n-well process and guard-rings with dense contacts to reduce the parasitic resistance[7].

The DC characteristics of the V-NPN measured with a probe station are shown in Fig. 2. The maximum forward current gain (β_F) is about 22 at the bias condition of V_{be} = 0.75 V and V_{ce} = 1 V. High frequency parameters such as the cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) are extracted from the measured S-parameters from 0.1 to 4 GHz. The intrinsic S-parameters are obtained with typical open and short de-embedding test structures. According to the definition, the current gain h_{21} and the unilateral power gain Gu are both measured. As shown in Fig. 3, the measured f_T is 1.1 GHz and f_{MAX} is 2.2 GHz at a collector current of 238 μA. Also, the relationship between f_T and I_c is measured in Fig. 4, which implies that the maximum f_T (mainly limited by the base width of the V-NPN) is 1.13 GHz at a collector current of 1 mA corresponding to a base transit time (τ) of about 139 ps.

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Received 16 January 2009, revised manuscript received 25 March 2009

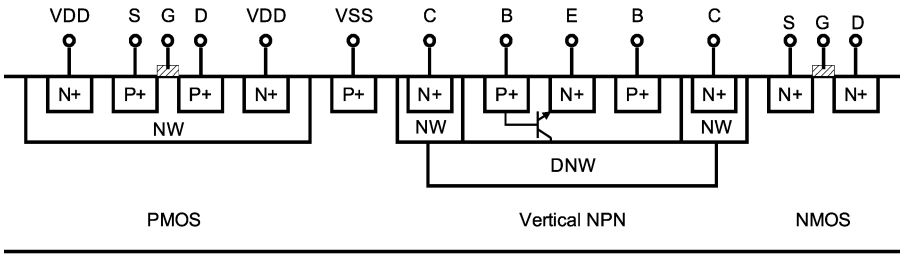

Fig. 1. Cross-section view of vertical NPN in the CMOS process.

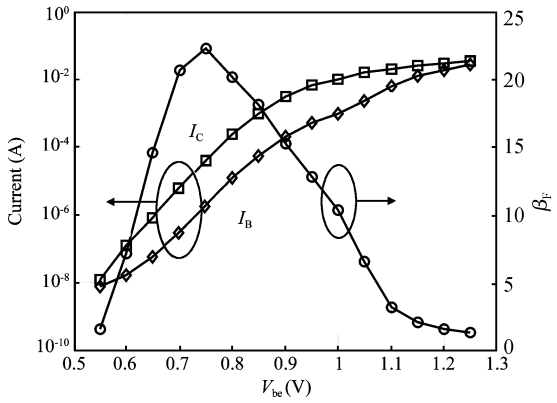

Fig. 2. Measured DC characteristics of the V-NPN at V_{ce} = 1 V.

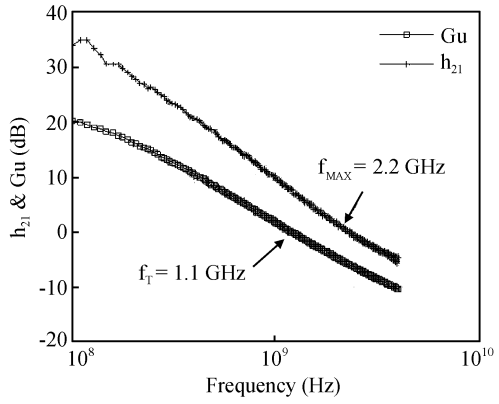

Fig. 3. Measured f_T and f_{MAX} of the V-NPN at I_c = 238 μA.

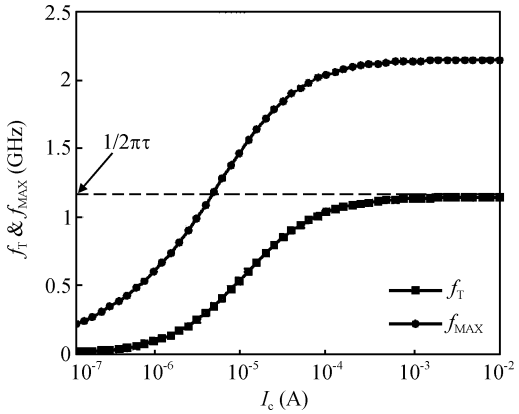

Fig. 4. Measured f_T and f_{MAX} at different collector currents I_c.

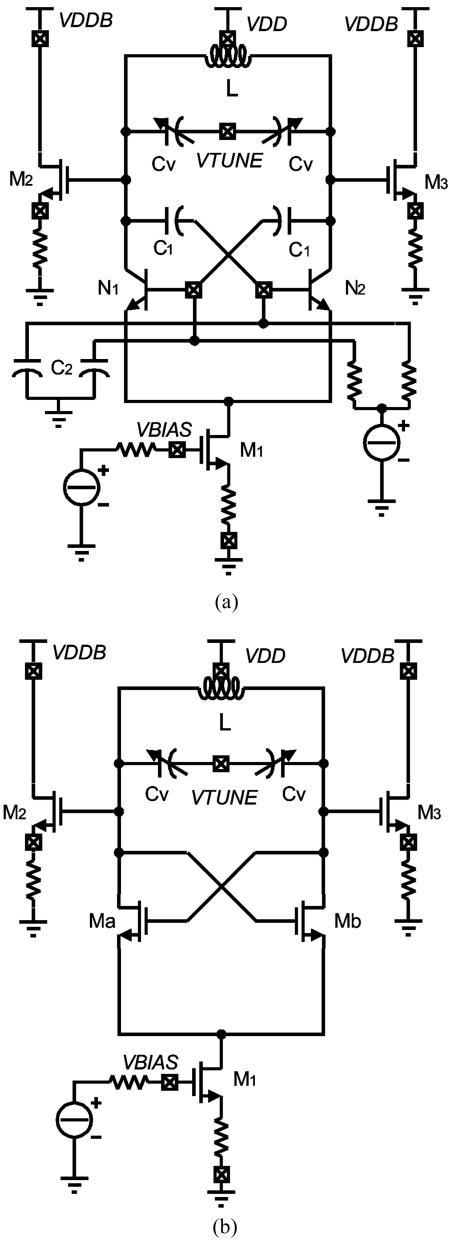

Fig. 5. (a) Proposed VCO using V-NPN transistors as a negative g_m-cell; (b) Typical VCO using MOSFET as a negative g_m-cell.

3. VCO design

3.1. Impact of 1/*f* noise on the phase noise

Intrinsic $1/f$ noise up-conversion is considered to be the main reason for the phase noise in $1/f^3$ region, which can be summarized as the dependence of two main parameters, i.e. one is the magnitude of the $1/f$ noise and the other is the up-conversion factor.

For a typical LC-VCO, as shown in Fig. 5(b), the $1/f$ noise of the tail current transistor is up-converted by modulating the tuning varactors (AM-PM conversion) and the cross coupled transistors. The former can be reduced by minimiz-

ing the varactor sensitivity with tuning range compensated by adding an array of digital switchable capacitors. The latter can be improved by increasing the linearity of the cross coupled transistors[5]. Therefore, the $1/f$ noise up-conversion of the tail current transistor can be minimized. The switching transistors or varactors can be tailored to minimize the up-conversion factor and the bias transistors can be properly sized to reduce the magnitude of flicker noise simultaneously independently of each other.

With respect to the $1/f$ noise up-conversion of the cross coupled transistors, both the magnitude and the up-conversion factor of its $1/f$ noise are all ascribed to the switching transistor itself. Although increasing the MOS device area can reduce the $1/f$ noise of the gm-cell, it deteriorates the up-conversion factor, which makes the gm-cell design more complicated and hard to trade off.

3.2. Circuit implementation

Here, V-NPN transistors in the CMOS process are used as the differential pair of a LC-VCO to address the problems above. Since the intrinsic $1/f$ noise of a V-NPN expressed by Eq. (2) is usually much smaller than that of a MOS device in Eq. (1), the magnitude of $1/f$ noise is greatly reduced disregarding the switching transistor size, and the close-in phase noise can thus be improved. Furthermore, design trade offs on sizing the cross coupled transistors can also be eliminated.

$$v^2_{\text{in},1/f,\text{MOS}} = \frac{K_{\text{f,MOS}}}{WLC_{\text{OX}}f}, \tag{1}$$

$$v^2_{\text{in},1/f,\text{VNPN}} = \frac{K_{\text{f,VNPN}}}{f}. \tag{2}$$

In order to verify this idea, two VCOs are designed in 0.18-μm CMOS RF/mixed signal technology. As shown in Figs. 5(a) and 5(b), a fully differential cross coupled topology with a source degenerated resistor is employed for better noise performance, and source followers are used for output match.

The phase noise of a VCO is basically related to several key parameters[8], including the voltage swing A_{o}, the tank impedance at resonance Req, the tank quality factor Q, the excess noise factor F, the corner frequency of the circuit noise $\Delta f_{1/f^3}$, and the oscillation frequency f_{o}, as shown in Eq. (3),

$$L(f_{\text{m}}) = \frac{2kTR_{\text{eq}}F}{A_{\text{o}}^2}\left(\frac{f_0}{2Qf_{\text{m}}}\right)^2\left(1+\frac{\Delta f_{1/f^3}}{f_{\text{m}}}\right). \tag{3}$$

For the sake of a fair and reasonable comparison, the same bias and tank circuits are designed. To enhance the comparison of the close-in phase noise, the $1/f^2$ region phase noise is minimized in both cases according to the sizing techniques[5], and the $1/f^3$ region phase noise is also optimized for the typical MOS topology in the following ways. First, for both topologies, a small current of 0.41 mA is chosen to reduce the frequency shift effect[9] and thermal noise in both the tail current transistor and the cross coupled transistors. The length of the tail current transistor size is increased in both VCOs for lower flicker noise. The width of the MOS cross coupled transistor is minimized almost to the limitation of the oscillation condition to suppress the $1/f$ noise up-conversion factor, and its length is increased to reduce the flicker noise while not degrading f_{T} so much. Varactors of small value are also employed to minimize the tuning sensitivity.

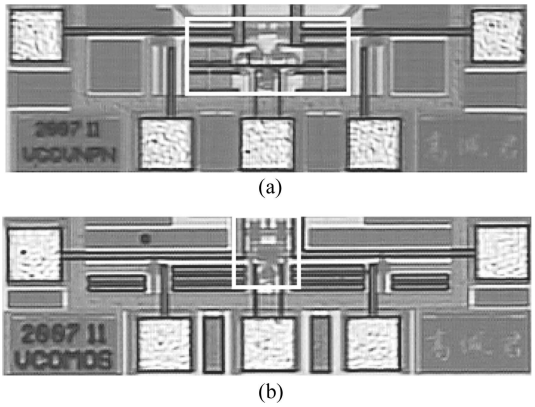

Fig. 6. Chip microphotograph of (a) V-NPN VCO and (b) MOS VCO.

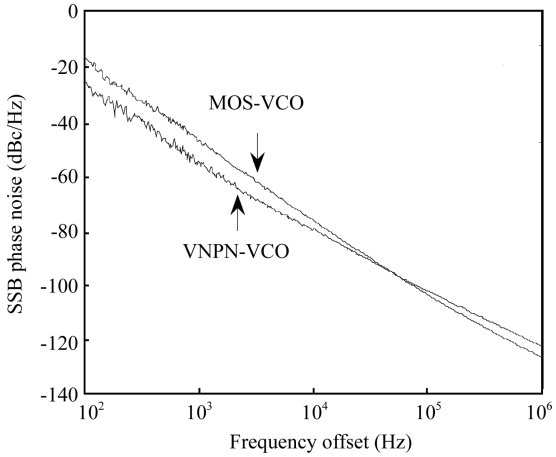

Fig. 7. Measured phase noise of the proposed V-NPN VCO compared to that of the MOS VCO.

4. Measurement results and discussion

In order to minimize the process effect, both MOS and V-NPN VCOs are implemented on the same wafer. Figure 6 shows a fabricated microphotograph with a core area of 100 $\times$ 100 μm^2 and 200 $\times$ 100 μm^2 each (without pad). The VCO core draws 0.41 mA from a 1.5 V supply. The measurement was performed on an E5052A signal source analyzer, with off chip inductors of 39 nH (Q = 46). The phase noise of the proposed V-NPN VCO is shown in Fig. 7 compared to that of the MOS VCO. The $1/f$ noise corner of the V-NPN VCO is just about 30 kHz, which is lower than the MOS VCO. The close-in phase noise of the V-NPN VCO is improved by 3.5–9.1 dB from 100 Hz to 10 kHz compared to that of its MOS counterpart. Under a varactor value of 500 fF to 1 pF, the V-NPN VCO presents a tuning sensitivity of 12 MHz/V at a differential output power of –8 dBm, where the single end output spectrum is shown in Fig. 8. The complete performance comparison is summarized in Table 1. The phase noise of the V-NPN VCO is improved by 3.5–9.1 dB from 100 Hz to 10 kHz offset compared to that of a similar CMOS VCO.

Table 1. Performance summary of MOS and V-NPN VCOs.

VCO	f_o (MHz)	P_{DC} (mW)	K_{VCO} (MHz/V)	P_{out} (dBm)	Phase noise (dBc/Hz)		
					100 Hz	1 kHz	10 kHz
MOSVCO	537	0.615	10	–7	–17.3	–47.7	–76.6
V-NPNVCO	545	0.615	12	–8	–26.4	–55.4	–80.1

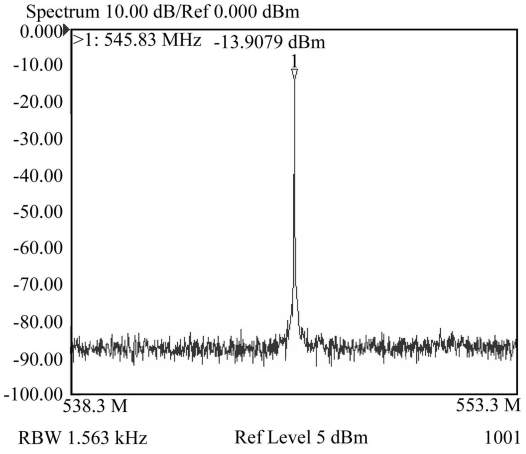

Fig. 8. Measured single-end output spectrum of V-NPN VCO.

However, the V-NPN VCO behaves a little worse than that of the MOS VCO at higher frequency offsets. This is primarily because the thermal noise of the cross coupled transistors, owing to an un-optimized layout on the base resistance, increases the noise level of the $1/f^2$ region. Layout techniques such as Inter-digital can be used to reduce the parasitic resistance of the base.

Furthermore, better $1/f^3$ region phase noise can be achieved if the V-NPN has higher f_T, which implies a better linearity of the negative gm cell, and as a result, reduces the up-conversion factor. The characteristic frequency of the V-NPN can be improved by either decreasing the base width or using some doping techniques in the process aspect, which can also extend its applications to higher frequencies.

Targeted for close-in phase noise reduction, a VCO using V-NPN transistors as its negative gm-cell is proposed in this paper. The measurement results show that the V-NPN VCO has enhanced phase noise of 3.5–9.1 dB compared to the MOS VCO from a 100 Hz to10 kHz frequency offset. The idea that the reduction of phase noise in the close-in $1/f^3$ region is fundamentally limited by the $1/f$ noise of the g_m-cell of the phase noise is also verified.

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