

An offset-insensitive switched-capacitor bandgap reference with continuous output*

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Abstract: An improved switched-capacitor bandgap reference with a continuous output voltage of 1.26 V has been implemented with Chartered 0.35- μm 5-V CMOS process. The output offset voltage, induced by non-ideal characteristics of operational amplifier and bias current generator, is suppressed by the proposed sample-and-hold circuit and self-bias technique. Experimental results show that the proposed circuit operates properly under a supply voltage varying from 3 to 5 V. The measured temperature coefficient is 112 ppm/ $^{\circ}\text{C}$ and the power supply rejection ratio of output voltage without any filtering capacitor is -40 dB and -33 dB at 100 Hz and 10 MHz, respectively.

Key words: bandgap reference; switched-capacitor; offset; self-bias; continuous output

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1. Introduction

Voltage reference is a ubiquitous block in modern mixed-signal systems, such as data converters, to provide a stable DC voltage insensitive to the variations of supply voltage and temperature. With the ever-increasing precision of data converters, the robust demand for low-offset voltage reference keeps growing. Conventional BJT-based bandgap reference (BGR)^[1], unfortunately, suffers from offset voltage resulting from asymmetry of the amplifier and mismatch between BJTs. This problem can be alleviated by enlarging the area of the amplifier input MOSTs pair^[2] or by some trimming circuits^[3,4]. These compensation techniques work to some extent, although they increase the circuit complexity and cost. Still, the mismatch between BJTs cannot be eliminated.

The switched-capacitor bandgap reference (SCBGR) with single BJT^[5-7] has been presented to minimize the harmful influence of amplifier offset voltage. Obviously, mismatch between BJTs is no longer a problem since only one BJT is adopted. However, output deviation due to imprecise bias current still exists and the non-continuous output limits its applications in continuous-signal systems.

In this paper, an improved SCBGR with continuous output is presented. A novel self-bias technique is adopted to dramatically reduce the offset sensitivity.

2. Conventional BGR

Figure 1 shows the typical structure of a conventional BGR^[8]. The output voltage (V_{out}) can be written as Eq. (1):

$$V_{\text{out}} = V_{\text{EB2}} + (1+k)V_T \ln n - (1+k)V_{\text{os1}}, \quad (1)$$

where n is the emitter area ratio between Q_2 and Q_1 , and V_{os1} represents the amplifier input offset voltage. Temperature compensation can be achieved by properly selecting k and n .

However, as illustrated by the last term in Eq. (1), V_{os1} is amplified by a factor of $1+k$, typically about 10, which causes V_{out} to deviate greatly.

3. Conventional SCBGR

In order to eliminate the impact of V_{os1} , a single-BJT SCBGR has been presented in Ref. [5], as shown in the right block of Fig. 2, where S_1 and S_2 are driven by non-overlapping clocks^[9].

In the first phase (ϕ_1), bias current I_1 flows through Q_1 to generate an emitter-base voltage V_{EB1} and the output voltage V_{out1} is given by

$$V_{\text{out1}} = V_{\text{EB1}} - V_{\text{os1}} = V_T \ln \frac{I_1}{I_S} - V_{\text{os1}}. \quad (2)$$

During the second phase (ϕ_2), an additional current I_2 , together with I_1 , flows through Q_1 and the emitter-base voltage V_{EB2}

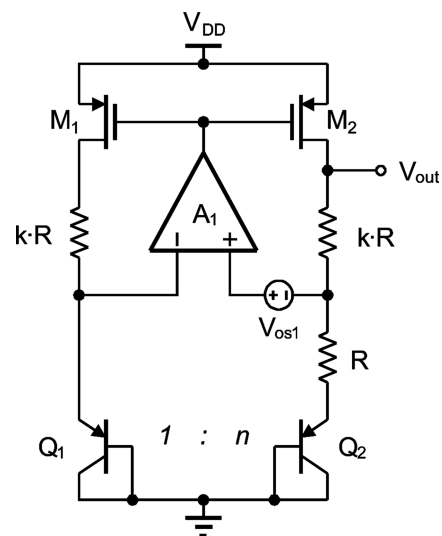


Fig. 1. Conventional BGR.

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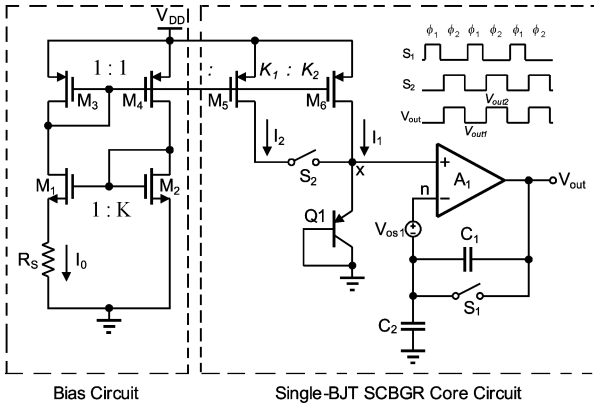


Fig. 2. Single-BJT SCBGR.

can be found again as:

$$V_{EB2} = V_T \ln \frac{I_1 + I_2}{I_S}. \quad (3)$$

Assuming $I_1 = K_1 I_0$ and $I_2 = K_2 I_0$, thanks to the proportional amplifier consisting of C_1 , C_2 , and A_1 , the desired output reference voltage V_{out2} is produced:

$$V_{out2} = V_T \ln \left[(K_1 + K_2) \frac{I_0}{I_S} \right] + V_T \frac{C_2}{C_1} \ln \left(1 + \frac{K_2}{K_1} \right) - V_{os1}. \quad (4)$$

It can be easily seen that the output offset voltage (V_{os1}) of SCBGR is reduced by $1 + k$ times compared with that of conventional BGR in Eq. (1).

Additionally, the accuracy of V_{out2} is also affected by the absolute value of I_0 . Assume a conventional bias current generator is applied, as shown in the left block in Fig. 2. Let us consider the expression of I_0 ^[2]:

$$I_0 = \frac{2}{\mu_n C_{ox} (W/L)_N} \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}} \right)^2, \quad (5)$$

where $(W/L)_N$ is the aspect ratio of M_1 . Practically, a great deviation, possibly as large as 20%, may be introduced to the value of R_S during the CMOS manufacturing process. Assume $R_S = (1 + \varepsilon)R_{S0}$, where R_{S0} and ε is the designed value and the deviation percentage of R_S respectively, and substitute it into Eq. (5), then Equation (4) can be rewritten as:

$$V_{out2} = V_T \ln \left[(K_1 + K_2) \frac{I_0}{I_S} \right] + V_T \frac{C_2}{C_1} \ln \left(1 + \frac{K_2}{K_1} \right) - V_{os1} - 2V_T \ln(1 + \varepsilon). \quad (6)$$

This shows that an extra offset voltage of $2V_T \ln(1 + \varepsilon)$ is added. Even so, the total offset voltage is always much smaller than that of the conventional BGR.

Unfortunately, this SCBGR cannot generate a constant DC reference voltage, which greatly limits its application.

4. Improved SCBGR

For the purposes of obtaining a continuous output voltage and reducing the offset voltage caused by the bias circuit, an improved SCBGR is proposed, as shown in Fig. 3, which

consists of a sample-and-hold (S/H) circuit, a self-bias circuit, and a conventional SCBGR core circuit.

4.1. S/H circuit

The output voltage of the conventional SCBGR (V_0) is converted to a continuous voltage (V_{out}) through an S/H circuit. As described in the right block of Fig. 3, switch S_3 samples the designed voltage (V_{out2}) during ϕ_2 . The sampling capacitor C_3 should be chosen adequately such that the stability and speed of amplifier A_1 deteriorate slightly.

The ripple voltage on V_1 is further suppressed by a simple low-pass-filter (LPF) consisting of R_f and C_4 . It is notable that the LFP bandwidth should be set much smaller than the clock frequency. In this design, a 10 M Ω high-resistance poly resistor R_f and a 10 pF MOS capacitor C_4 are chosen to accomplish this.

4.2. Self-bias circuit

A novel self-bias technique is exploited to reduce the output offset voltage arising from resistor deviation in the conventional SCBGR. As shown in the left block of Fig. 3, the bias current I_0 is generated by V_{out} through a typical voltage-to-current convertor. Taking all the error sources (V_{os1} , V_{os2} , and ε of R_S) into account, we can write the output reference voltage V_{out} as:

$$V_{out} = V_T \ln \left[(K_1 + K_2) \frac{I_0}{I_S} \right] + V_T \frac{C_2}{C_1} \ln \left(1 + \frac{K_2}{K_1} \right) - V_{os1} - V_T \ln(1 + \varepsilon) + V_T \ln \left(1 + \frac{V_{os2}}{V_{out}} \right). \quad (7)$$

Since V_{os2} is usually several mV while V_{out} is 1.26 V in this design, the last term in Eq. (7) is always negligible. Consequently, the total output offset voltage is reduced by $V_T \ln(1 + \varepsilon)$ compared with that of SCBGR in Eq. (6). In other words, the offset voltage due to the bias current deviation is halved. Moreover, from Eq. (5) we can see that the bias current I_0 in the conventional SCBGR suffers from variations in technology parameters, such as μ_n and C_{ox} , while in this design, thanks to the self-bias circuit, I_0 equals V_{out}/R_S and is independent of them.

4.3. Amplifier design

A high-gain fast-settling folded-cascode amplifier A_1 , as shown in Fig. 4, is designed to reduce the systemic offset and obtain a high accuracy V_0 . The core circuit of A_1 consists of M_{16} – M_{26} . The area of M_{17} – M_{18} should be appropriately enlarged to decrease the input offset voltage. A start-up circuit formed by M_1 – M_7 is necessarily utilized to prevent the bias circuit from reaching zero-current state. When $EN = 0$, M_5 is turned on to pull P-node up to V_{DD} . Thus, the whole circuit is shut down. When EN is set to V_{DD} , the start-up circuit pulls P-node to ground through M_6 and M_7 for a short period to activate the amplifier.

The same structure is chosen for amplifier A_2 in the self-bias circuit to simplify the design. The gain bandwidth product

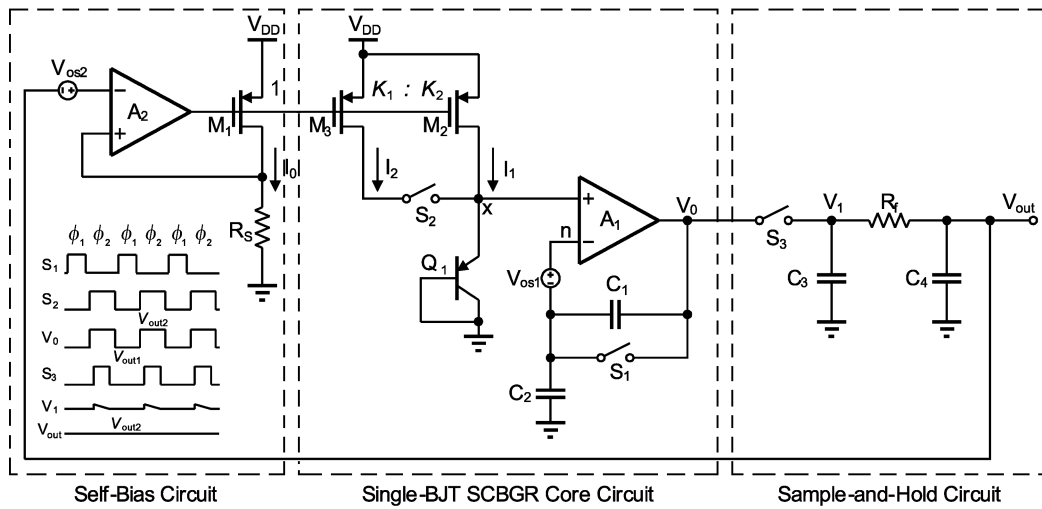


Fig. 3. Structure of the improved SCBGR.

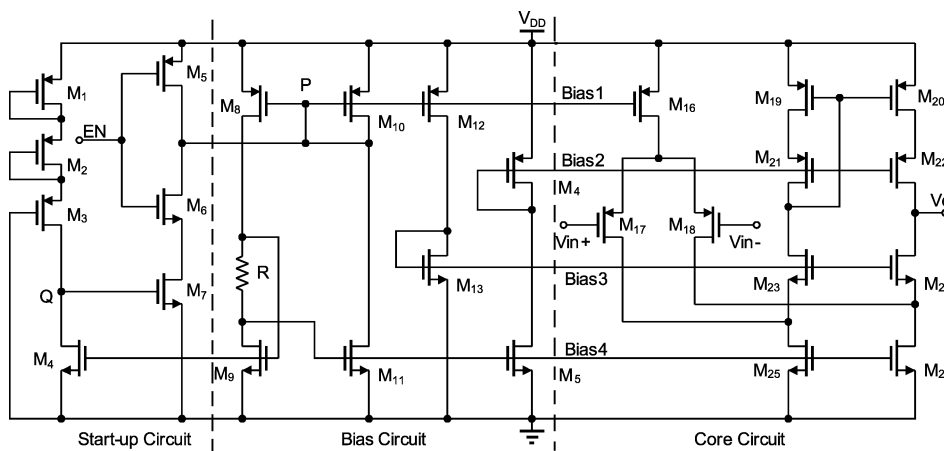


Fig. 4. Structure of amplifiers A₁ and A₂.

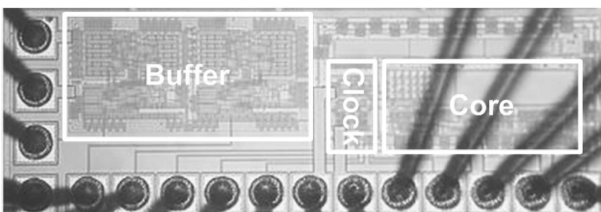


Fig. 5. Die photo of prototype chip.

of A₂, however, can be designed to be much lower since the input of A₂ is constant and no settling requirement is needed. As a result, the proposed self-bias circuit consumes nearly the same power as the conventional bias current generator does but improves the accuracy greatly.

5. Experimental results

The proposed SCBGR has been fabricated with Chartered 0.35- μm 1P4M 5-V CMOS process. The die photo is shown in Fig. 5. Careful matching, particularly of the current source MOSTs M₁–M₃ and capacitors C₁–C₂ in Fig. 3, should be carried out during the layout design to enhance the output precision. In order to prevent the digital part from affecting the analog core circuit, both the non-overlapping clock generator and the SCBGR core circuit are surrounded by guard rings.

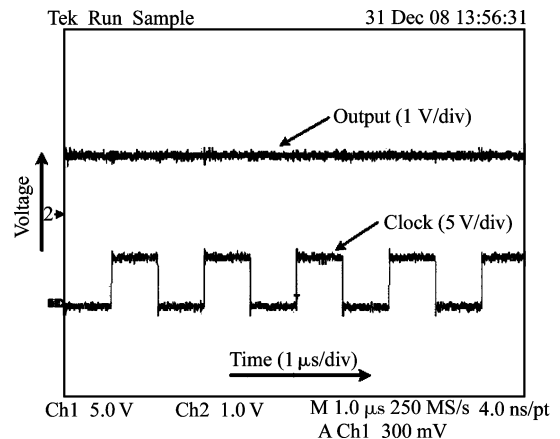


Fig. 6. Waveforms of output and system clock.

In addition, a voltage buffer with class-AB output stage is applied to drive the test instruments. The chip area excluding the output buffer is 0.048 mm².

The output waveforms of this chip and the input clock signal are shown in Fig. 6. We can see that a constant output reference voltage of 1.26 V is generated with a 500 kHz clock signal. The measured temperature characteristic of output voltage under three different supply voltages with a temperature range of 20 to 100 °C is shown in Fig. 7 and the minimal

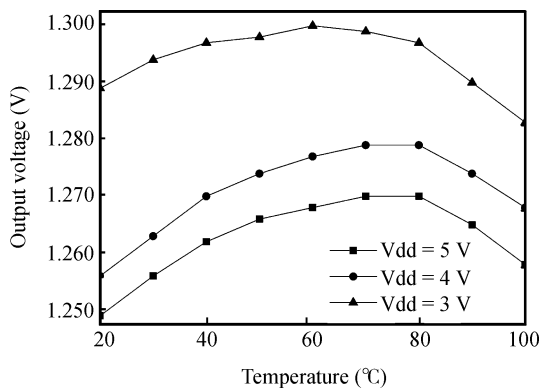


Fig. 7. Temperature performance under different power supplies.

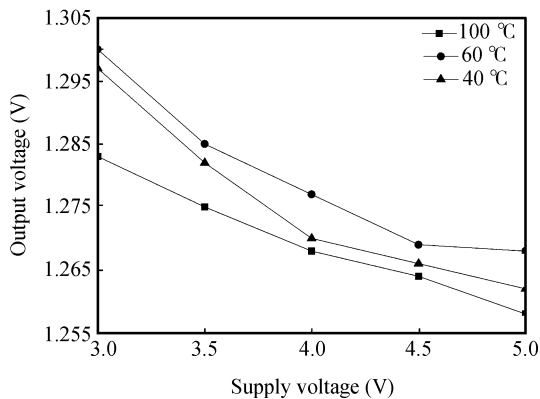


Fig. 8. Measured supply sensitivity results at different temperatures.

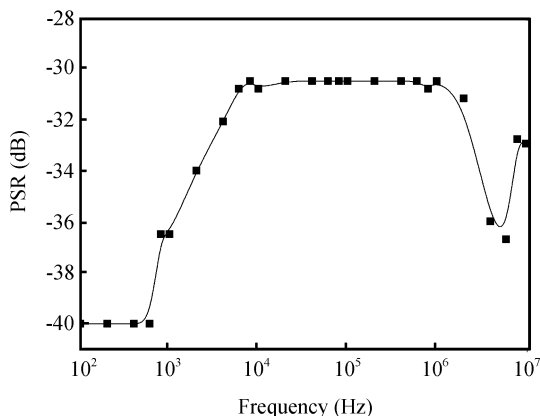


Fig. 9. Measured PSR of the proposed SCBGR.

temperature coefficient (TC) is 112 ppm/°C at $V_{DD} = 3$ V without any trimming schemes. The large TC may arise from nonideal S_3 and variation of R_f with temperature. Figure 8 shows the experimental supply sensitivity results of output voltage V_{out} at different temperatures. When the supply voltage changes from 3 to 5 V, the minimal variation of the proposed SCBGR output is 25 mV at 100 °C, which means a line regulation of 0.98%/V. The measured PSR of the proposed SCBGR without any filter capacitors at room temperature, as shown in Fig. 9, is -40 dB at 100 Hz and is still less than -30 dB with a frequency up to 10 MHz, which is comparable with the conventional BGR. Stability is a key consideration in the design of the two amplifiers. Since the gain bandwidth prod-

Table 1. Measured performance summary.

Performance	Value
Technology	0.35- μ m CMOS
Supply voltage	3 to 5 V
Supply current	34 μ A
Output voltage	1.26 V
TC	112 ppm/°C
Line sensitivity	0.98%/V
PSR	-40 dB @ 100 Hz, -33 dB @ 10 MHz
Die area	0.048 mm ²

uct (GBW) and phase margin of amplifier may be easily influenced by variations of process parameters, adequate head-room must be provided during design, which increases the bias current. The total current draw of this design is 34 μ A. The summary of the measured performances which are close to the simulation results is given in Table 1.

6. Conclusions

An improved switched-capacitor bandgap reference has been presented. Thanks to the proposed sample-and-hold circuit and self-bias technique, a stable output voltage of 1.26 V is generated and the output offset voltage is greatly suppressed. The measured temperature coefficient is 112 ppm/°C, and the power supply rejection ratio of output voltage without any filtering capacitor is -40 dB and -33 dB at 100 Hz and 10 MHz.

References

- [1] Gray P R, Hurst P J, Lewis S H, et al. Analysis and design of analog integrated circuits. New York: John Wiley & Sons, 2003
- [2] Razavi B. Design of analog CMOS integrated circuits. New York: McGraw Hill, 2001
- [3] Ceekala V G, Lewicki L D, Wieser J B, et al. A method for reducing the effects of random mismatches in CMOS bandgap references. ISSCC, 2002, 1: 392
- [4] Ruzza S, Dallago E, Venchi G, et al. An offset compensation technique for bandgap voltage reference in CMOS technology. ISCAS, 2008: 2226
- [5] Gilbert B, Shu S. Switching bandgap voltage reference. USA Patent, 1996, 5563504
- [6] Gregorie B R. Switched capacitor voltage reference circuits using transconductance circuit to generate reference voltage. USA Patent, 2004, 6819163
- [7] Gregorie B R. A compact switched-capacitor regulated charge pump power supply. IEEE J Solid-State Circuits, 2006, 41(8): 1944
- [8] Michejda J, Kim S K. A precision CMOS bandgap reference. IEEE J Solid-State Circuits, 1984, 19(6): 1014
- [9] Khan Q A, Wadhwa S K, Misri K. A low voltage switched-capacitor current reference circuit with low dependence on process, voltage and temperature. Proceedings of the 16th International Conference on VLSI Design, 2003: 504