An asymmetric MOSFET-C band-pass filter with on-chip charge pump auto-tuning

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Abstract: An asymmetric MOSFET-C band-pass filter (BPF) with on chip charge pump auto-tuning is presented. It is implemented in UMC (United Manufacturing Corporation) 0.18 μm CMOS process technology. The filter system with auto-tuning uses a master-slave technique for continuous tuning in which the charge pump outputs 2.663 V, much higher than the power supply voltage, to improve the linearity of the filter. The main filter with third order low-pass and second order high-pass properties is an asymmetric band-pass filter with bandwidth of 2.730–5.340 MHz. The in-band third order harmonic input intercept point (IIP_3) is 16.621 dBm, with 50 Ω as the source impedance. The input referred noise is about 47.455 μV_{rms}. The main filter dissipates 3.528 mW while the auto-tuning system dissipates 2.412 mW from a 1.8 V power supply. The filter with the auto-tuning system occupies 0.592 mm^2 and it can be utilized in GPS (global positioning system) and Bluetooth systems.

Key words: MOSFET-C filter; auto tuning; charge pump; CMOS circuit design; wireless system
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1. Introduction

In wireless chip systems, analog integrated filters are often required to reject neighboring channel interferers. On some occasions, the neighboring channel interferers are several tens of decibels higher than the desired signals[1]. So the integrated filter must have a precise cutoff frequency. As we all know, large tolerances due to fabrication processes, temperature variation and aging need to be corrected or compensated. So an auto-tuning circuit for calibrating the RC or Gm–C time constants is indispensable on many occasions.

Generally speaking, two kinds of on-chip tuning methods are to be chosen[2]: direct and indirect. For the former, the circuits used for tuning and for signal processing are the same, while for the latter two matched circuits are needed; one of them is tuned, and the tuning parameters are conveyed to the other, which processes the signal. The latter method is the so-called master-slave technique. The direct tuning method is often used in the application of filtering for which the input signal is only needed part of the time[3]. Besides, direct tuning needs many switches for fast switching which results in spurs in the waveforms. So we choose the master-slave technique for the auto-tuning. Although the active RC filter has excellent linearity, it is limited by the discrete tuning in which the cutoff frequency is tuned digitally with capacitor or resistor matrices using MOSFET switches. As well as the appearance of spurs in the waveform, the tuning accuracy is limited by the discrete quantization errors of the matrices. Compared with discrete tuning, charge pump continuous tuning is chosen for its precise tuning accuracy.

Here we choose an asymmetric MOSFET-C BPF for three reasons. Firstly, as we all know, the MOSFET resistors in a MOSFET-C filter all work in the triode region. $1/f$ noise is absent in the triode-operated MOSFET resistors. Secondly, the asymmetric BPF left stop-band can attenuate the $1/f$ noise further with optimal power consumption and chip area. Thirdly, the large dynamic range in the MOSFET-C filter compared to the Gm–C alternative is also preferable. Besides, the MOSFET-C filter has good linearity if properly designed.

2. Architecture

The main filter in Fig. 1 of the BPF is an asymmetric band-pass filter with third order low-pass and second order high-pass properties, although a third order symmetric BPF which can easily be synthesized from software can also accommodate the specifications of the application. The proposed filter needs 5 op amps (operational amplifier) while the symmetric third BPF needs 6 op amps to accommodate the filter specifications. So the asymmetric BPF is efficient in both

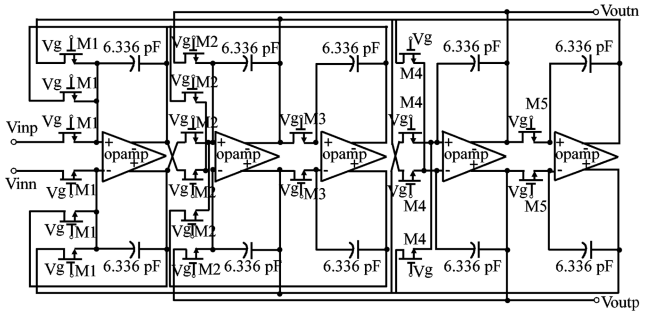

Fig. 1. Main filter of the asymmetric BPF.

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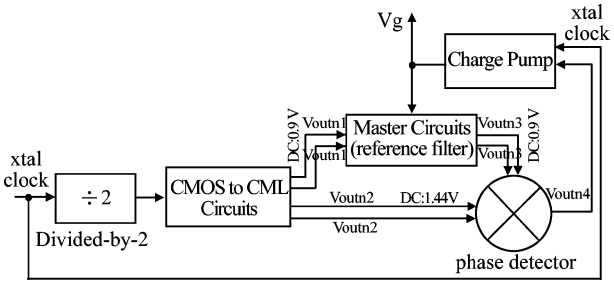

Fig. 2. Charge pump based auto-tuning architecture.

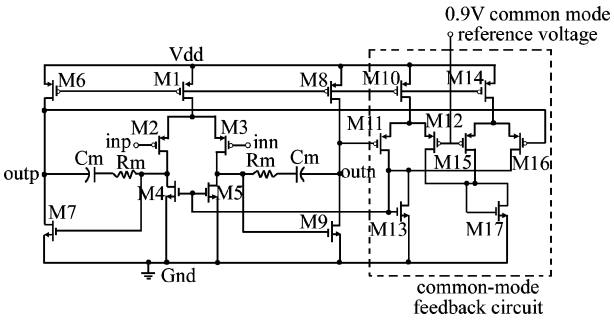

Fig. 3. Schematic of the differential operational amplifier circuit.

area and power consumption. The auto-tuning circuit which is shown in Fig. 2 consists of a divided-by-2 circuit, a CMOS to CML circuit, a reference filter, a phase detector and a charge pump.

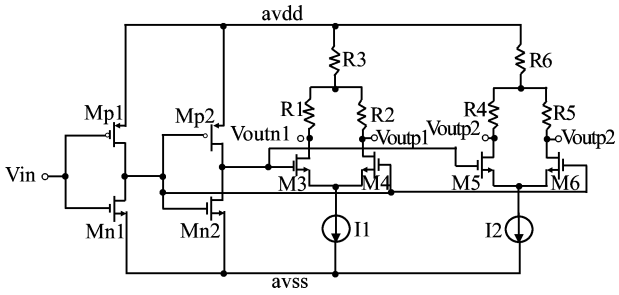

Fig. 4. Schematic of the CMOS to CML circuit.

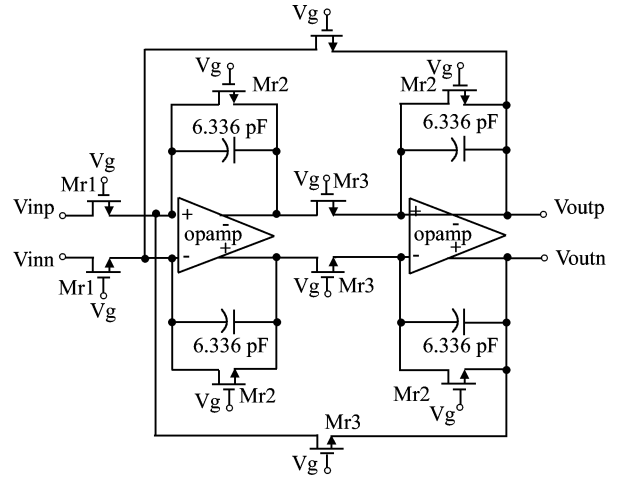

Fig. 5. Reference filter circuit.

3. Circuit design and implementation

3.1. Operational amplifier circuit

Figure 3 shows the schematic diagram of the fully differential op amp circuit employed in the main filter[4]. In order to provide a differential signal with a common-mode voltage, a common-mode feedback circuit is used. The common-mode voltage is set to around 0.9 V by means of the common-mode reference voltage. The total current drain of the op amp is 350 μA, and its gain-bandwidth product is approximately 400 MHz, which means about 40 dB of gain at the center frequency of 4 MHz. Because the Q factor of the poles in the filter is low[5], this simple low-current op amp meets the requirements. In the op amp circuit figure, $R_{\rm m}$ and $C_{\rm m}$ are the Miller compensation resistor and capacitor which are used to strengthen the stability of the op amp.

3.2. Main filter circuit

In Fig. 1, the MOS transistors M1–M5 are all working in the triode region with the same channel length and have proportional matched widths[5]. In the layout of the main filter, the dummy transistors are all placed around the triode-region transistors to ensure better matching properties. The gates of the triode-region transistors are all linked to the same voltage $V_{\rm g}$ which is generated from the charge pump circuit. In order to make these transistors work in the deep triode region, $V_{\rm g}$ needs to be raised to be 2.663 V, much higher than the 1.8 V supply voltage. The channel length is chosen to be 4 μm to avoid channel modulation effects and have a better matching property. In addition, transistors which possess low threshold voltage and high breakdown properties in the UMC process are chosen to realize the MOSFET resistors. As the main filter has main poles of low Q factors and low center frequency (4.035 MHz center frequency), Q tuning for the BPF is unnecessary[5]. In other words, the center frequency can be tuned to the desired frequency without obviously changing the bandwidth.

3.3. CMOS to CML circuit

The CMOS to CML circuit in Fig. 4 is used to provide two groups of differential voltages with different common mode voltages. In Fig. 2, $V_{\rm outp1}$ and $V_{\rm outn1}$ are differential with common mode voltage 0.900 V suitable for the reference filter. $V_{\rm outp2}$ and $V_{\rm outn2}$ are differential with 1.44 V common mode voltage provided for $V_{\rm inp}$ and $V_{\rm inn}$ in the phase detector in Fig. 6. Then the reference filter circuit outputs $V_{\rm outp3}$ and $V_{\rm outn3}$ are provided for the $V_{\rm conp}$ and $V_{\rm conn}$ differential signals in the phase detector.

3.4. Reference filter

The second order MOSFET-C low-pass reference filter has a similar architecture to the main filter but has a higher Q value of the poles. The reference filter in Fig. 5 has a cutoff frequency of 8.184 MHz which is half of the crystal frequency (xtal clock frequency of 16.368 MHz). When xtal clock in Fig. 2 is divided by 2, the frequency becomes 8.184 MHz. When the CML voltage level generated from the CMOS to CML circuit at a frequency of 8.184 MHz passes through the

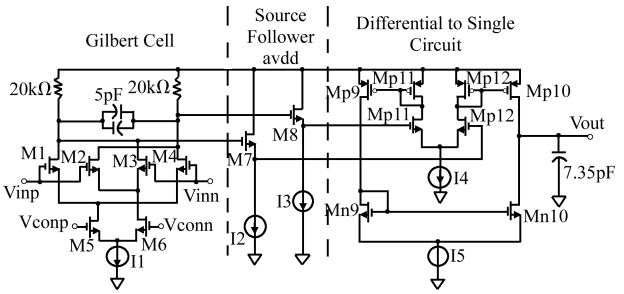

Fig. 6. Phase detector circuit.

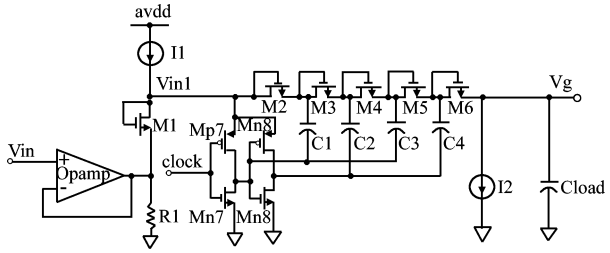

Fig. 7. Charge pump circuit.

reference filter, the phase of the output signal is orthogonal with that of its input. Also, the 16.368 MHz and 8.184 MHz clock signals are in the stop-band of the BPF to prevent the interferers appearing in the pass-band.

3.5. Phase detector

The phase detector in Fig. 6 consists of three parts: Gilbert cell, source follower and differential to single circuit. The Gilbert cell compares the phase of $V_{\rm inp}$ and $V_{\rm inn}$ to that of $V_{\rm conp}$ and $V_{\rm conn}$. If the two are orthogonal, it will generate a $V_{\rm out}$ signal for the charge pump circuit to generate a proper $V_{\rm g}$ signal for the main filter. The reference filter, phase detector and charge pump construct a negative feedback loop to stabilize the $V_{\rm g}$ which provides gate voltage for the MOSFET resistors in the main filter.

3.6. Charge pump

The charge pump circuit in Fig. 7 is derived from the Dickson multiplier[6]. The voltage multiplier raises $V_{\rm g}$ to the required value and the current source I_2 provides a leakage path. The generated $V_{\rm g}$ only needs to drive transistor gates and thus does not need to supply a dc current. M2–M6 are diode-connected transistors functioning as diodes. This kind of scheme is slightly different from the work in Ref. [1]. The capacitance values of C_1–C_4 are the same and all are equal to $C_{\rm c}$. The gate-drain voltage of the diodes is annotated as $V_{\rm D}$. The output of the charge pump is given by[1]

$$V_{\rm G} = (n+1)V_{\rm in} - \frac{nI_2}{C_{\rm c}F_{\rm clk}}. \quad (1)$$

Here we choose $n = 5$, $I_2 = 100$ nA, $C_{\rm c} = 200$ fF and $F_{\rm clk} = 16.368$ MHz.

4. Simulation results

A BPF with auto-tuning system has been fabricated in UMC standard 0.18 μm CMOS technology. A filter within a

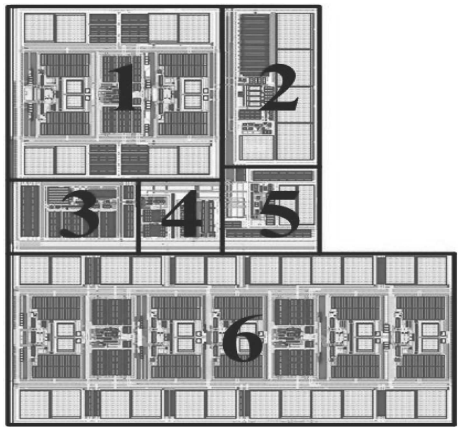

Fig. 8. Layout photo of the BPF with auto-tuning system.

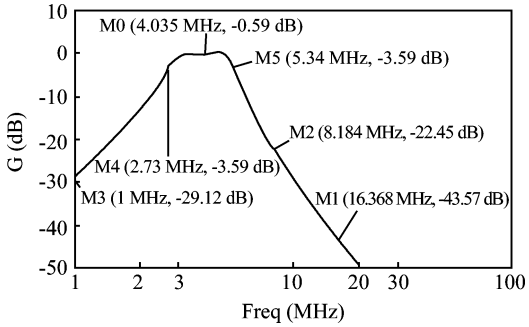

Fig. 9. AC response of the BPF.

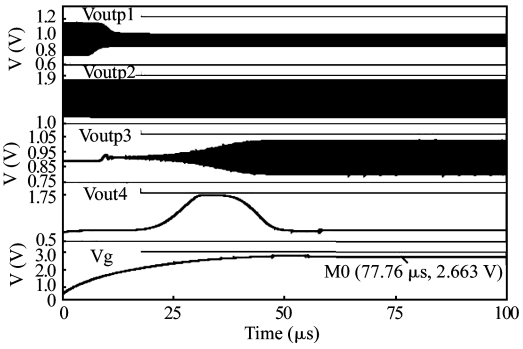

Fig. 10. Transient response of the calibration circuits.

GPS chip system has been described. The layout of the filter system is shown in Fig. 8 surrounded by dark lines marked by annotations 1–6. The numbers 1–6 in Fig. 8 respectively represent the sub-circuit layout areas in the filter systems. 1 represents the reference filter; 2 represents the charge pump circuit; 3 represents the bias circuit providing voltages and currents for other circuits; 4 is the CMOS to CML circuit; 5 is the phase detector circuit; 6 is the main filter.

Figure 9 shows the AC response of the BPF with asymmetric attenuation at two stop-bands. It attenuates –29.12 dB at 1 MHz and –43.57 dB at 16.368 MHz. The transient response curves of $V_{\rm outp1}$, $V_{\rm outp2}$, $V_{\rm outp3}$, $V_{\rm out4}$ and $V_{\rm g}$ in calibration circuits are shown in Fig. 10.

The magnified transient response curve of the $V_{\rm g}$ is shown in Fig. 11. The auto-tuning system settling time is less than 100 μs. The $V_{\rm inp}$ and $V_{\rm outp}$ of the main filter are shown in Fig. 12. The simulated third order harmonic input intercept point ($\rm IIP_3$) is shown in Fig. 13. The $\rm IIP_3$ can be calculated

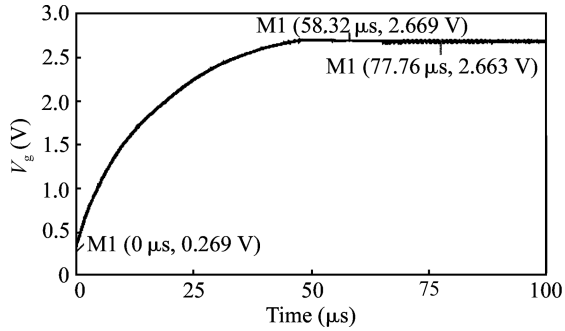

Fig. 11. Magnified transient response of the V_g in Fig. 10.

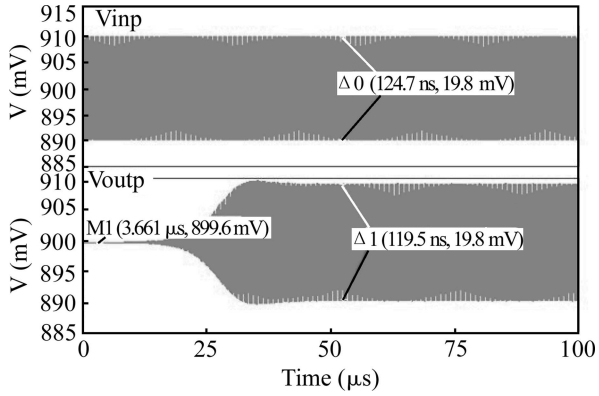

Fig. 12. Transient response of the input and output of BPF.

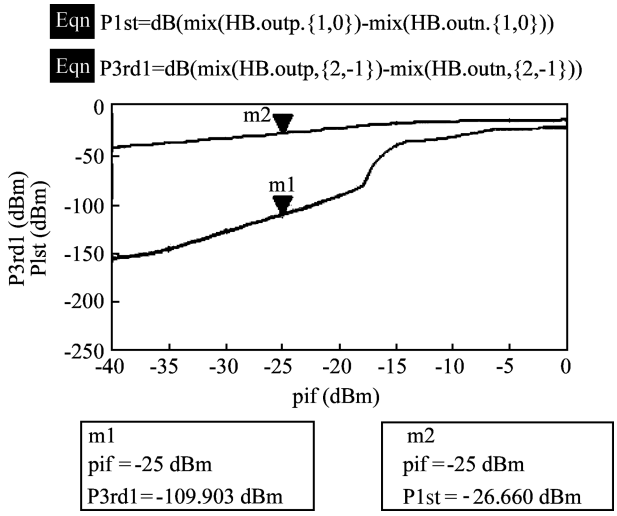

Fig. 13. Linearity (IIP_3) of the BPF.

according to Eq. (2)[7]:

$$\mathrm{IIP_3}|_{\mathrm{dBm}} = \frac{(P_{1\mathrm{st}} - P_{3\mathrm{rd1}})|_{\mathrm{dB}}}{2} + \mathrm{pif}|_{\mathrm{dBm}}. \quad (2)$$

From Fig. 13, we can find that the input power is swept from –40 to 0 dBm with steps of 1 dBm in which the (–40 dBm, –18 dBm) range corresponds to a linear input range. The value of IIP_3 can be calculated from any row of values from –40 to –18 dBm. For instance, we choose the row of value pif = –25 dBm. According to Eq. (2), the value of IIP_3 is 16.621 dBm which corresponds to good linearity. A filter performance summary is shown in Table 1. A performance comparison with Ref. [1] is shown in Table 2. The filter performance is obviously superior in current consumption, linearity, and tuning speed to the case in Ref. [1] although it provides less gain than Ref. [1].

Table 1. Performance summary of BPF.

Parameter		Value
Supply voltage (V)		1.8
Leakage current (nA)		0.7
Pass-band performance	BW (MHz)	(2.730, 5.340)
	Gain (dB)	–0.67
	Ripple (dB)	0.25
	IIP_3 (dBm)	16.621
Stop-band attenuation	@1 MHz (dB)	–29.12
	@16.368 MHz (dB)	–43.57
Noise performance	Input referred noise (μV_{rms})	47.455
	Noise figure (dB)	38
Main filter	Occupying area (mm^2)	0.300
	Current consumption (mA)	1.960
Calibration circuits	Occupying area (mm^2)	0.292
	Current consumption (mA)	1.340
Total	Occupying area (mm^2)	0.592
	Current consumption (mA)	3.300

Table 2. Performance comparison with Ref. [1].

Parameter		Ref. [1]	This work
Supply voltage (V)		2.7	1.8
Current consumption (mA)	Main filter	2.8	1.96
	Tuning circuit	~ 1.5	1.34
Cutoff frequency/Bandwidth (MHz)		1.92	(2.73, 5.34)
Pass-band gain (dB)		8.5	–0.67
Pass-band IIP_3 (dBm)		11	16.621
Input referred noise (μV_{rms})		47	47.455
Tuning system settling time (μs)		150	< 100

5. Conclusion

Fabricated in UMC 0.18 μm CMOS process technology, this asymmetric band-pass filter is presented with a charge pump auto-tuning architecture. The asymmetric architecture is efficient both in area and power consumption while accommodating the specifications well. It can be tuned to a bandwidth of (2.73 MHz, 5.34 MHz) with a pass-band gain of −0.67 dB and pass-band ripple of 0.25 dB utilizing an auto-tuning scheme based on a charge pump circuit. In addition, the BPF can be tuned to the desired center frequency without obviously changing the bandwidth. With 50 Ω as the source impedance, the pass-band IIP_3 and total input referred noise are 16.621 dBm and 47.455 μV_{rms} respectively. The attenuation at 1 MHz and 16.368 MHz are –29.12 dB and –43.57 dB respectively. The main filter consumes 3.528 mW and the calibration circuits consume 2.412 mW from a 1.8 V power supply. The main filter and the calibration circuits occupy an area of 0.77 × 0.39 = 0.300 mm^2 and 0.53 × 0.55 = 0.292 mm^2 respectively. The filter can be used in GPS and Bluetooth systems.

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