A low power cyclic ADC design for a wireless monitoring system for orthopedic implants*

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Abstract: This paper presents a low power cyclic analog-to-digital convertor (ADC) design for a wireless monitoring system for orthopedic implants. A two-stage cyclic structure including a single to differential converter, two multiplying DAC functional blocks (MDACs) and some comparators is adopted, which brings moderate speed and moderate resolution with low power consumption. The MDAC is implemented with the common switched capacitor method. The 1.5-bit stage greatly simplifies the design of the comparator. The operational amplifier is carefully optimized both in schematic and layout for low power and offset. The prototype chip has been fabricated in a United Microelectronics Corporation (UMC) 0.18-μm 1P6M CMOS process. The core of the ADC occupies only 0.12 mm^2. With a 304.7-Hz input and 4-kHz sampling rate, the measured peak SNDR and SFDR are 47.1 dB and 57.8 dBc respectively and its DNL and INL are 0.27 LSB and 0.3 LSB, respectively. The power consumption of the ADC is only 12.5 μW in normal working mode and less than 150 nW in sleep mode.

Key words: monitoring system; low power consumption; small size; analog to digital convertor; single to differential convertor

DOI: 10.1088/1674-4926/30/08/085009 **EEACC:** 1265H

1. Introduction

Total knee replacement (TKR) can release patients with degenerative joint disease from severe pain and immobility due to osteoarthritis. However, TKR implants will fail because of wearing, loosening, misalignment, etc. Therefore, early diagnosis of these abnormalities is essential in order to avoid these extreme revision surgeries[1]. Many embedded devices which could provide new in-vivo diagnostics have been put forward and many methods to generate power continually for these devices have been analyzed.

The power generation characteristics of stiff lead zirconate titanate (PZT) ceramics were analyzed and their equivalent circuit was proposed in Ref. [2]. It was then verified by simulation and experimental results. It was found that the maximum power (about 1.2 mW) is generated when the four PZTs receive uniform and maximum force from the implant.

In Ref. [3], a novel architecture of a wireless monitoring system for real-time monitoring of orthopedic implants was proposed. The system architecture consists of two parts: one embedded in the orthopedic implants, and the other outside the body. Inside the embedded part, sensors are applied to obtain in-vivo data which will be then saved in EEPROM. It can be powered by an RF signal as well as PZT elements[2]. The embedded chip is the main part of the system. All the modules in the embedded chip are shown in Fig. 1. It consists of RF circuits, a micro antenna, power circuits, piezoelectric elements, memory, a low power micro control unit, and an analog-to-digital convertor (ADC). The wireless transceiver in the RF circuits transmits or receives data using the micro antenna. The power circuit should transfer the power from PZT elements into useful power for other circuits. The ADC is designed to transform the biological information into digital data to be stored in the memory. The proposed system has been implemented in a 0.18-μm CMOS process of the United Microelectronics Corporation (UMC).

The ADC is critical for the system. This paper presents the detailed design of an ADC for the system. A two-stage cyclic structure is chosen, which is often embedded in a system on chip (SOC) due to its compact size[4, 5]. By adding a single-to-differential converter in the front end and carefully optimizing both schematic and layout, the proposed ADC has the following features compared with other works: (1) single-ended input; (2) multi-channel selection; (3) smaller area; (4) lower power consumption[4, 5]. The proposed ADC is embedded in the monitoring system SOC. For better testing, the

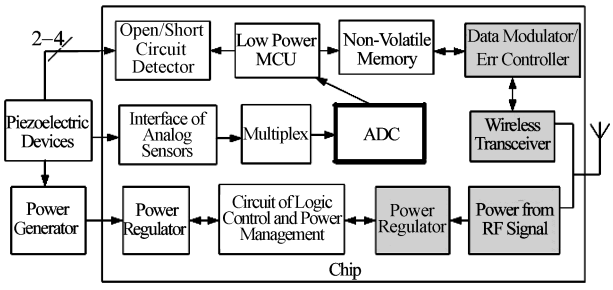

Fig. 1. Embedded chip of the system.

* Project supported by the National Natural Science Foundation of China (No. 60475018).

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Received 21 January 2009, revised manuscript received 1 April 2009

ADC has also been fabricated and packaged individually. In addition, the design requirements put to ADC by the system will be depicted. The cyclic architecture will be explained. The detailed circuit of the ADC will be described and some low power strategies will be shown.

2. Requirement of system

Many special requirements are made on the design of the ADC due to the specific application. First of all, the ADC must have the characteristic of multi-channel selection. Four identical PZT elements are used in the wireless monitoring system, which will provide power for the system in normal working mode and generate the pressure signal of TKR implants[3]. The channel selection signal decides which channel will be converted at a certain time. Only one channel will be chosen. Secondly, two modes are needed, which are the normal working mode and the sleep mode. The system decides the mode of the ADC according to the working situation of the moment. For example, when the wireless transceiver is transmitting data, the ADC is in sleep mode to save system power. In normal working mode, the power dissipation of the ADC can not exceed 50 μW owing to the limited power generated by the PZT elements or the RF signal. Finally, the working condition of the orthopedic implants and the diagnosis situation demand many design specifications of the ADC. A sample frequency of 400 Hz is enough because the patient often has four steps in one second when they are walking, while a sample speed of more than 4 kHz is needed for precise clinic diagnosis. Clinic diagnosis also demands the resolution of the ADC to be 8 bit. Moreover, the chip size must be as small as possible, which is determined by the SOC system.

Some types of ADC are widely used in other applications. A delta sigma ADC can provide high resolution. However, the large power consumption is unacceptable and the high resolution is not so necessary in this application. The pipelined ADC can provide high speed but it has a large area and power consumption. In addition, when the sample rate is low, the leakage current of the switch will lead to inaccuracy in the pipelined ADC[6]. Generally, they are not taken into consideration in small area or low sample rate designs. The successive-approximation ADC (SAR ADC) is a good choice if a moderate speed and moderate resolution convertor is to be designed. But the accuracy of a conventional SAR ADC depends on the matching accuracy of the on-chip passive components, which is in proportion to the square root of the area[7]. Thus, a large chip size is needed in order to maintain the necessary ratio accuracy for SAR ADC. Because of the reasons mentioned above, all three kinds of ADC can not satisfy the demands of the monitoring system.

In this design, we adopt the structure of two-stage cyclic ADC. The cyclic ADC is a modification of the pipelined ADC. Compared with the pipelined ADC, the cyclic ADC has a smaller area, and a higher capacitor switching rate for the same conversion rate, which helps to reduce the leakage effect of the switch when the conversion rate is as low as 400 samples/s. In other word, it saves area and improves conversion accuracy in this application. It is widely used in SOC for its compact area. The detailed architecture will be described in the next section.

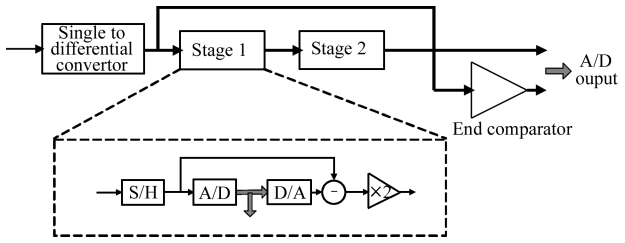

Fig. 2. Overall architecture of cyclic ADC.

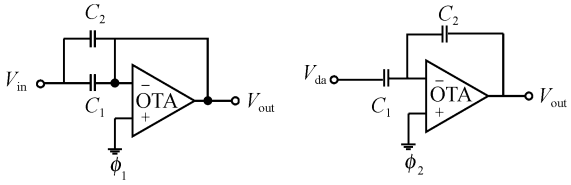

Fig. 3. Switched capacitor implementation of MDAC.

3. Cyclic architecture

3.1. Overall architecture

The overall architecture of the cyclic ADC is illustrated in Fig. 2. The 8-bit cyclic ADC has two stages and its conversion period is composed of 8 clock phases. The input signal will be firstly converted from single-ended to fully differential-ended at the 1st clock phase, and then tracked and sampled at the 2nd stage at the 2nd clock phase. After that, the output of the 2nd stage will be fed back as the input of the 1st stage at the 3rd, 5th, 7th clock phase of the conversion period. The 8-bit digital output code is generated at the end of the conversion period. Each stage consists of a sample/hold (S/H) circuit, a single bit AD and DA convertor, an analog subtractor and an $\times 2$ amplifier.

3.2. Multiplying DAC block (MDAC)

The S/H, DAC, subtractor, and $\times 2$ amplifier generally can be combined in a multiplying DAC functional block (MDAC), as shown in Fig. 3. The conventional switched capacitor structure is adopted here. The function of one bit ADC can be accomplished by the comparator. In MDAC, operation is via charge transfer using a capacitor array. At the end of the sample phase ϕ_1, the capacitors C_1 and C_2 capture the input signal and the charge on them can be expressed by

$$Q = V_{\text{in}}(C_1 + C_2). \tag{1}$$

In transfer phase ϕ_2, the charge on C_1 and C_2 will be redistributed under the driving of the OTA, and the output voltage becomes:

$$V_{\text{out}} = \frac{C_1 + C_2}{C_2} V_{\text{in}} - \frac{C_1}{C_2} V_{\text{da}}, \tag{2}$$

where $V_{\text{da}} = 0$ or V_{ref}, decided by the output of the comparator.

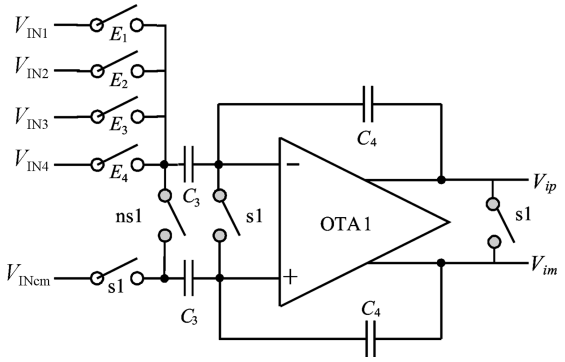

Fig. 4. Single to differential convertor.

If $C_1 = C_2$, the output voltage can be expressed as

$$V_{\text{out}} = 2V_{\text{in}} - V_{\text{da}}. \tag{3}$$

Thus, the S/H, DAC, subtractor, and ×2 amplifier function are realized by the MDAC.

A 1.5-bit stage has been chosen in the design of MDAC as in most pipelined ADCs. Some redundancy built in the 1.5-bit stage provides a large tolerance for component tolerances and imperfections. The requirement on the offset voltage of the comparator is reduced greatly due to the redundancy. With the help of a digital correction algorithm which eliminates the redundancy later, the final digital results can be calculated. The 1.5-bit stage greatly reduces the demand of the comparator, thus dynamic comparators can be used for low power.

3.3. Differential implementation

The fully differential circuit could reject the common-mode disturbances generated by the digital circuits, the clock drivers, etc. This is the most common circuit style in mixed-signal circuits. Most other cyclic ADCs have differential inputs[4, 5]. But in this design, the input signal, which contains diagnosis pressure data, is only single-ended. In order to connect the single-end input with the differential conversion core, a single-to-differential conversion circuit is included. The switched capacitor architecture is used here again, as shown in Fig. 4. The output of the conversion circuit is equal to:

$$V_{\text{ip}} - V_{\text{im}} = \frac{C_4}{C_3}(V_{\text{IN}} - V_{\text{INcm}}). \tag{4}$$

The channel selection function can also be achieved by the single-to-differential converter. The 4-1 analog multiplexer controlled by E_1–E_4 decides which channel will be selected and sampled at a certain time. Although one ADC per channel could preserve the signal integrity[5], there exists offset and gain mismatch among different ADCs. This may destroy the comparability of converted results from different channels. To avoid this problem, we integrate the channel selection function into the ADC and use only one ADC to convert the signal from different channels. The signal integrity could be ensured by limiting the length of the sensitive analog wires.

The A/D conversion circuits, which are in fully differential style and include the two main MDACs, the comparators and the digital redundancy correction logic, are shown in Fig. 5. Other modules such as reference voltage generation circuit are omitted here for simplicity. The corresponding switch-controlling signals are shown in Fig. 6.

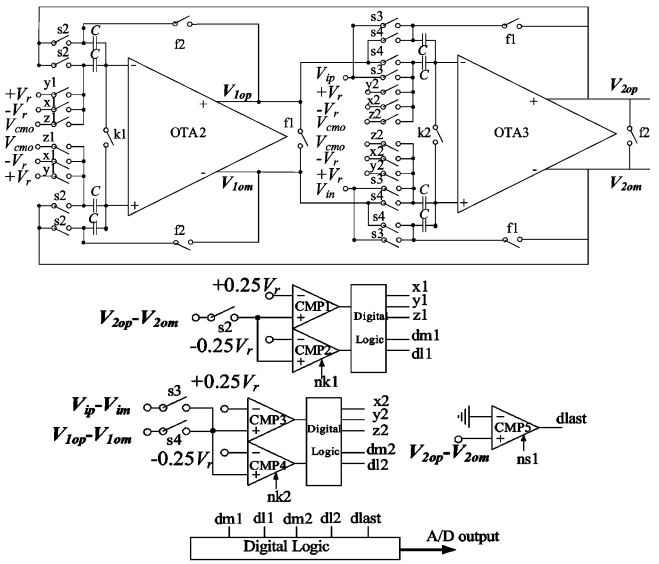

Fig. 5. ADC architecture in fully differential style.

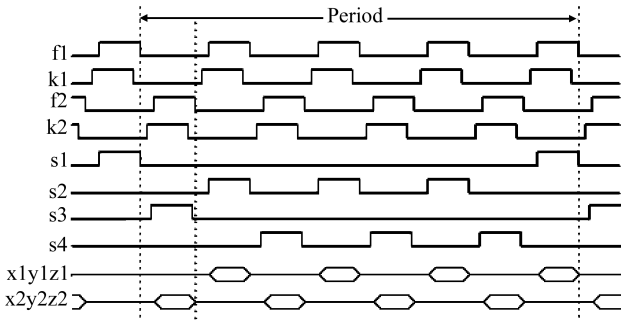

Fig. 6. Switch-controlling signals.

3.4. Sleep mode

The power of the system generated by the PZT elements or the RF power circuits is limited[3]. In order to save power as much as possible, the modules which do not have operations or are in idle status at a certain moment should be powered down. For example, the system forces the ADC to go to sleep when the RF transceiver is in transmission state. The power consumption of the ADC consists of two parts: the analog part and the digital part. The analog power is mainly consumed by the operational amplifiers which are set by the bias current. They are used to drive the analog output to the desired accuracy. The digital power is in proportion to the frequency of the input clock. The power-down function can be implemented by two means. One is turning off the current of the analog part by closing the bias. Almost no power will be consumed by the analog circuit in this condition. The other is using the clock-gating method to close the clock signal of the digital part. There is no activity associated with reloading of registers in the digital part, thus no power is consumed. Only leakage current will lead to tiny power consumption in sleep mode.

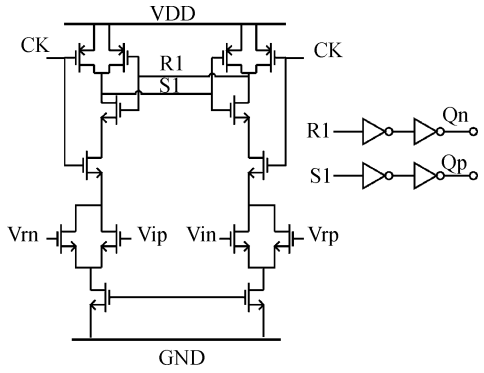

Fig. 7. Dynamic comparator.

4. Circuit design

From the description of the system architecture of the cyclic ADC, it can be seen that the operational amplifier and the comparator are the two key modules of the ADC. The design of the two components will be discussed in this section.

4.1. Operational amplifier

Operational amplifiers are used in the MDAC, the single to differential convertor and the reference voltage generator. The operational amplifier designed here is based on the fully differential folded-cascode structure as Ref. [4]. This structure has a good compromise between low power and large output swing. A high-swing biasing circuit provides the four bias voltages for the operational amplifiers. A switched capacitors common-mode feedback circuit is also integrated to stabilize the common output voltage and reduce clock feed through distortion.

In normal working mode, the power efficiency and analog signal processing accuracy are mainly decided by operational amplifiers. In this design, large L and low $V_{gs} - V_{th}$ input transistors are adopted for accuracy and power optimization. Large L helps to reduce the input offset voltage, and low $V_{gs} - V_{th}$ helps to get a high DC gain and a relatively high transconductor g_m under the constraint of low current. The decrease of the transistor speed resulting from large L and low $V_{gs} - V_{th}$ is not critical here, as the circuit works in a low sample rate and the requirement of the operational amplifier band-width is low.

The layout of the operational amplifier is also optimized carefully. The input transistors and current mirror are placed in common centroid style to lower the mismatch. In this way, the effects of global changes can be averaged out. Dummy transistors are added for better matching.

The post-layout simulation shows that the designed operational amplifier has a DC gain of 70 dB and a band-width of 140 kHz under the worst case. The phase margin exceeds 70 $^\circ$. Each amplifier with bias circuit consumes less than 1.8 μW power.

4.2. Comparator

The dynamic comparator utilizing the latch structure is shown in Fig. 7. This structure has the advantages of low power and high speed. The input offset voltage is not a critical restriction of the ADC due to the adoption of a 1.5-bit stage.

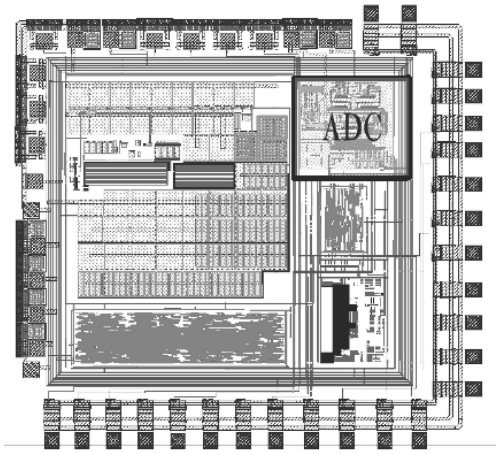

Fig. 8. Layout of the ADC in the system.

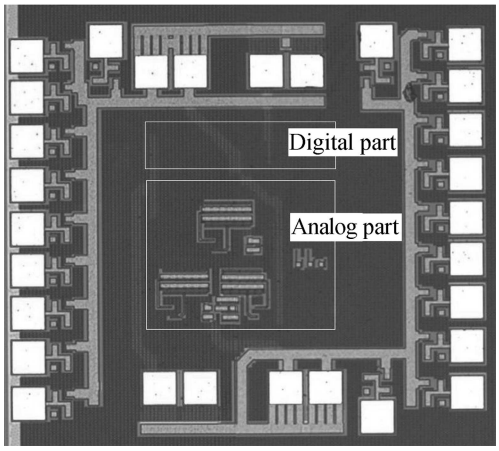

Fig. 9. Micrograph of the test chip.

5. Experimental results

The monitoring system has been fabricated in a UMC 0.18-μm 1P6M CMOS process. The ADC is embedded in the system, as shown in Fig. 8. It has also been fabricated under the same process and packaged individually for better testing. Figure 9 shows a micrograph of the test chip. The core of the ADC including both analog and digital part occupies only 0.12 mm^2 and the area of whole chip including pad is 0.7 mm^2. In the measurements, the supply voltages AVDD, DVDD were all set to 1.8 V. The following part of this section describes how the prototype was tested and its performance.

5.1. Static performance

A code density test was conducted using a full-swing sinusoidal input with amplitude of 1.8 V. A sample frequency of 4 kHz is implemented, which satisfies the demands of the wireless monitoring system. More than 1 million samples were taken. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC are shown in Figs. 10 and 11 respectively. The DNL is in the range of –0.25 to 0.27 LSB and the INL is in the range of –0.3 to 0.2 LSB.

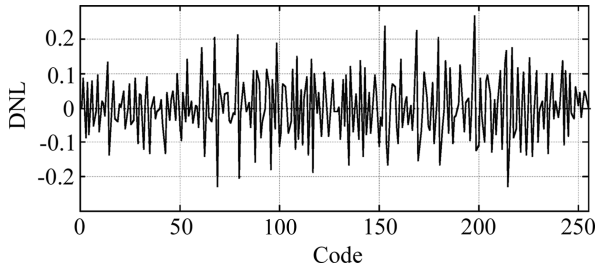

Fig. 10. Measured DNL of the ADC.

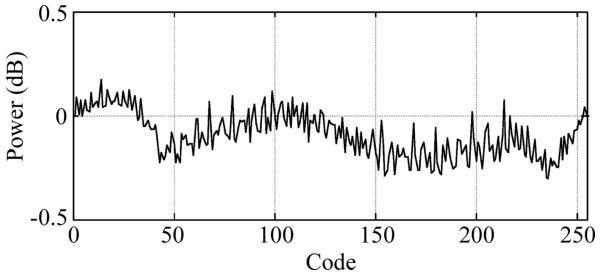

Fig. 11. Measured INL of the ADC.

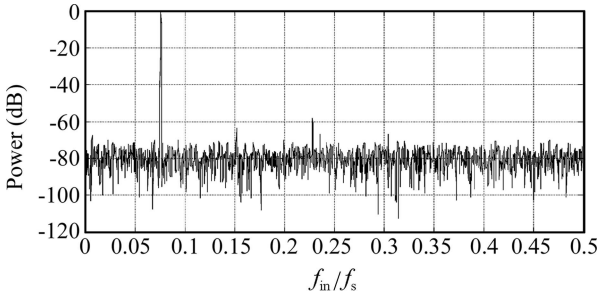

Fig. 12. Measured output spectrum of the cyclic ADC with –0.15 dBFS, 304.7 Hz sinusoidal input and 4 kHz sample frequency.

5.2. Dynamic performance

Figure 12 plots the measured output spectrum of the ADC under the sample frequency of 4 kHz. The amplitude and frequency of the input sine signal were set to –0.15 dBFS, 304.7 Hz. The result shows that the ADC has an SFDR of 57.8 dBc and an SNDR of 47.1 dB. This corresponds to an effective number of bit (ENOB) of 7.53 bit under the sample frequency, which the system demands, according to Eq. (5).

$$\text{ENOB} = \frac{\text{SNDR(dB)} - 1.76}{6.02}. \tag{5}$$

5.3. Power consumption

In normal working mode, the total power dissipation of the cyclic ADC is 12.5 μW under 1.8 V supply voltage and a 4 kHz sample frequency. When the ADC is in sleep mode, the sum of the current flow through AVDD and DVDD is only 78 nA. This means that the ADC consumes less than 150 nW in sleep mode.

A summary of the performance is provided in Table 1. The experimental results show that proposed ADC satisfies all the requirements of the monitoring system. It has good static and dynamic performance. Its low power and small size make it suitable for the monitoring SOC.

Table 1. ADC performance summary.

Parameter	Value
Supply voltage	1.8 V
Sample frequency	4 kHz
Input range	0–1.8V
Power dissipation (Normal working mode)	12.5 μW
Power dissipation (Sleep mode)	0.15 μW
SFNR @ f_{in} = 304.7 Hz, f_s = 4 kHz	57.8 dBc
SNDR @ f_{in} = 304.7 Hz, f_s = 4 kHz	47.1 dB
ENOB @ f_{in} = 304.7 Hz, f_s = 4 kHz	7.53 bit
DNL	0.27 LSB
INL	0.3 LSB
Max sample frequency	40 kHz, ENOB > 7 bit
Chip size (ADC core)	400 × 300 μm^2

6. Conclusion

This paper describes the design of a 12.5 μW, 4 kHz, 8-bit cyclic ADC for a real-time wireless monitoring system for orthopedic implants. A front-end single to differential convertor is included to connect the single-end input with the differential conversion core. Two-stage cyclic architecture is adopted in the conversion core. A 1.5-bit stage is utilized to simplify the design of the comparator. The operational amplifier and dynamic comparator are designed with careful optimization. Experimental results show that the ADC chip under a 0.18-μm 1P6M process consumes only 12.5 μW with a sample rate of 4 kHz and 7.53 bit ENOB. By turning off the bias of the analog part and the clock of the digital part, the ADC consumes less than 150 nW in sleep mode. The proposed ADC satisfies all the requirements of the specific application. The low power and small size make it possible to put the ADC inside the monitoring SOC. Future work includes some clinical experiment tests with the system in an application where PZT elements are used for power generation in a TKR implant.

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