A dual-mode complex filter for GNSS receivers with frequency tuning*

Gan Yebing(甘业兵)[1,†], Ma Chengyan(马成炎)[2], and Yuan Guoshun(袁国顺)[1]

(1 Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

(2 Hangzhou Zhongke Microelectronics Co, Ltd, Hangzhou 310053, China)

Abstract: A fifth/seventh order dual-mode OTA-C complex filter for global navigation satellite system receivers is implemented in a 0.18 μm CMOS process. This filter can be configured as the narrow mode of a 4.4 MHz bandwidth center at 4.1 MHz or the wide mode of a 22 MHz bandwidth center at 15.42 MHz. A fully differential OTA with source degeneration is used to provide sufficient linearity. Furthermore, a ring CCO based frequency tuning scheme is proposed to reduce frequency variation. The measured results show that in narrow-band mode the image rejection ratio (IMRR) is 35 dB, the filter dissipates 0.8 mA from the 1.8 V power supply, and the out-of-band rejection is 50 dB at 6 MHz offset. In wide-band mode, IMRR is 28 dB and the filter dissipates 3.2 mA. The frequency tuning error is less than ±2%.

Key words: complex filter; OTA; dual-mode; frequency tuning; CCO; GNSS

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1. Introduction

Recent research on global navigation satellite systems (GNSS) has rapid progress. GPS is in commercial use now, and some other systems such as Galileo and the Chinese Compass system are under construction. Hence, it will be practical to improve positioning accuracy through a combination of multi-mode positioning and information. Research into this application has been reported[1].

Image signal rejection is a key point in the design of high sensitivity GNSS receivers. After down conversion, the image signal overlaps on the wanted signal, and thus degrades the SNR of the IF output. As the received signal in the antenna is rather weak (under the thermal noise floor), an increase of SNR by 3 dB through image rejection is critical to the tracking sensitivity. In this work a dual-mode complex filter is designed to reject image interference for a GNSS receiver. Through circuit reuse and switching, the filter can be configured as narrow-band mode or wide-band mode，thus reducing the die area and power dissipation. Due to process corners, temperature variation and power supply fluctuation, on-chip frequency tuning is required for active filters.

Design details of the filter and the tuning scheme are also presented.

2. Complex filter design

2.1. Image rejection scheme selection

The image rejection scheme lies on the receiver architecture. This involves either high-IF, low-IF or zero-IF[2].

The high-IF requires high quality factor off-chip filters. Ideally a zero-IF receiver has no image problem, but flicker noise and dc offset might significantly degrade the SNR which is unacceptable in this receiver. Generally zero-IF is more suitable for wide-band systems. To relax the image rejection requirement and reduce the folded-back interference level, low-IF is preferable for this receiver. In this work a low-IF of 4.1 MHz is chosen for narrow mode and 15.42 MHz for wide mode. Figure 1 shows the architecture of the GNSS receiver.

In low-IF receivers, any phase or gain mismatch between the I and Q branch will cause the image signal at $-\omega_{\rm IF}$ to spill over the image band at $\omega_{\rm IF}$. As a result the maximum image reject ratio will be limited by the I/Q imbalance:

$$\mathrm{IMRR}_{\max} \approx -10\lg\left(\tan^2\frac{\theta}{2}+\frac{\Delta^2}{4}\right), \tag{1}$$

where Δ and θ are the gain and phase mismatch, respectively. For IMRR > 30 dB, the maximum tolerable phase and gain imbalances are 3.6° and 6.4%. Hence, it is critical to improve the I/Q balance in LO, mixer and the complex filter to achieve higher IMRR.

As mentioned above, the received satellite signal is rather weak and lies under the thermal noise floor. The low-IF architecture makes the image signal lie within the same band of the desired signal. There is no strong interference in the band, and hence, only the thermal noise needs to be rejected. The

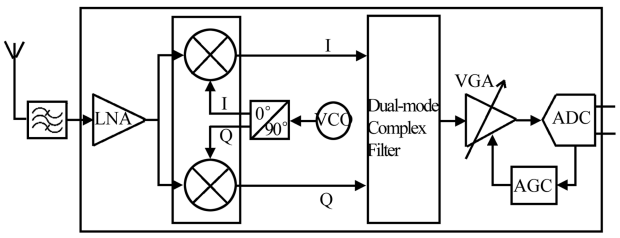

Fig. 1. Architecture of the receiver.

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† Corresponding author. Email: ganyebing@casic.ac.cn

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effective C/N_oratio with image rejection is given by[1]

$$\left(\frac{C}{N_o}\right)_{OUT} = \frac{C}{N_o + N_{image}} = \left(\frac{C}{N_o}\right)_{IN} \times \frac{1}{1 + \frac{1}{IMRR}}. \quad (2)$$

From Eq. (2), image interference results in 3 dB C/N_o loss, and a finite IMRR of 16 dB reduces C/N_o loss to just 0.1 dB, which is negligible for most cases. In addition, I/Q imbalance limits the attainable IMRR. Thus IMRR higher than 30 dB is not necessary for this receiver. Simulation results show that a Butterworth filter of fifth order in narrow-band mode and seventh order in wide-band mode is sufficient to provide enough IMRR.

For on-chip complex filters, there are several potential architectures. Though passive RC complex filters[3] can achieve high IMRR, due to their band reject response and poor selectivity, an additional band-pass filter is needed to provide out-of-band attenuation. The finite input impedance also loads the mixer. An active OPA-RC filter[4] provides large linearity, but tuning is difficult. OTA-C band-pass complex filters can achieve high image rejection and large out-of-band attenuation. As it works in current mode, the filter dissipates little and can be easily reconfigured. Hence, OTA-C filters are widely used in analog systems[5–7]. In this design, a linearity improved OTA-C complex filter is proposed.

2.2. Complex filter theory

Complex filtering operates in the complex domain, thus quadrature down converting is required. After eliminating higher order terms, the result of mixing is

$$Y(j\omega) = 0.5A_{des}A_{lo}e^{j\omega_{IF}t} + 0.5A_{img}A_{lo}e^{-j\omega_{IF}t}. \quad (3)$$

As the wanted signal is located at ω_{IF}, and the image signal is located at $-\omega_{IF}$, the image signal can be filtered out by a band-pass complex filter center at ω_{IF}. The OTA-C complex filter is designed through linear translation which shifts the center frequency of a low-pass filter (LPF) from 0 to ω_c. Taking a first order complex filter as an example, after translation, the frequency response is

$$Y(j\omega) = \frac{1}{j(\omega - \omega_c)/\omega_o} X(j\omega). \quad (4)$$

Assume that $\omega_o = g_{mo}/C$ and $\omega_c = g_{mc}/C$. Replacing X and Y with $X = X_I + jX_Q$ and $Y = Y_I + jY_Q$ will lead to

$$Y_I = \frac{g_{mo}}{j\omega C}(X_I - Y_I) - \frac{g_{mc}}{j\omega C}Y_Q, \quad (5)$$

$$Y_Q = \frac{g_{mo}}{j\omega C}(X_Q - Y_Q) + \frac{g_{mc}}{j\omega C}Y_I. \quad (6)$$

Figure 2 presents the process of linear translation for OTA-C complex filters. Only a gyrator is required to be added where capacitors are located.

2.3. Complex filter design

Since the filter occupies a large area, it is advisable to design a dual-mode filter with as many shared components as possible. Capacitors in the filter occupy nearly 2/3 of the total area. In this work, all the capacitors are shared and the filter frequency is reconfigured by switching the g_m values. As explained above, as $\omega_c \propto g_{mc}/C$ and $\omega_o \propto g_{mo}/C$, $\omega_c(\omega_o)$ will change proportionally with $g_{mc}(g_{mo})$ values. The full circuit of the dual-mode complex filter is shown in Fig. 3. It is a cascaded biquad structure. In narrow-band mode, the third biquads are shortened, thus the filter is configured as a fifth order Butterworth filter. In wide-band mode, the third biquads are enabled and their outputs are selected, so the filter is seventh order.

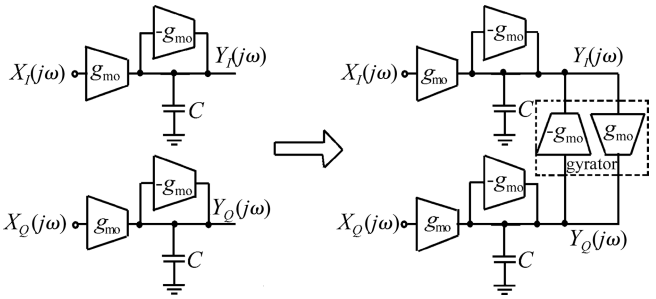

Fig. 2. Conversion of an LPF to a complex BPF through linear frequency translation.

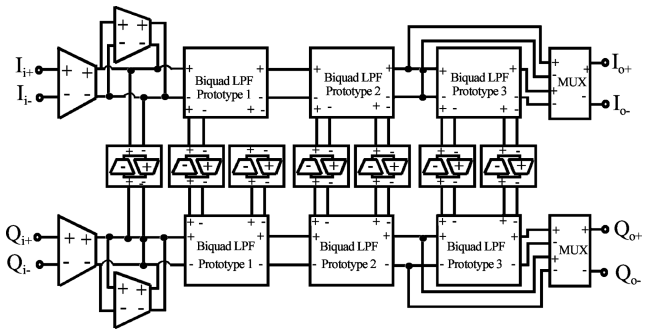

Fig. 3. Complete circuit of the complex filter.

2.4. OTA design

There are several optional OTA structures. Nauta's OTA[8] and pseudo differential OTA[5] provide fine linearity and are suitable for low voltage application. However, both are hard to tune. A simple full differential OTA with tail current source is easy to tune. But the linearity is poor as the g_m value decreases quickly with input level. In this paper, a fully differential OTA with source degeneration[9, 10] is adopted.

As shown in Fig. 4(a), M3 and M4 are biased in the triode region with variable on resistances according to input level. The total g_m is

$$g_m = \frac{i_{o1} - i_{o2}}{V_d} = \frac{2}{1/g_{m1} + 1/g_{m2} + (r_{ds3} \| r_{ds4})}, \quad (7)$$

where r_{ds3} and r_{ds4} are the on resistances of M3 and M4. As the input level increases, the parallel resistance of M3 and M4 reduces. This reduced resistance attempts to cancel the decrease of g_{m1} and g_{m2}, thus keeping the g_m value constant. Assume that all NMOS transistors have the same process parameters.

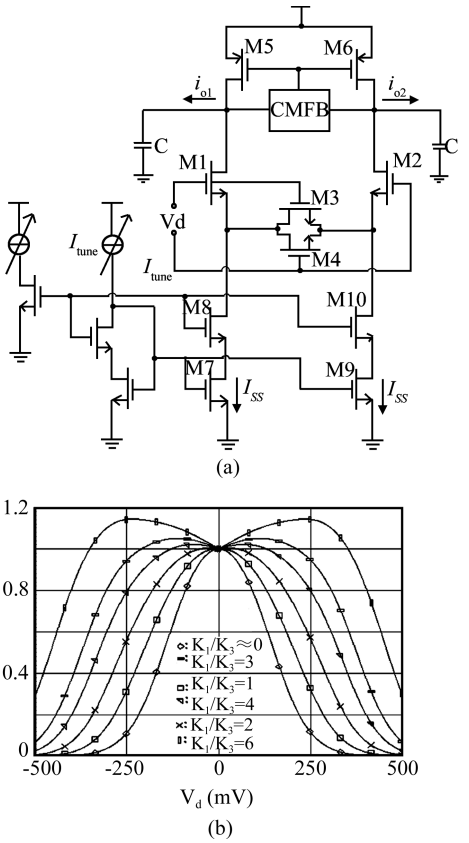

Fig. 4. (a) OTA with source degeneration; (b) Normalized g_m with different k_1/k_3.

Denote k_1, k_2, k_3 as $k_i = 0.5\mu_n C_{ox} (W/L)_i$. The equivalent small signal transconductance is

$$g_{m0} = \frac{4k_3}{k_1 + 4k_3} \sqrt{k_1 I_{SS}}. \tag{8}$$

If a proper k_1/k_3 is chosen, a more stable OTA is achieved. Simulation results of different k_1/k_3 with the TSMC 0.18 μm CMOS process are shown in Fig. 4(b). Since the OTA dissipates more as k_1/k_3 increases, a ratio of $k_1/k_3 = 3.5$ is proposed in this work as a good tradeoff between linearity and power. With this ratio, the input level can be as high as ±220 mV with ±3% fluctuation of g_m value.

From Eq. (8), increasing the g_m value by n times requires n^2 times more tail current. Thus it is not economical to switch the tail current to digitally change g_m. In this work the g_m value is configured through switching parallel OTA numbers, and the variable tail current is used for continuous tuning.

3. Frequency tuning

The requirement for frequency tuning is a result of large time-constant fluctuations due mainly to process variation, temperature and supply fluctuation. There might be around 20% variation for on-chip resistors or g_{mo} values, and more than 10% variation for capacitors which results in a total 30%–50% error for g_m/C time-constant products.

In this work, a PLL based frequency tuning scheme is adopted. As shown in Fig. 5, when the loop is stable, time constant of the oscillator is locked to the reference. The

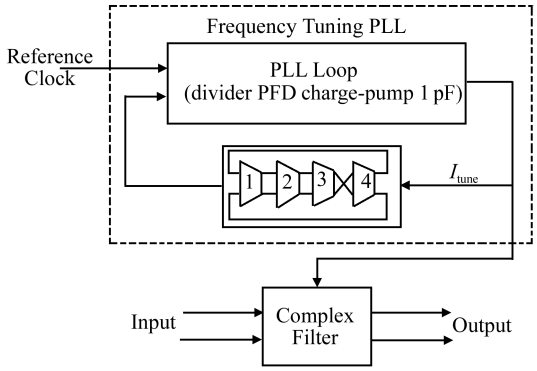

Fig. 5. Frequency tuning scheme in this work.

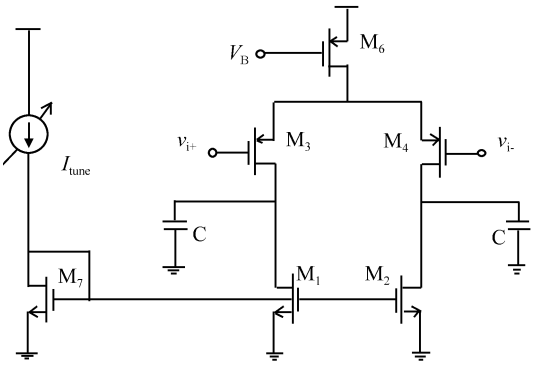

Fig. 6. Simplified schematic of the delay cell.

control voltage is also connected to the complex filter to tune the g_m value by changing the tail current. As the oscillator and the complex filter have the same time constant term g_m/C, if the PLL is locked, the frequency of the filter is tuned to the desired value, too.

The key point of tuning is to find a matching g_m/C time-constant product between the oscillator and the filter. A relaxation oscillator is proposed in Ref. [5] and the tuning error is 1.2% while a similar design used in Ref. [7] only obtains a tuning error of about 7%.The frequency of the relaxation oscillator must remain low enough to eliminate system error, and thus the required period before the loop becomes stable is much longer. In Ref. [11] a harmonic oscillator is proposed; however, the tuning accuracy is not presented. A similar design in Ref. [9] shows that the tuning error with a harmonic oscillator is less than 2.5%. The main disadvantages of harmonic oscillators are that they are difficult to oscillate and the nonlinearity will degrade the tuning accuracy. In this work, a ring CCO with triode transistors is proposed. The oscillator is easy to design and the CCO based tuning circuit has moderate tuning accuracy. The CCO can work in a wide frequency range, thus a higher PFD frequency is adopted and a shorter convergence period is achieved.

The simplified delay cell of the ring CCO is shown in Fig. 6. M1 and M2 are biased in the deep triode region. According to the "Barkhausen criteria", the CCO oscillates at ω_{osc}:

$$\omega_{osc} = \frac{1}{r_{ds1} C} = \frac{2k_1 \left(V_{gs,1} - V_{thn}\right)}{C}. \tag{9}$$

Assume that all NMOS transistors have the same process

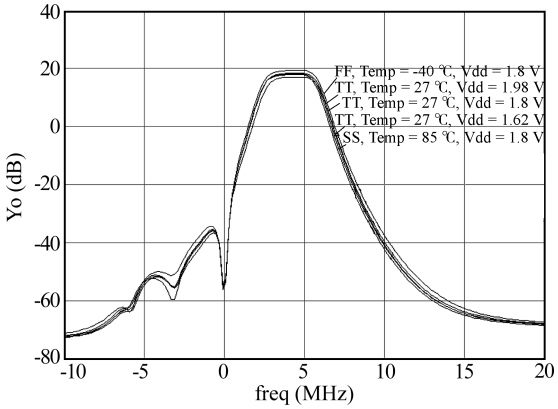

Fig. 7. Simulated tuning results.

parameters. As $V_{gs,1} = V_{gs,7}$, replacing $V_{gs,1} - V_{thn}$ with $V_{gs,7} - V_{thn}$ will lead to

$$\omega_{osc} = \frac{2k_1\left(V_{gs,7} - V_{thn}\right)}{C} = k\frac{\sqrt{k_1}}{C}\sqrt{I_{tune}}, \qquad (10)$$

where $k = \sqrt{4k_1/k_7}$.

The frequency related parameters of the complex filter are $\omega_o = g_{mo}/C$ and $\omega_c = g_{mc}/C$, where the g_m value is given by Eq. (8). Thus the time constant of the filter can be denoted as

$$\omega_{filter} \propto \frac{g_{mo}}{C} = k'\frac{\sqrt{k_1}}{C}\sqrt{I_{tune}}, \qquad (11)$$

where $k' = 4k_3/(k_1 + 4k_3)$. In Eqs. (10) and (11), the process related parameters $\sqrt{k_1}/C$ are identical, and ω_{osc} and ω_{filter} are tuned by I_{tune} simultaneously. The CCO and the filter have matched time-constants, and thus the filter can be tuned by this ring CCO based PLL.

The simulated results are shown in Fig. 7. Under ±20% process variations in FF and SS corners, –40 °C to 85 °C temperature range and ±10% power supply fluctuation, the tuning error is less than ±1.5%.

The tuning error mainly comes from two sources. First, the transistors of the OTA work in the active region while the transistors of the CCO work in the triode region. This will cause some system error in different corners. Second, M1 and M2 will leave the deep triode region with a higher amplitude level which causes variation in the oscillating frequency. Thus the oscillating amplitude must be limited.

4. Experiment result

The filter and the frequency tuning circuit have been implemented in the TSMC0.18 μm CMOS process. A chip micrograph is shown in Fig. 8. The areas occupied by the filter and the tuning circuit are 0.48×0.62 mm^2 and 0.22×0.28 mm^2, respectively. The filter dissipates 0.8 mA in narrow-band mode and 3.2 mA in wide-band mode respectively from a 1.8 V power supply. The tuning circuit dissipates 0.28 mA. Figures 9 and 10 are the measured frequency responses of the filter. The filter is 4.4 MHz bandwidth center at 4.1 MHz and

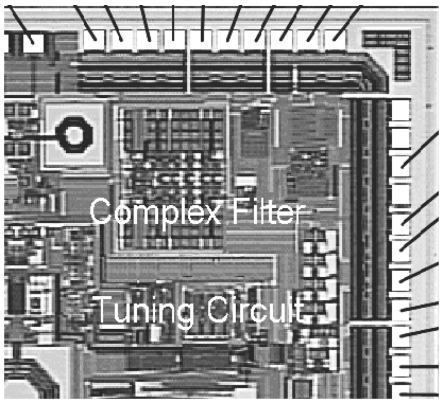

Fig. 8. Die micrograph.

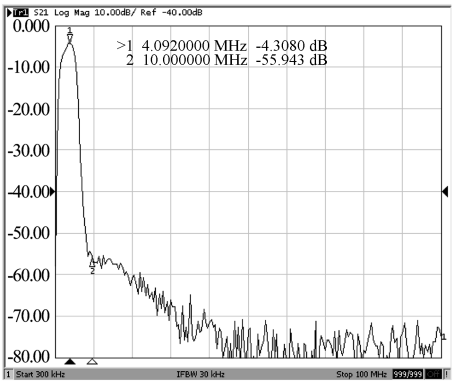

Fig. 9. Frequency response of narrow mode.

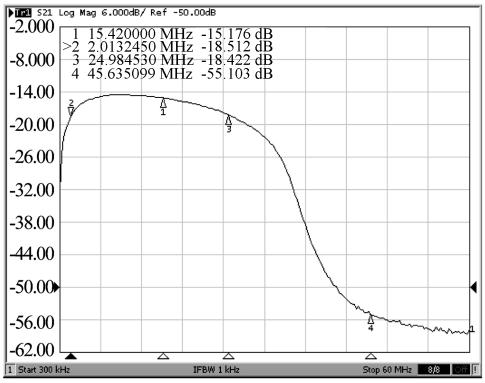

Fig. 10. Frequency response of wide mode.

22 MHz center at 15.42 MHz. The out-of-band suppression in narrow mode is about 50 dB at 6 MHz offset. The measured tuning error is about ±2%.

To measure IMRR, quadrature sinusoidal signals are required. In this work, these signals are obtained by mixing the RF signal with the quadrature LO. The measured IMRR in the whole pass band is more than 35 dB in narrow-band mode and more than 28 dB in wide-band mode. The measured IMRR are much smaller than the simulation, probably due to I/Q imbalance of the test signals and the filter itself. But both satisfy the requirement of the receiver.

5. Conclusions

A dual-mode OTA-C complex filter has been presented. Through component reuse and switching, this filter can be con figured as the fifth order narrow-mode of a 4.4 MHz

Table 1. Measured results of the filter.

Parameter	Narrow mode	Wide mode
Order	5 th	7 th
Center frequency (MHz)	4.092	15.42
–3 dB bandwidth (MHz)	4.4	22
Pass-band gain (dB)	–4.5	–15
Attenuation @ f_c + 6 MHz (dBc)	> 45	/
Image rejection ratio (dB)	> 35	> 28
3% linear range (mV)	> 200	> 200
V_{dd} (V)	1.8	1.8
I_{dd} (mA)	0.8	3.2
Filter area (mm^2)	0.3	0.3
Tuning circuit area (mm^2)	0.06	0.06

bandwidth center at 4.1 MHz or the seventh order wide-mode of a 22 MHz bandwidth center at 15.42 MHz. The measured image rejection ratios are 35 dB and 28 dB respectively. The ring CCO based PLL tuning scheme provides improved frequency accuracy. All these characteristics make the filter well suited for use in multi-mode GNSS receivers.

References

[1] Ko J, Kim J, Cho S, et al. A 19-mW 2.6-mm^2 L1/L2 dual-band CMOS GPS receiver. IEEE J Solid-State Circuits, 2005, 40(7): 1414

[2] Pui-Ln M, Seng-Pan U, Martin R P. Transceiver architecture selection review state-of-the-art survey and case study. IEEE Circuits Syst Mag, 2007, 7(2): 6

[3] Behbahani F, Kishigami Y, Leete J. CMOS mixers and polyphase filters for large image rejection. IEEE J Solid-State Circuits, 2001, 36(6): 873

[4] Linggajaya K, Do M A, Ma J G. A new active polyphase filter for wideband image reject downconverter. IEEE International Conference on Semiconductor Electronics, 2002: 213

[5] Emira A A, Sanchez-Sinencio E. A pseudo differential complex filter for Bluetooth with frequency tuning. IEEE Trans Analog Digital Signal Processing, 2003, 50(10): 742

[6] Khoury J M. Design of a 15-MHz CMOS continuous time filter with on-chip tuning. IEEE J Solid-State Circuits, 1991, 26(12): 1988

[7] Teo T H, Khoo E S, Uday D. Fifth order low- pass transitional gm-C filter with relaxation oscillator frequency tuning circuit. IEEE Conference on Electron Devices and Solid-State Circuits, 2003: 229

[8] Andreani P, Mattisson S, Essink B. A CMOS gm-C polyphase filter with high image band rejection. Solid-State Circuits Conference, 2000: 272

[9] Krummenacher F, Joehl N. A 4-MHz CMOS continuous-time filter with on-chip automatic tuning. IEEE J Solid-State Circuits, 1988, 23(3): 750

[10] Cui Fuliang, Ma Dequn, Huang Lin, et al. Image rejection for Bluetooth receiver. Chinese Journal of Semiconductors, 2005, 26(1): 153 (in Chinese)

[11] Ma Dequn, Cui Fuliang, He Jie, et al. Design considerations and implementation for low power on-chip automatic tuning. Chinese Journal of Semiconductors, 2004, 25(9): 1186 (in Chinese)