A controllable resistor and its applications in pole–zero tracking frequency compensation methods for LDOs*

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Abstract: This paper presents a controllable resistor, which is formed by a MOS-resistor working in the deep triangle region and an auxiliary circuit. The auxiliary circuit can generate the gate–source voltage which is proportional to the output current of an low dropout regulator for the MOS-resistor. Thus, the equivalent output resistance of the MOS-resistor is inversely proportional to the output current, which is a suitable feature for pole-zero tracking frequency compensation methods. By switching the type of the MOS-resistor and current direction through the auxiliary circuit, the controllable resistor can be suitable for different applications. Three pole-zero tracking frequency compensation methods based on a single Miller capacitor with nulling resistor, unit-gain compensation cell and pseudo-ESR (equivalent serial resistor of load capacitor) power stage have been realized by this controllable resistor. Their advantages and limitations are discussed and verified by simulation results.

Key words: controllable resistor; pole–zero tracking; single-Miller-capacitor with nulling resistor; unit gain compensation cell; pseudo-ESR power stage

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1. Introduction

1.1172.5Low dropout regulators (LDOs) are widely used in communication applications due to their low noise and fast response characteristics. But the wide range of output current introduces a great challenge in stability issues for the closed loop. Extensive research has been done on this aspect. In Ref. [1], a pole–zero tracking frequency compensation method was introduced by Kwok and Mok; a moving zero tracks the output pole of the LDO, thus a pole–zero cancellation is made to stabilize the loop. Recently, a pole-pole tracking method has been realized by a "power MOSFET array" in Ref. [2], which shows good stability, load and linear regulation response. An impedance-attenuation buffer with dynamically-biased shunt feedback has been used in Ref. [3] to stabilize the loop and achieve better transient response. Comparing the AC characteristics between heavy and light loads, the frequency compensation technology in Ref. [3] is another pole–pole tracking method. Also Ref. [4] can be categorized as using the same method with different realizations of the buffer stage.

Comparing two frequency compensation methods, pole-zero tracking and pole–pole tracking, the latter has undergone extensive development in recent years, and many different architectures have been proposed. The main reason is that the tracking-pole in the latter method is inherent in the loop; any changes of the tail current for the gain stage would affect the position of the corresponding output pole. Thus the circuits' implementation is relatively easy, and "dynamically-biased shunt feedback"[3] and the method of Ref. [4] are based on this idea. In the contrast, in order to introduce a zero in the loop transfer function, an additional signal path feed-forward or to ac-ground is needed; especially a serial connected resistor and capacitor should be included into such a signal path. For example, such a zero could be generated by "the nulling resistor in a Miller compensation"[5], "unit-gain compensation cell"[6] or a pseudo-ESR power stage, shown in Fig. 1. Furthermore, in order to achieve the "tracking" feature, the corresponding resistance should be inversely proportional to the output current. Although a MOS-resistor could be used to generate the variable resistor, the auxiliary circuit which produces the controllable source–gate voltage is the key for the pole–zero tracking frequency compensation method. Looking back to Mok's method[1], it does not fit the previously mentioned three zero generation methods. Since one node of the MOS-resistor should connect to supply voltage in Ref. [1], none of nodes of the corresponding resistor in Fig. 1 connects to supply voltage. In this paper, a suitable auxiliary circuit which can generate a controllable source–gate voltage for the MOS-resistor is developed. The simulation results show that this auxiliary circuit can significantly reduce the impact of process variation on the equivalent resistance, and even the influence of body effects has been eliminated. Also, the auxiliary circuit has been described in detail from the theory and simulation results. Three pole–zero tracking frequency compensation methods based on single Miller capacitor with nulling resistor, unit-gain compensation cell and pseudo-ESR power stage have been described with the simulation results. Their advantages and limitations are discussed.

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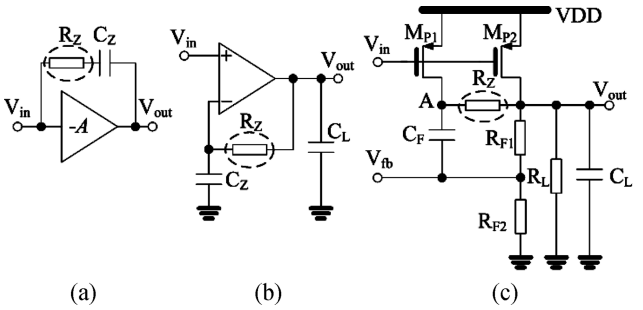

Fig. 1. Zero generation circuits, R_z in the dashed ellipse is the corresponding resistor used to generate the zero. (a) Single Miller capacitor with nulling resistor; (b) Unit gain compensation cell; (c) Pseudo-ESR power stage.

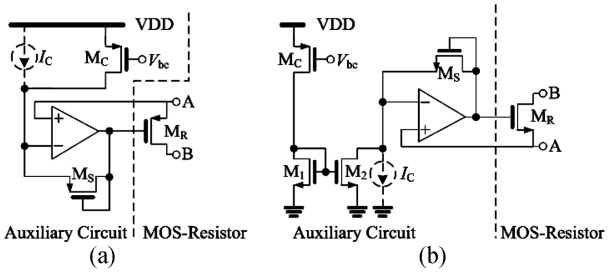

Fig. 2. Controllable resistor with auxiliary circuit, assuming that the current to be proportional is generated by a PMOS: (a) for P-type MOS-resistor; (b) for N-type MOS-resistor.

2. Controllable resistor and auxiliary circuit

Figure 2 shows the controllable resistor with the auxiliary circuit for both P-type and N-type MOS-resistors. As shown in Fig. 2, MR is the MOS-resistor, and nodes A and B represent the corresponding nodes for the equivalent resistor. The auxiliary circuit contains three parts: the current mirror MC (with additional M1 and M2 to change the direction of the mirrored current in Fig. 2(b)), a diode connected MOSFET of the same type of the MOS-resistor MS, and an operational amplifier to ensure the function. The architecture of the Opamp is different from application to application according to the operational point of nodes A and B; it will be discussed in detail in the next section. I_C is an optional constant current source, which is used to prevent MS from working in the sub-threshold region or the copied current being below the noise floor of the MOSFET.

The theory of the auxiliary circuit is simple: the Opamp held MS and MR have the same source voltage, as their sources are connected to Opamp's invert and non-invert inputs respectively. Then the current mirror copies the current that we want to be proportional to with a factor "α". The copied current will go through MS to generate the source–gate voltage with the gate voltage at the output of the Opamp. This gate voltage will be sent directly to the gate of MR. Since MS and MR have the same source voltage and their gates are connected together, then MR has the same source–gate voltage as MS which is proportional to the current that we require. Finally the equivalent resistor of MR is inversely proportional

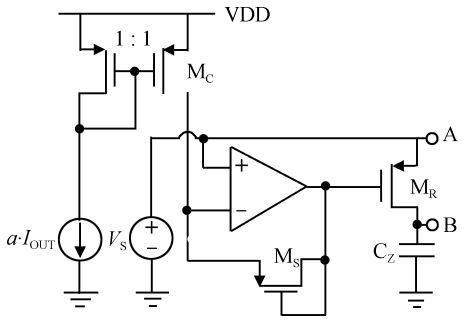

Fig. 3. Testing circuit for the controllable resistor.

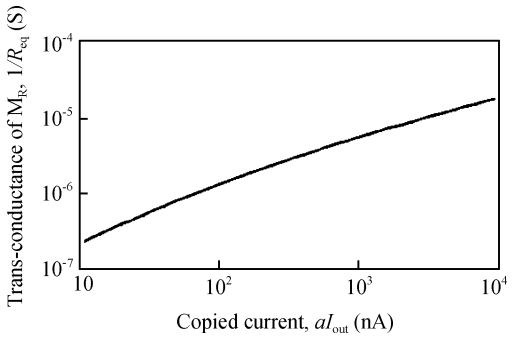

Fig. 4. Trans-conductance of MR, $1/R_{eq}$, against the copied current.

to the required variable current of the LDO. Below is the expression of the source–gate voltage, V_{GS}, and the equivalent resistor, R_{eq}. Suppose that the output current of the LDO is the current that we want to be proportional to:

$$|V_{GS}| = \sqrt{\frac{2\,(\alpha I_{out} + I_C)}{\mu C_{OX}\,(W/L)_{MS}}} + |V_{TH}|, \tag{1}$$

$$R_{eq} = \frac{1}{\mu C_{OX}\,(W/L)_{MR}\,|V_{GS} - V_{TH}|} = \frac{\sqrt{(W/L)_{MS}}}{(W/L)_{MR}\,\sqrt{2\mu C_{OX}\,(\alpha I_{out} + I_C)}}. \tag{2}$$

As shown in Eq. (2), the threshold voltage has been cancelled in the calculation, if MS and MR used the same type of MOS transistor; thus the impact of process variation has been suppressed. Moreover, since MS and MR have the same source voltage, the influence of body effects on them is almost the same, and then this issue can be ignored in the circuit design. A testing circuit has been built and is shown in Fig. 3 to verify these aspects. The testing circuit has two input signals "V_A" and "αI_{out}" generated by a voltage source and a current source respectively to represent the source voltage of MS and MR, and the copied current by the current mirror. A capacitor, C_Z, has been placed between node B and ground to cut off the DC path of MR; then MR will work in the deep triangle region, and it will be the working condition for MR if it replaces the R_Z in Figs. 1(a) and 1(b).

Figure 4 shows the simulation results of the trans-conductance of the equivalent resistor against the copied current, when the latter changes from 10 nA to 10 μA. As shown in the figure, $1/R_{eq}$ is proportional to the square root of the copied current, "αI_{out}", thus Equation (2) has been verified.

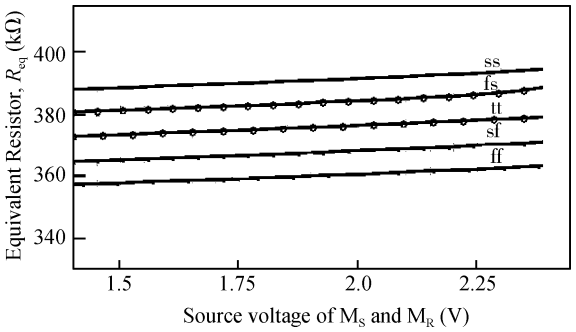

Fig. 5. Equivalent resistance of MR against the source voltage of MS and MR under process variation with 300 nA fixed copied current.

Figure 5 shows the equivalent resistance of MR against the source voltage of MS and MR under process variation with 300 nA fixed copied current. When considering the process variation and changes of source voltage, the equivalent resistance only changes by ±4.7%. The size W/L of MS and MR are 10 μm/5 μm and 10 μm/10 μm respectively.

$|V_{GS,\max}|$ represents the largest source–gate voltage in absolute value of MR, which occurs when the copied current has its maximum value. When considering the limitation of the Opamp's output in Fig. 3 and the same source–gate voltage between MS and MR, then the following choices can be made. If $V_{DD}-V_A > |V_{GS,\max}|$, a P-type MOS-resistor could be used; and if $V_A - V_{SS} > |V_{GS,\max}|$, a N-type MOS-resistor could be used. The architecture of the Opamp in the auxiliary should fulfill the requirement of operation point of input voltage (V_A) and output range which is decided by the variation of copied current and size of MS. And during the circuit's design, node A should connect to more stable points in order to relax the requirement of the Opamp in the auxiliary circuit. In the following section, three pole-zero tracking frequency compensation methods based on this controllable resistor are given and analyzed.

3. Pole-zero tracking frequency compensation methods

3.1. Single Miller capacitor with nulling resistor (SMCNR)

The single Miller capacitor is widely used in multiple-stage operational amplifier frequency compensations, and the nulling resistor is usually used to eliminate the zero in the right-half-plane (RHP). If the nulling resistor is large enough, the corresponding zero will come into the left-half-plane (LHP) which can be used to cancel a pole in the loop transfer function, and then help the loop to achieve better stability. Figure 6 shows a 3-stage LDO with pole-zero tracking method based on single Miller capacitor frequency compensation and nulling resistor. Here the nulling resistor is formed by a MOS-resistor and is controlled by the auxiliary circuit. The supply voltage is 3.3 V and output voltage is 3 V with 150 mA maximum output current and 1 μF load capacitor. The first gain stage is a telescope cascode structure to provide high gain and high output impedance; thus with a Miller capacitor, the dominant pole will be located on the output of the first gain stage. The second gain stage is a simple common source amplifier with Miller capacitor and the third gain stage (power stage) is traditionally formed by a PMOS transistor with load resistor and capacitor. C_E in Fig. 6 is the total parasitic capacitor looking at the node A (or the output of the first gain stage). Since the output voltage of the first gain stage is the most stable one for all current loads, the MOS-resistor is connected to this node other than the output of the second gain stage. The open-loop transfer function is:

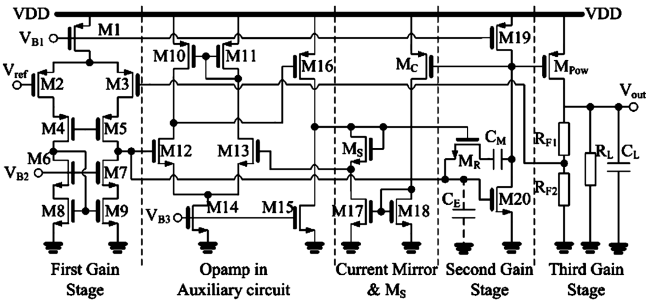

Fig. 6. Three-stage LDO with Miller capacitor frequency compensation, and the nulling resistor is controllable to form a tracking zero by the auxiliary circuit.

$$A(s) = g_{m1}g_{m2}g_{m3}r_{O1}r_{O2}R_L \times \frac{1+\left(R_{eq}-1/g_{m2}\right)C_M s}{(1+g_{m2}r_{O1}r_{O2}C_M s)\left(1+\dfrac{C_M s}{g_{m2}}\right)(1+R_L C_L s)\left(1+R_{eq}C_E s\right)}, \tag{3}$$

where g_{mi} and r_{Oi} are the circuit's trans conductance and output resistance of the ith gain stage, and R_{eq} is the equivalent resistance of MR with the expression shown in Eq. (2). As shown in Eq. (3), the loop has 4 poles and a zero given by:

$$P_1 = 1/g_{m2}r_{O1}r_{O2}C_M, \tag{4}$$

$$P_2 = g_{m2}/C_M, \tag{5}$$

$$P_3 = 1/R_L C_L = I_{out}/V_{out}C_L, \tag{6}$$

$$P_4 = \frac{1}{R_{eq}C_E} = \frac{(W/L)_{MR}\sqrt{2\mu C_{OX}(\alpha I_{out}+I_C)}}{C_E\sqrt{(W/L)_{MS}}}, \tag{7}$$

$$Z_1 = \frac{1}{\left(R_{eq}-1/g_{m2}\right)C_M} \approx \frac{(W/L)_{MR}\sqrt{2\mu C_{OX}(\alpha I_{out}+I_C)}}{C_M\sqrt{(W/L)_{MS}}}. \tag{8}$$

According to Eqs. (4)–(8), P_3 is proportional to the I_{out}; P_4 and Z_1 are proportional to the square root of I_{out}; and P_4 and Z_1 have fixed ratio C_M/C_E. So the frequency compensation scheme is that at the heavy load of the LDO, Z_1 is used to cancel P_2, and P_3 and P_4 are out of the unit gain bandwidth; at the light load, Z_1 and P_3 are moving to lower frequency, thus Z_1 is used to cancel P_3, and P_2 and P_4 are out of the unit gain bandwidth. Figures 7 and 8 show the AC simulation results and load regulation response of the proposed design. The

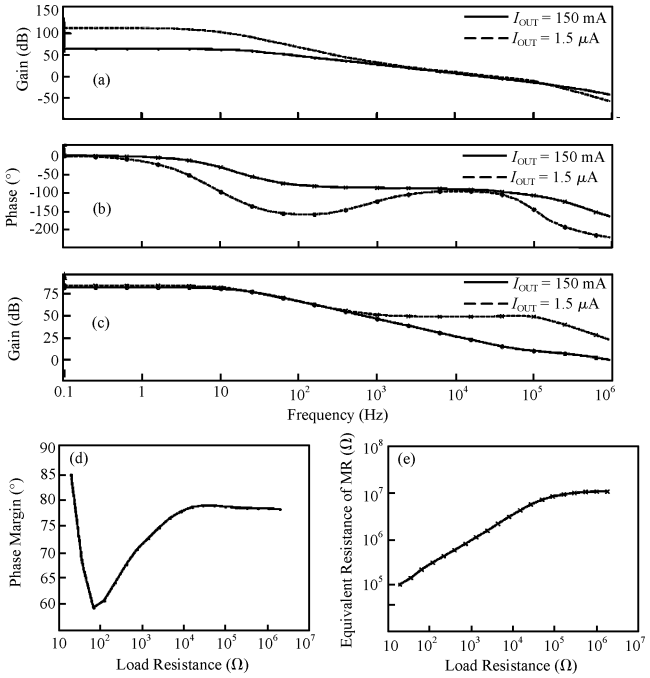

Fig. 7. AC simulation results of Miller capacitor compensation with controllable resistor under heavy load (I_{out} = 150 mA) and light load (I_{out} = 1.5 μA): (a) Loop gain; (b) Loop phase; (c) Total gain of first and second gain stage; (d) Phase margin under all current load; (e) Equivalent Resistance of MR under all current load.

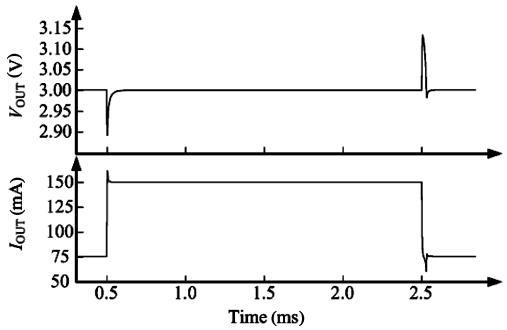

Fig. 8. Load regulation response of the LDO when I_{out} changes between 75 mA and 150 mA for SMCNR LDO.

gains of first and second gain stages are observed together to see the effect of Miller capacitor compensation with controllable resistor in Fig. 7(c), the moving Z_1 and the cancellation of Z_1 and P_2 at the heavy load can be seen clearly in this figure. Figure 7(d) ensures the stability of the loop under all current loads. In Fig. 7(e), R_{eq} does not rise linearly with load resistor at large resistance due to the limitation of current mirror, but the stability has been ensured by the minimum value of Z_1 that can be reached.

A large Miller capacitor about 20 pF is used here to enlarge the ratio between P_4 and Z_1, so that P_4 will always be outside of the unit gain bandwidth in order not to degrade the phase margin of the loop.

3.2. Unit gain compensation cell (UGCC)

A unit gain compensation cell with controllable resistor is built based on the research on Ref. [6], in order to reduce

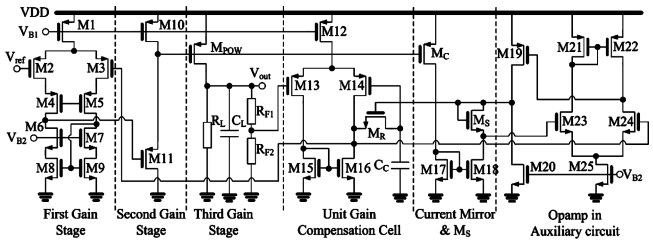

Fig. 9. Three-stages LDO based on unit gain compensation cell with controllable resistor.

the impact of process (SMIC 0.18 μm in Ref. [6] and TSMC 0.35 μm in the proposed design) on two designs; the supply and output voltages have been doubled to 2.4 and 2 V respectively; the maximum output current is 100 mA and load capacitor is 10 μF, all of which are the same as in Ref. [6]. Figure 9 shows the topology of the proposed design. "M5" in Ref. [6] is replaced by MR here, since the gate of "M5" in Ref. [6] is connected to ground, thus process variation and body effects would impact the location of "ω_{ZC}" in Ref. [6]. This problem has been solved in the proposed design and simulation results in section 2 have verified the method. The transfer function of the loop in proposed design shown in Fig. 9 is given by:

$$A(s) = g_{m1}g_{m2}g_{m3}r_{O1}r_{O2}R_L \times \frac{1}{(1+r_{O1}C_{L1}s)(1+r_{O2}C_{L2}s)(1+R_LC_Ls)} \times \frac{A_U\left(1+R_{eq}C_Cs\right)}{1+A_U+R_{eq}C_Cs+r_{OU}C_{LU}s+r_{OU}C_Cs+R_{eq}C_Cr_{OU}C_{LU}s^2}. \quad (9)$$

where C_{Li} is the circuit's load capacitance of the ith gain stage, and R_{eq} is the equivalent resistance of MR with the expression shown in Eq. (2). A_U, r_{OU} and C_{OU} are the loop gain, output resistance and load capacitor of the UGCC. Based on Eq. (9), the loop has 5 poles and a zero given by:

$$P_1 = 1/r_{O1}C_{L1}, \quad (10)$$

$$P_2 = 1/r_{O2}C_{L2} \approx g_{M11}/C_{L2}, \quad (11)$$

$$P_3 = 1/R_LC_L = I_{out}/V_{out}C_L, \quad (12)$$

$$Z_1 = \frac{1}{R_{eq}C_C} \approx \frac{(W/L)_{MR}\sqrt{2\mu C_{OX}(\alpha I_{out}+I_C)}}{C_C\sqrt{(W/L)_{MS}}}. \quad (13)$$

The positions of P_4 and P_5 are dependent on the ratio between $r_{OU}C_{OU}$ and $R_{eq}C_C$.

Case 1: if $1/R_{eq}C_C \ll 1/r_{OU}C_{OU}$, then:

$$P_4 \approx A_U/R_{eq}C_C, \quad P_5 \approx 1/r_{OU}C_{LU}. \quad (14)$$

Case 2: if $1/R_{eq}C_C \approx 1/r_{OU}C_{OU}$, then P_4 and P_5 will be a pair of complex pole located at:

$$P_4 = P_5 \approx \sqrt{A_U/R_{eq}C_Cr_{OU}C_{LU}}. \quad (15)$$

Case 3: if $1/R_{eq}C_C \gg 1/r_{OU}C_{OU}$, then:

$$P_4 \approx 1/R_{eq}C_C, \quad P_5 \approx A_U/r_{OU}C_{LU}. \quad (16)$$

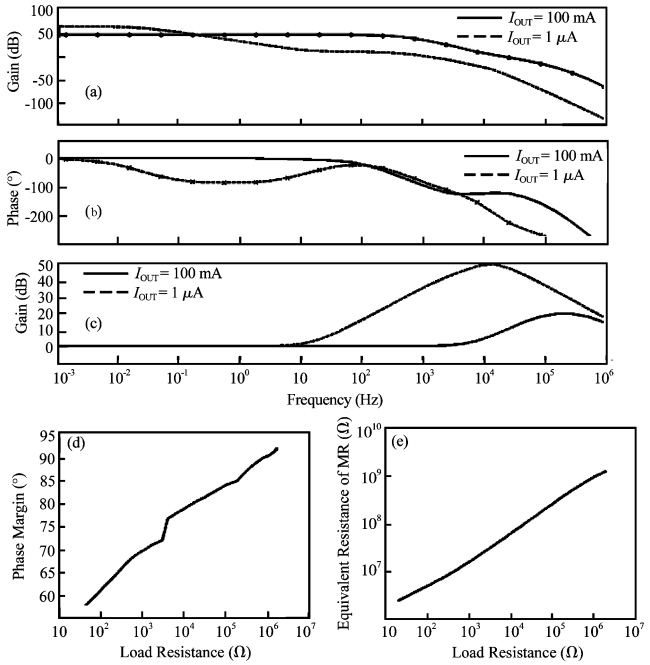

Fig. 10. AC simulation results of UGCC with controllable resistor under heavy load (I_{out} = 100 mA) and light load (I_{out} = 1 μA): (a) Loop gain; (b) Loop phase; (c) Gain of UGCC; (d) Phase margin under all current load; (e) Equivalent resistance of MR under all current loads.

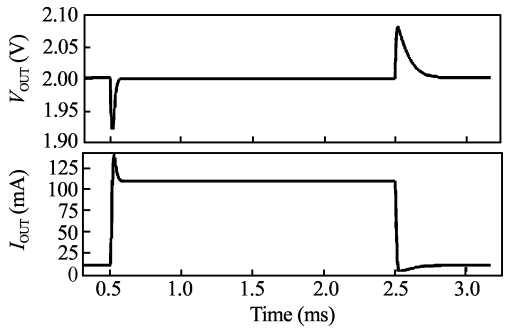

Fig. 11. Load regulation response of LDO when I_{OUT} changing between 10 mA and 100 mA for UGCC LDO.

In the circuits' implementation, case 3 should be avoided to stabilize the loop; cases 1 and 2 can be accepted, if both P_4 and P_5 are out of the unit gain bandwidth. Furthermore, the ratio between Z_1 and P_4 will increase with larger R_{eq} in case 2, according to Eqs. (13) and (15). This is the situation that occurs in the proposed design.

As a source-follower has been used for the second stage, P_2 has been pushed out of the unit gain bandwidth, while P_1 and P_3 are inside of the cross point of the loop gain. Z_1 is used to cancel P_3 at the heavy load, and cancel P_1 at the light load. Figures 10 and 11 show the AC simulation results and load regulation response of the proposed design. The cancellation strategy can be seen by the comparison of heavy load and light load frequency response shown in Figs. 10(a) and 10(b). In Fig. 10(c), the tracking zero can be observed by the frequency characteristic of the UGCC. Since there is no slew-rate-enhancement circuit in the proposed design, a longer time is needed for EA to drive the power transistor, thus the response time is about 500 μs in Fig. 11. C_C in the proposed

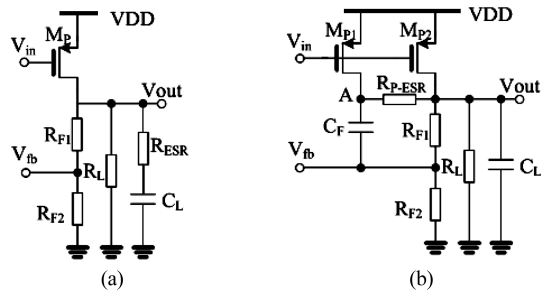

Fig. 12. (a) Traditional ESR circuit; (b) Power stage and feedback network with pseudo-ESR.

design is 10 pF, and 10 μF load capacitor with no ESR can be used.

3.3. Pseudo-ESR power stage (P-ESR PS)

The ESR of the load capacitor is used to introduce a zero into the transfer function to stable the loop in the traditional design. But for commercial requirements, a low ESR load capacitor is usually used in recent designs. Thus a pseudo-ESR inside of the chip for gain stage has been developed to form a new frequency compensation method. In the traditional ESR circuit, the frequency of the zero can be easily calculated as

$$Z_{ESR} = \frac{1}{C_L R_{ESR}}. \tag{17}$$

If we neglect the M_{P2} and C_F in Fig. 12(b), the remaining circuit is quite similar to the traditional ESR circuit, based on the small signal model of the topology shown in Fig. 12(b); the expressions for poles and zeros are given by:

$$Z_1 = g_{m,P2}/g_{m,P1}C_L R_{P\text{-}ESR} = g_{m,P2}\Big/\left(g_{m,P1}C_L R_{eq}\right), \tag{18}$$

$$Z_2 = 1/C_F R_{F1}, \tag{19}$$

$$P_3 = 1/R_L C_L, \tag{20}$$

$$P_4 = 1/C_F\left(R_{F1}//R_{F2}\right). \tag{21}$$

Since the feedback ratio is small in the application, Z_2 and P_4 are cancelled by each other. In order to couple the Z_1 from node A to node V_{fb}, Z_2 should follow the requirement:

$$Z_F = \frac{1}{C_F R_{F1}} < \frac{1}{C_L R_{P\text{-}ESR}}\frac{g_{m,P2}}{g_{m,P1}} = Z_1. \tag{22}$$

The first two gain stages and the auxiliary circuits with the pseudo-ESR power stage are shown in Fig. 13 to form a 3-stage LDO. The rest of the poles in the transfer function are given by:

$$P_1 = 1/r_{O1}C_{L1}, \tag{23}$$

$$P_2 = 1/r_{O2}C_{L2}. \tag{24}$$

Thus the whole transfer function for the loop gain is given by:

$$A(s) = g_{m1}g_{m2}g_{m3}r_{O1}r_{O2}R_L \times \frac{\left(1 + g_{m,P1}R_{eq}C_L s\Big/g_{m,P2}\right)\left(1 + R_{F1}C_F s\right)}{\left(1 + r_{O1}C_{L1}s\right)\left(1 + r_{O2}C_{L2}s\right)\left(1 + R_L C_L s\right)\left[1 + \left(R_{F1}//R_{F2}\right)C_F s\right]}. \tag{25}$$

In this application, P_1 has been pushed out of the unit gain bandwidth, while P_2 and P_3 are inside of the cross point of the

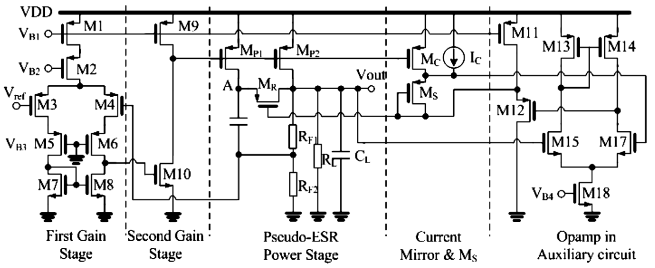

Fig. 13. Three-stage LDO based on pseudo-ESR power stage with controllable resistor.

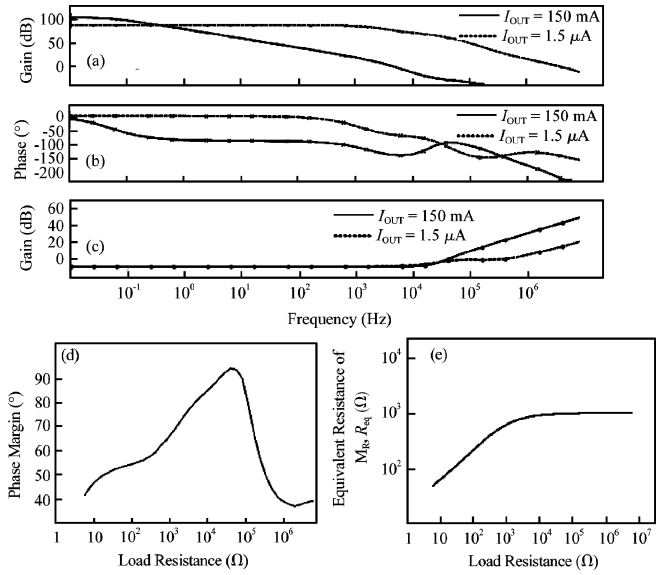

Fig. 14. AC simulation results of pseudo-ESR power stage with controllable resistor under heavy load (I_{out} = 100 mA) and light load (I_{out} = 1 μA): (a) Loop gain; (b) Loop phase; (c) Gain of UGCC; (d) Phase margin under all current load; (e) Equivalent resistance of MR under all current load.

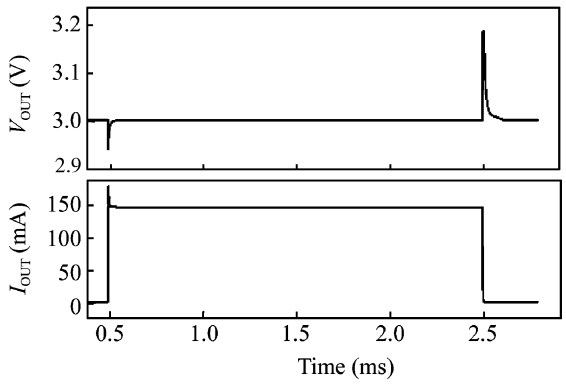

Fig. 15. Load regulation response of the LDO when I_{OUT} changes between 1.5 A and 150 mA for the LDO with pseudo-ESR power stage.

loop gain. At the heavy load, Z_1 moves to higher frequency to reduce the unit gain frequency, thus the impact on phase margin caused by P_1 has been reduced; at the light load, Z_1 moves towards P_2 to make a pole–zero cancellation to stabilize the loop. The minimum location of Z_1 has been fixed by a constant current source I_C in Fig. 13. Figures 14 and 15 show the AC simulation results and load regulation response of the proposed design. The tracking zero can be observed in the frequency characteristics of the feedback network, as the Z_1 has been coupled from node A to V_{fb} in Fig. 4(c). The limitation for minimum value of Z_1 is verified by the fixed maximum value of R_{eq} shown in Fig. 14(e). The load regulation response shown in Fig. 15 ensures the stability of proposed design. The value of C_F is 4 pF, and low ESR load capacitor can be used here.

4. Discussion

Compared with the MOS-resistor with a fixed bias, the present controllable resistor overcomes the deviation caused by process variation and body effects, thus it is more suitable to replace the passive resistors in the chip to conserve area.

Compared with the fixed zero in Ref. [6], the pole–zero tracking method presented in section 3.2 can stabilize the loop without ESR and restrict the quiescent current from 20.5 to 10.3 μA which is closer to commercial requirements.

Compared with the traditional pole–zero tracking method[1], the presenting controllable resistor provides greater freedom on the connecting of the MOS-resistor, and then different kinds of topologies can be built which place extra emphasis on power consumption or gain bandwidth production respectively.

The three compensation methods are compared in the following aspects:

(a) Circuit complexity: how many differential amplifiers (D) and single stage amplifiers (S) are used in the proposed designs.

(b) Power consumption: including the quiescent current and the dynamic current. The latter is caused by the current mirror in the auxiliary circuit and depends on the factor "α" in Eqs. (1) and (2).

(c) Gain-bandwidth production (GBP): since the gain and bandwidth of the open loop varies from different current loads, GBP has been considered here. Here higher GBP means more accuracy and faster response speed.

(d) Poles' and zeros' distribution: The poles and zeroes are sorted by their locations, from lower frequency to higher frequency. The distribution also implies maximum bandwidth and the cost of quiescent current to push the poles. The poles or zeros in parenthesis mean that they are out of the cross point of the loop gain.

Table 1 gives the performances of three compensation methods based on such specifications. As shown in Table 1, the SMCNR method has minimum GBP and quiescent current. Since $P_{1,SMCNR}$ is located at very low frequency, less than 10 Hz, so less tail current is assigned to the first gain stage. As a results of high output resistance of the first stage and pole splitting effects caused by the Miller capacitor, the SMCNR method has a minimum bandwidth of about 6 kHz for the cross point of the loop gain. This topology is suitable for low power consumption applications, but the response speed is low and needs a slew-rate-enhancement circuit to improve the transient response.

Table 1. Performance of three compensation methods.

Parameter		SMCNR	UGCC	P-ESR PS
Circuits' complexity		2D3S	3D3S	2D3S
Quiescent current (μA)		5.13	10.3	33.1
Dynamic current, "α"		1.78×10^{-3}	0.71×10^{-3}	0.012×10^{-3}
Gain bandwidth production (dB·Hz)		0.67×10^{6}	3.78×10^{6}	69.8×10^{6}
Pole and zero distribution	Heavy load	$P_1 < P_2 < Z_1 < (P_3) < (P_4)$	$P_1 < P_3 < Z_1 < (P_2) < (P_4) < (P_5)$	$P_2 < P_3 < Z_2 < P_4 < Z_1 < (P_1)$
	Light load	$P_1 < P_3 < Z_1 < (P_2) < (P_4)$	$P_3 < P_1 < Z_1 < (P_2) < (P_4) < (P_5)$	$P_3 < P_2 < Z_2 < P_4 < Z_1 < (P_1)$

The UGCC method has the most complex circuitry, since the unit gain compensation cell and auxiliary circuit for the controllable resistor each need a differential amplifier. More tail current is needed to push two poles, P_4 and P_5, in the UGCC out of the unit gain bandwidth, so additional quiescent current is used. A source follower has been placed as the second gain stage here, which sacrifices DC gain to achieve higher bandwidth.

The pseudo-ESR power stage will cost the most quiescent current as it needs to push P_1 out unit gain bandwidth to achieve faster response speed and higher PSR at the high frequency. Since Z_1 is not needed to track P_3 firmly among all the current loads, minimum dynamic current is used here as factor "α" is only 0.012×10^{-3} for the pseudo-ESR power stage.

5. Conclusion

A controllable resistor has been introduced in this paper. Using this technology, three pole–zero tracking frequency compensation methods have been developed based on a single Miller capacitor with nulling resistor, unit gain compensation cell and pseudo-ESR power stage. Both the load regulation response and the AC simulation for open loop including loop gain, phase, tracking zero, phase margin and equivalent resistance under all current loads are shown in corresponding sections. According to the simulation results, the three compensation methods can ensure the stability of the LDO without ESR in the load capacitor, and they provide frequency compensation solutions from low power consumption applications to high PSR, high response speed applications.

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