A semi-empirical analytic model for threshold voltage instability in MOSFETs with high-*k* gate stacks*

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Abstract: A semi-empirical analytic model for the threshold voltage instability of a MOSFET is derived from Shockley–Read–Hall (SRH) statistics to account for the transient charging effects in a MOSFET high-*k* gate stack. Starting from the single energy level and single trap assumption, an analytical expression for the filled trap density in terms of dynamic time is derived from SRH statistics. The semi-empirical analytic model for the threshold voltage instability is developed based on MOSFET device physics between the threshold voltage and the induced trap density. The obtained model is also verified by extensive experimental data of trapping and de-trapping stress from different high-*k* gate configurations.

Key words: high-*k* gate stack; nanoscale MOSFETs; interface trap and charges; trapping and detrapping; threshold voltage dynamic behavior; compact modeling

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1. Introduction

The 2004 International Technology Roadmap for Semiconductors (2004 ITRS) proposes the use of high-*k* dielectrics to extend CMOS scaling to its limit[1–8]. High-*k* gate dielectrics are actually required for the sub-65 nm MOS structure because conventional SiO_2 film is too thin, e.g. 1 nm to minimize the tunneling current and the out-diffusion of boron from the gate. A thick layer can be used with high-*k* material to lower the gate tunneling and the parasitic capacitance between the gate and the source (and drain). Many issues, however, have to be solved before this is acceptable for the products. For example, use of the high-*k* dielectric will lead to dynamic behavior like hysteresis in drain current[9], instability of the threshold voltage[10–14] and degradation of mobility[15], which definitely affect the device and circuit performance. In order to benchmark test and design nano-scale circuits with high-*k* MOSFETs, it is thus necessary for the CAD simulation to develop compact models to capture such dynamic behavior.

A semi-empirical analytic model for threshold voltage instability of MOSFETs is developed from basic Shockley–Read–Hall (SRH) statistics in this paper to account for the transient charging effects in a high-*k* gate structure. In order to develop the analytic model, single energy level and single trap simplifications are used. Under the single energy level and single trap assumption an analytical expression for the trap density in terms of dynamic time is derived from the SRH statistics equation. Following this theoretical result, the semi-empirical analytic model for the threshold voltage instability is developed based on the MOSFET device physics between the threshold voltage and the induced trap density with the inclusion of multiple energy level and trap effects. Finally, the analytic behavior model is also verified by extensive experimental data from different high-*k* gate transistors and corresponding different trapping and de-trapping stress, indicating the validity of the analytic model.

2. Analytic model development

It is well known that electrons and holes entering the gate stack get trapped and de-trapped, thus resulting in dynamic behavior of MOSFET performance. Sources of trap carriers may be the gate current, direct tunneling to trap, and indirect tunneling from interfacial traps[16]. Figure 1(a) indicates different kinds of traps and trapping mechanisms through which trapping/de-trapping comes into effect. Different parts of the high-*k* gate stack are indicated, and the oxide thickness is supposed to be T_{IL}. The sum of direct and indirect tunneling forms the gate leakage current J_G.

Therefore, the trapping and de-trapping processes can be described by SRH statistics. According to SRH statistics with the assumption of single energy level and single trap as shown in Fig. 1(b), the filled trap probability variation with time is modeled by the probability equation:

$$\frac{\mathrm{d}f_t}{\mathrm{d}t} = \left(c_n n + c_p p\right)\frac{N_t}{n_t} - \left(e_n + c_n n + e_p + c_p p\right) f_t, \qquad (1)$$

where N_t is the available trap density, c_n and e_n are specific trap constants for the electron trapping mechanism, e.g. capture and emission coefficient, c_p and e_p are hole trapping spe-

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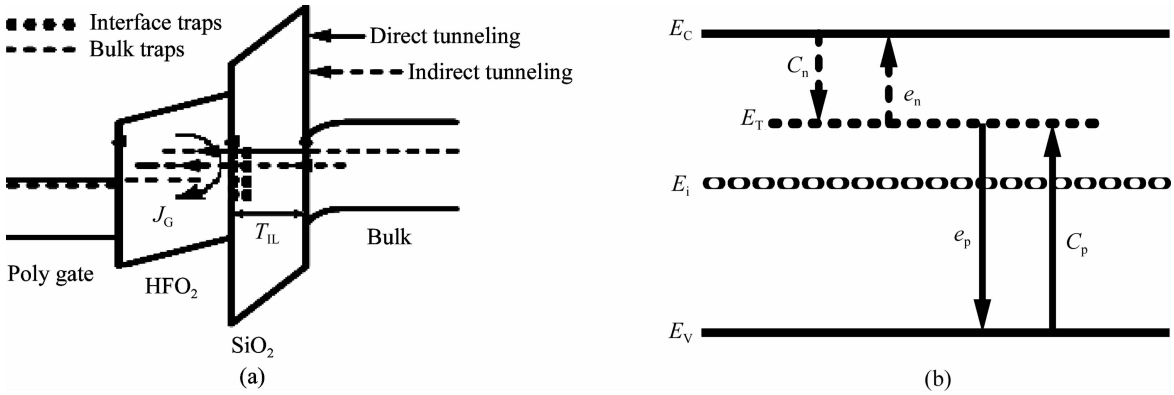

Fig. 1. (a) Possible trapping/de-trapping mechanisms and (b) SRH model using single trap energy in a high-k gate stack.

cific trap constants, n and p are electron and hole densities, and E_T is the trap level.

For n-MOSFETs in strong inversion ($n \gg p$) and for trap energies close to E_C[15], the hole-related terms can be neglected; the filled trap density is modeled as

$$\frac{dn_t}{dt} = c_n n (N_T - n_t) - e_n n_t. \tag{2}$$

For thin interface layers, direct tunneling is the main source of carriers. Consider a case where traps are located at the bottom interface of the high-k layer, so there is a two-step process: carriers tunnel from the inversion layer to the trap position and carriers get trapped at the trap position. If the tunneling probability that a carrier can reach the edge of the interface layer follows the general tunneling current, the capture constant c_n is given by the WKB approximation:

$$c_n = c_{n0} \exp\left[-\frac{4\sqrt{2m}}{3\hbar}\frac{t_{oxe}}{V_{oxe}}\sqrt[3/2]{\phi_B}\left(1 - \frac{V_{oxe}t_{IL}}{\phi_B t_{oxe}}\right)\right] \approx \frac{kJ_g}{n}, \tag{3}$$

where $J_g \propto \exp(-t_{IL}, V_{ox})$.

The WKB approximation is employed to show that $c_n \propto \exp f_n(-t_{IL}, V_{ox})$ for different trapping mechanisms, where V_{ox} is the voltage across the high-k layer and t_{IL} is the thickness of the high-k layer. Thus, the capture constant exhibits a similar exponential dependence on gate voltage and insulator thickness. Indirect tunneling will also have an exponential dependence through the tunneling probability term. If trapping dominates through gate current carriers and capture and emission exist simultaneously, we have:

$$\frac{dn_t}{dt} = kJ_g N_T - Rn_t, \tag{4}$$

where

$$R = c_n n + e_n,\ e_n = e_{n0} \exp\frac{E_t - E_f}{kT} = e_{n0} \exp\frac{q\Delta\phi_s}{kT}. \tag{5}$$

On performing the integral of Eq. (4), one can obtain an analytic expression for the filled trap density as shown in Eq. (6):

$$n_t = \frac{J_g N_T}{R}\left[1 - e^{-Rt}\right]. \tag{6}$$

Since trapping and de-trapping of charges in interfacial and bulk traps results in dynamic behavior from the perspective of MOSFET device physics[16], all dynamic behavior can be modeled through the change in the MOSFET threshold voltage. Based on MOSFET device physics, $\Delta V_{th} \propto V_{FB} \propto (Q_{it}/C_{ox})$, and considering the impact of stress gate voltage, we have:

$$\Delta V_{th} = \frac{qn_t}{C_{high-k}} = \frac{qJ_g N_T t_{HfO_2}}{R\varepsilon_0\varepsilon_{HfO_2}} \exp(BV_s)\left[1 - \exp(-\beta R t^m V_s^b)\right]. \tag{7}$$

Here, β, b, m and B are the fitting parameters, and V_s is the stress gate voltage.

In order to make the analytic model capture the complex characteristics of the trapping and de-trapping density coming from the different sources and mechanisms, e.g. emission and capture effects and direct and indirect tunneling processes, semi-empirical coefficients and correction exponential factors have to be introduced as shown in Eq. (8).

$$\Delta V_{th} = kn_t = \frac{kJ_g N_T}{R^\alpha}\left[2 \mp e^{-R\beta_1 t^{m_1}} \mp e^{-R\beta_2 t^{m_2}}\right]. \tag{8}$$

Here, k, α, β and m are the fitting parameters and the tunneling current density follows the physics based expression as shown in BSIM5[17]. The value of the sign function of Eq. (8) depends on the stress condition: the sign function should take a positive value for the de-trapping transient while keeping a negative value for the trapping transient period.

3. Results and discussion

In order to test our analytic model, different high-k gate dielectric configurations are measured and then the threshold voltage shift is extracted for the stress time and stress bias[9]. The physical thickness of the SiO_2 film, the high-k dielectric and the gate voltage are put into the corresponding expressions to model the gate tunneling and the capture/emission constant. Then, Equation (7) is used to fit the experimental data to the extracted β, b, m and B. The details of the parameters for a sample with 4.5 nm thickness and 800 °C N_2 annealing are $T = 1073$ K, $\varepsilon_{HfO_2} = 5$, $N_T = 5 \times 10^{10}$ cm^{-2}, $R = 1.55 \times 10^3$, $m = 0.365$, $t_{HfO_2} = 4.5$ nm, $B = 4$, $J_g = 0.16$ A/cm, $\beta = 1.26 \times 10^{-3}$, $b = 1.65$.

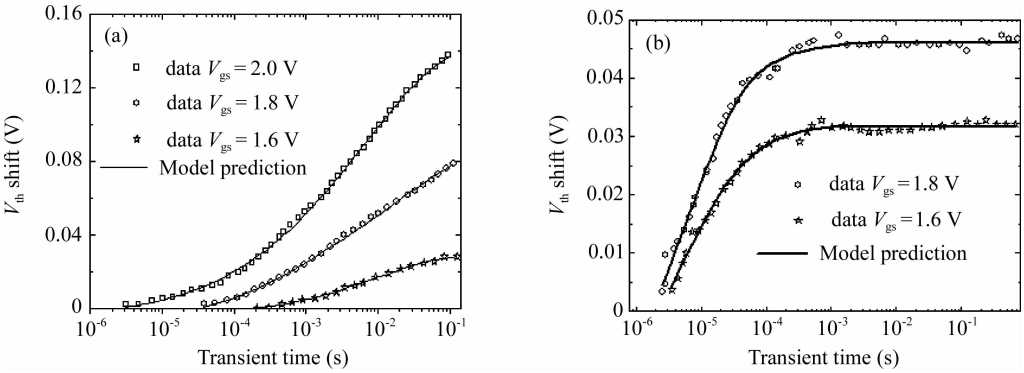

Fig. 2. Comparison of analytic model prediction and experiment-extracted data showing the threshold voltage increase due to the trapping mechanism: (a) 4.5 nm HfO_2, 800 °C N_2 annealing; (b) 3 nm HfO_2, 600 °C N_2 annealing.

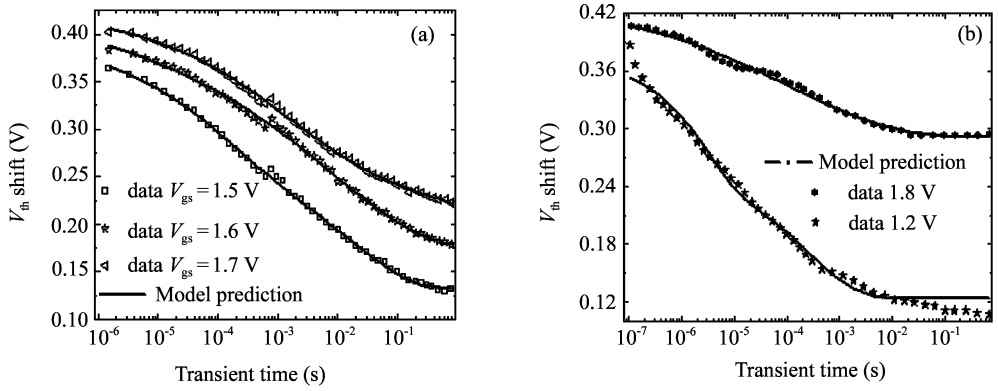

Fig. 3. Comparison of analytic model prediction and experiment-extracted data showing the threshold voltage decrease due to the de-trapping mechanism: (a) 4.5 nm HfO_2, 600 °C PDA; (b) 4.5 nm HfO_2, 600 °C N_2 annealing.

The relationship between part parameters and temperatures is obtained based on the exact values at 800 °C N_2 annealing

$$\begin{cases} R = R_0 T_0 \exp(-T_0/T)/T, \\ B = B_0 T/T_0. \end{cases} \tag{9}$$

For the experimental sample HfO_2 gate stack with 4.5 nm thickness and 800 °C annealing under N_2 atmosphere, the measured stress condition is from 1.6 to 2 V with a transient time of 1 s, the extracted threshold voltage instability is plotted in Fig. 2(a) with points and the model prediction is also shown in this figure with lines. It is easily seen that the analytic model matches the experimentally measured V_{th} shifts well[9].

Under stress conditions of 1.8 V and 2 V with a transient time of 1 s, the experimental sample 3 nm HfO_2 gate stack with 600 °C N_2 annealing shows a significant difference compared with the first sample in the dynamic behavior of the threshold voltage as shown by the points in Fig. 2(b). Here, the induced trap density demonstrates a clear saturation trend at early transient times. One can observe that, however, the analytic model matches the experimentally measured V_{th} shifts well, as shown in Fig. 2(b).

It is interesting that the presented analytic model can be used to model the dynamic change in V_{th} for de-trapping[9]. Figure 3 demonstrates that the analytic model prediction is in good agreement with experimental data for different V_{th} shifts for 4.5 nm HfO_2, 600 °C PDA and 4.5 nm HfO_2, 600 °C N_2 annealing.

4. Conclusions

A semi-empirical analytical model is developed in this paper to characterize the threshold voltage shift transients in high-k MOSFETs as a function of dynamic time. To capture dynamic behavior of the threshold voltage and model the various experiment results, the analytic filled trap density is derived from SRH statistics and semi-empirical coefficients and correction terms are introduced into the threshold voltage expression. The analytic model prediction is also in agreement with experimental data, demonstrating the model's validity to efficiently incorporate the threshold voltage dynamic behavior into any compact model framework used in VLSI circuit simulators.

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