A fast-hopping 3-band CMOS frequency synthesizer for MB-OFDM UWB system*

Zheng Yongzheng(郑永正), Xia Lingli(夏玲琍), Li Weinan(李伟男), Huang Yumei(黄煜梅)†, and Hong Zhiliang(洪志良)

(State Key Laboratory of ASIC & System, Fudan University, Shanghai 201203, China)

Abstract: A fast-hopping 3-band (mode 1) multi-band orthogonal frequency division multiplexing ultra-wideband frequency synthesizer is presented. This synthesizer uses two phase-locked loops for generating steady frequencies and one quadrature single-sideband mixer for frequency shifting and quadrature frequency generation. The generated carriers can hop among 3432 MHz, 3960 MHz, and 4488 MHz. Implemented in a 0.13 μm CMOS process, this fully integrated synthesizer consumes 27 mA current from a 1.2 V supply. Measurement shows that the out-of-band spurious tones are below −50 dBc, while the in-band spurious tones are below −34 dBc. The measured hopping time is below 2 ns. The core die area is 1.0×1.8 mm^2.

Key words: frequency synthesizer; phase-locked loop; ultra-wideband; CMOS
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1. Introduction

Due to its high channel capacity, the ultra-wideband (UWB) system is an attractive solution for the implementation of high data rate short-range wireless networks. The multi-band OFDM alliance (MBOA) proposal divides the unlicensed band of 3.1–10.6 GHz into 14 sub-bands with a spacing of 528 MHz[1, 2]. These sub-bands are grouped into five groups as illustrated in Fig. 1. Only the first band group, corresponding to the lower part of the spectrum (3.1–4.8 GHz), is considered as mandatory by the current standard proposal for MB-OFDM UWB system. The center frequencies for the three mandatory bands are 3432 MHz, 3960 MHz, and 4488 MHz. Due to the large signal bandwidth, direct conversion is the most promising architecture for UWB radio and consequently the local oscillator (LO) needs to generate the center frequencies of all the bands in use, with a maximum transition time of 9.5 ns. Furthermore, in direct-conversion architecture, the transceiver's LO needs to provide quadrature (I/Q) signals. The generation of the center frequencies cannot be done using a conventional phase-locked loop (PLL) because the PLL locking transient takes a long time, on the order of micro-seconds. Recently, many frequency synthesizers in an MB-OFDM direct transceiver have been reported in Refs. [3–6]. The possible ways of performing the frequency generation in a UWB system are discussed in Ref. [3]. The synthesizer presented in Ref. [4] uses two PLLs and a single-sideband (SSB) mixer to span the frequencies in band group 1. This architecture has a good compromise between performance and silicon area. This paper describes a fast-hopping 3-band frequency synthesizer based on this architecture in detail for MB-OFDM UWB system in a 0.13 μm CMOS process. Also, the synthesizer specification and architecture are introduced and the measurement results are described.

2. Synthesizer specification and architecture

The proposed frequency synthesizer architecture is given in Fig. 2, which is mainly composed of two PLLs and one QSSB (quadrature SSB) mixer. The frequency plan used here is similar to that proposed in Refs. [4, 5]. The first PLL (PLL1) generates the center frequency of 3960 MHz, and the second PLL (PLL2) realizes the band spacing frequency of 528 MHz. The SSB mixer requires quadrature inputs so as to accomplish frequency addition or subtraction. To generate the required quadrature signals for the SSB mixer, a quadrature voltage-controlled oscillator (QVCO) is adopted in PLL1. The quadrature signal of 528 MHz is generated from the output of the first two stage divide-by-2 circuits in PLL2. The steady quadrature signal of 3960 MHz (which is the carrier frequency of band #2) is applied to one input port of the SSB mixer. When the carrier frequency of band #1 (3432 MHz) needs to be produced, this 3960 MHz tone is shifted down by applying a −528 MHz tone at the other SSB mixer input port. Similarly, to generate the carrier frequency of band #3 at the SSB mixer output, the 3960 MHz tone is shifted up using a +528MHz tone. Finally, to generate the carrier of band #2, the 3960 MHz tone is made available at the SSB-mixer's output node by applying a DC signal at the other input port, yielding a transparent SSB mixer. Note that frequency-hopping is achieved by a frequency multiplexer. This multiplexer produces DC or quadrature output signals with different phase sequences. The quadrature SSB mixer is intended for generating quadrature carrier frequencies. According to Ref. [6], the design specifications for the proposed synthesizer are presented in Table 1.

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† Corresponding author. Email: yumeihuang@fudan.edu.cn
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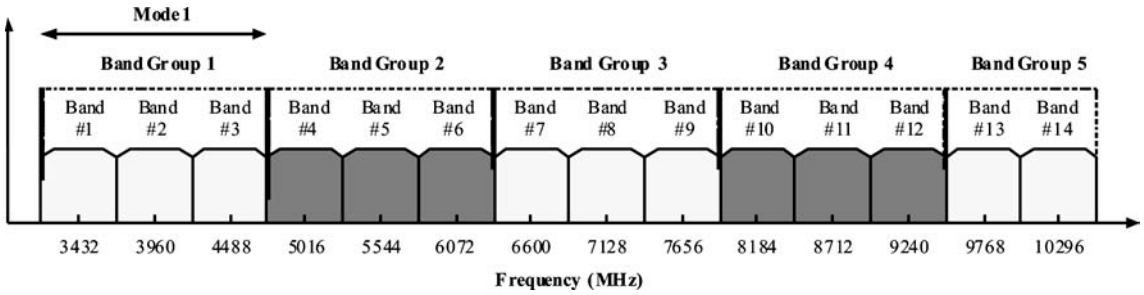

Fig. 1. Frequency plan of MB-OFDM UWB system.

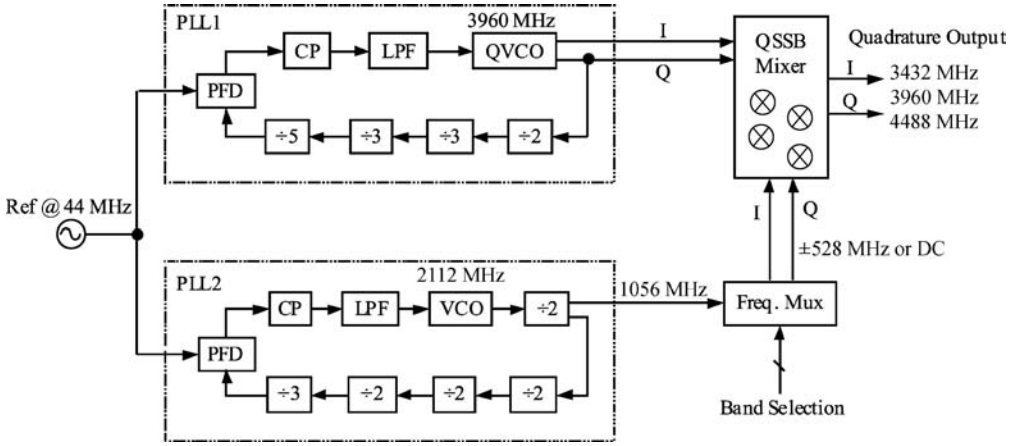

Fig. 2. Proposed frequency synthesizer diagram for MB-OFDM UWB system.

Table 1. Design specifications.

Parameter	Value
LO frequency	3432 MHz, 3960 MHz, 4488 MHz
Switching time	< 9.5 ns
Out-of-band spurious tone	< −45 dBc (2.4 GHz ISM) < −50 dBc (5 GHz ISM)
In-band spurious tone	< −30 dBc
Integrated phase error	3.5°rms

3. Circuit implementation

3.1. Phase-locked loop design

As mentioned previously, two integrated on-chip PLLs are needed to deliver fundamental frequencies at 3960 MHz and 2112 MHz, respectively. A type-II charge-pump-based PLL with total fourth order is adopted for this application. Each PLL consists of phase-frequency detector (PFD), charge pump (CP), third-order loop filter, VCO, and divider chain. Both PLLs use a classical third-order passive loop filter topology as shown in Fig. 3. This topology poses three poles (including one pole at zero) and one zero in the frequency response. The largest pole is added for additional attenuation of unwanted spurs. The open-loop gain of the PLL can be expressed as

$$G(s) = \frac{I_{\mathrm{CP}}K_{\mathrm{VCO}}}{2\pi N}\frac{Z(s)}{s} = \frac{I_{\mathrm{CP}}K_{\mathrm{VCO}}}{2\pi N}\frac{sT_{\mathrm{Z}}+1}{s^2(C_1+C_2+C_3)(sT_{\mathrm{P1}}+1)(sT_{\mathrm{P3}}+1)}, \quad (1)$$

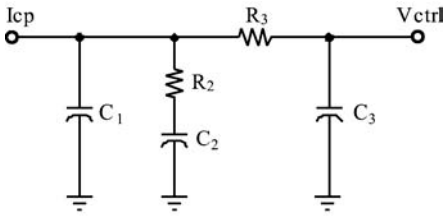

Fig. 3. Third-order passive loop filter.

where K_{VCO} is the VCO gain in unit of rad/V, I_{CP} is the charge pump current, and N is the division ratio. $Z(s)$ is the impedance transfer function of the loop filter. Designing the loop filter involves solving for the time constants, and then determining the loop filter components from these time constants. According to Ref. [7], the time constants can be expressed by the PLL parameters as

$$T_{\mathrm{P1}} = \frac{\sec\phi(\omega_{\mathrm{c}}) - \tan\phi(\omega_{\mathrm{c}})}{\omega_{\mathrm{c}}(1+T_{31})}, \quad (2)$$

$$T_{\mathrm{P3}} = T_{\mathrm{P1}}T_{31}, \quad (3)$$

$$T_{\mathrm{Z}} = \frac{1}{\omega_{\mathrm{c}}^2(T_{\mathrm{P1}}+T_{\mathrm{P3}})}, \quad (4)$$

where ω_{c} is unit-gain open loop bandwidth, $\phi(\omega_{\mathrm{c}})$ is phase margin, and T_{31} is the ratio of the two poles. This pole ratio can range from zero to one. If the open loop bandwidth, phase margin, and pole ratio are specified, the time constants can be calculated accordingly.

The PLL close-in phase noise contribution of each noise source is enlarged by the division ratio N[8]. To reduce N, an achievable external reference of 44 MHz is selected for both PLLs. To minimize the noise coupling between the two PLLs,

Table 2. Summary of the parameters of the two PLLs.

Parameter	Value	
	PLL1	PLL2
PLL reference freq. (MHz)	44	44
Output freq. (MHz)	3960	2112
VCO (QVCO) gain (MHz/V)	475	275
Charge pump current (μA)	200	200
Division ratio	90	48
Open loop bandwidth (kHz)	628	628
Phase margin	55°	55°
Non-zero pole ratio	0.4	0.4
C_1 (pF)	9.77	10.60
C_2 (pF)	206.69	224.37
C_3 (pF)	2.20	2.38
R_2 (kΩ)	3.89	3.58
R_3 (kΩ)	16.50	15.20

their PFDs are triggered at different (positive and negative) reference clock edges. The parameters of the two PLLs including their loop filters in the proposed synthesizer are summarized in Table 2. A high charge pump current of 200 μA and a large non-zero pole ratio of 0.4 are selected for both PLLs for considerations of carrier phase noise performance and unwanted spur suppression. The parameters of the loop filter components are determined based on the principle proposed in Ref. [7]. The VCO (QVCO) input capacitance puts practical limits on the parameters of the loop filter. Typically, this input capacitance is on the order of 100 fF to 1 pF. It is desirable to have the capacitor C_3 next to the VCO to be at least 4 times the VCO input capacitance to keep it from distorting the performance of the loop filter. The main capacitor C_2 always occupies a large chip area. To implement the capacitor C_2 in a more efficient way, the cascaded self-biased capacitor multiplier proposed in Ref. [9] is adopted here.

3.2. VCO (QVCO)

As mentioned previously, two PLLs are used to create the output frequency tones for band group 1. Each PLL needs a VCO circuit. To generate quadrature signals at 3960 MHz, a typical LC quadrature VCO (QVCO) is implemented. The QVCO consists of two cross-coupled LC VCO with four pMOS coupling transistors, which is similar to Ref. [10]. This QVCO has a good compromise between power consumption and phase noise performance. For PLL2, the VCO has been designed to have an oscillation frequency of four times 528 MHz, i.e., 2112 MHz to minimize the inductance and the chip area without sacrificing its quality factor. The implemented LC VCO schematic using complementary nMOS and pMOS cross-coupled pairs is shown Fig. 4. Non-minimum gate lengths were used for nMOS (M3, M4) and pMOS (M1, M2) to improve the phase noise by reducing transistor flicker noise, exploiting waveform symmetry and maximizing output swing. The current of the VCO is provided by a current bias of 200 μA and a pMOS current mirror. The length and width

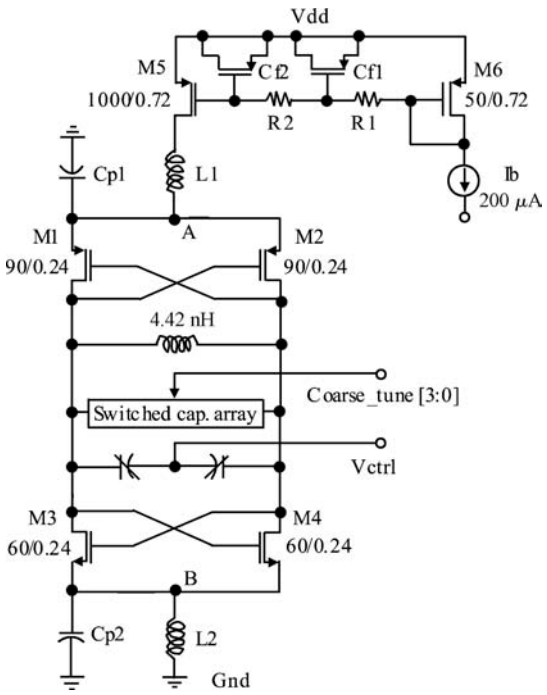

Fig. 4. 2112 MHz VCO schematic.

of M5 and M6 are made large to reduce flicker noise, and thus close-in phase noise.

To realize low phase noise, a dual noise filtering circuit composed of L1 and Cp1, L2 and Cp2 is added. Each LC tank resonates at the second harmonic of the oscillation frequency[11], thus raising the impedance. Cp1 and Cp2 are the parasitic capacitors at the common source (virtual ground) of the differential pair, i.e., node A and node B, respectively. The L1 and L2 are symmetrical series stacked inductors made of metal M5–M8 in the 8 metal-layer process to minimize their areas. Simulation shows that this LC filtering technique improves the carrier phase noise effectively by 5–10 dB. In Fig. 4, a two-stage RC low-pass filter composed of R1, Cf1 and R2, Cf2 is inserted between M5 and M6 to remove the flicker and thermal noise generated by the current bias circuit[12]. The capacitor Cf1 and Cf2 are made of common pMOS transistors with each source, drain and bulk tied together to realize a large value with a small layout area.

For both of the above VCOs, the inductors are all implemented by using on-chip differential spirals. The varactor is a MOS type made of gate and n-diffusion in an n-well, which is provided by the technology in use. To compensate for the parasitic capacitance and the possibility of the inductor modeling inaccuracy, the 4-bit switched capacitor arrays are added for each VCO tank. This digital tuning scheme divides a wide tuning range into 16 smaller bands and the VCO gain is decreased accordingly. The variable capacitance of the varactor is slightly larger than the unit capacitance of the switched capacitor array in order to cover the frequency band including the desired frequency without gap.

3.3. QSSB mixer

To provide quadrature (I/Q) signals for the transceiver's LO, a quadrature SSB (QSSB) mixer is proposed in the syn-

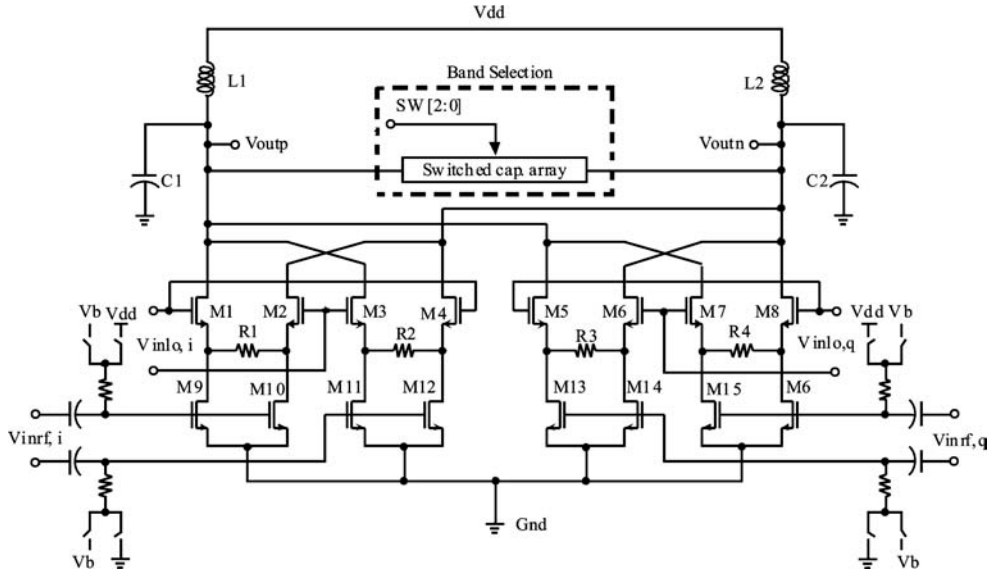

Fig. 5. SSB mixer (the AC coupling network of the LO port is omitted for clarity).

thesizer. The QSSB mixer consists of a pair of SSB mixers. The operation of the SSB mixer can be demonstrated by the following equations:

$$A\sin(\omega_1 t)B\cos(\omega_2 t) + A\cos(\omega_1 t)B\sin(\omega_2 t) = AB\sin(\omega_1+\omega_2)t, \tag{5}$$

$$A\sin(\omega_1 t)B\cos(-\omega_2 t) + A\cos(\omega_1 t)B\sin(-\omega_2 t) = AB\sin(\omega_1-\omega_2)t, \tag{6}$$

where A and B represent the input amplitudes. Equation (6) is obtained by inverting the phase $\omega_2 t$ of Eq. (5). The UWB system requires quadrature signals from the output of the synthesizer. By adding (or subtracting) $\pi/2$ to phase $\omega_1 t$, the quadrature outputs are generated, respectively, as

$$A\sin(\omega_1 t+\pi/2)B\cos(\omega_2 t) + A\cos(\omega_1 t+\pi/2)B\sin(\omega_2 t) = AB\cos(\omega_1+\omega_2)t, \tag{7}$$

$$A\sin(\omega_1 t+\pi/2)B\cos(-\omega_2 t) + A\cos(\omega_1 t+\pi/2)B\sin(-\omega_2 t) = AB\cos(\omega_1-\omega_2)t. \tag{8}$$

The SSB mixer used in the frequency synthesizer consists of two Gilbert multiplier-based mixer cores whose outputs are added together as currents. Figure 5 shows the proposed SSB mixer. The 3960 MHz signal is fed into the LO input ports and the 528 MHz signal is fed into the RF input ports. Spurs appear at the output of the SSB mixers in two different ways[5]. First, the image sideband spur of an SSB mixer is heavily influenced by mismatches between the I and Q mixers. In addition to mismatches, nonlinearities in the SSB mixer itself also introduce sideband spurs, which span over the whole spectrum due to cross-products of the input harmonics. The architecture introduced in Fig. 5 incorporates LC band-pass loads and source degeneration techniques to suppress sidebands. Band selection is accomplished by adjusting capacitor arrays to change the resonance frequency of the LC tank. The center frequency of the resonator is adjusted simultaneously with the band switching

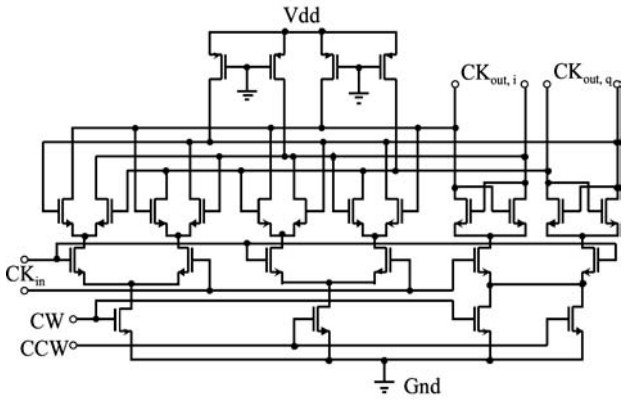

Fig. 6. Frequency multiplexer schematic.

of the frequency synthesizer. Due to the narrowband characteristic of the LC tank, good sideband suppression can be achieved. A source degeneration technique is employed in the LO port to improve the linearity. Here, R1–R4 linearize the LO port switches M1–M8 with no voltage headroom consumption. In order to avoid extra voltage headroom consumption under low voltage supply, both the source degeneration technique in the RF port and the tail current source are removed.

To bias the common-mode voltage of the RF and LO ports to fixed voltage levels, the AC coupling networks that consist of capacitors and resistors are inserted before the input RF and LO ports of the SSB mixer. In this way, the linearity of the QSSB mixers is ensured and the unwanted spurs are minimized. DC mixing is realized by switching half of the RF transistors to ground and half to the supply voltage (V_{dd}). In addition, the incoming signals to RF terminals are disabled by the previous MUX stage simultaneously. In this case, the QSSB mixer only works as a buffer with cascade transistors.

3.4. Frequency multiplexer

The frequency multiplexer is shown in Fig. 6, which is a modified version of the tri-mode divider proposed in Ref. [5]. It is a combination of two conventional CML divide-by-

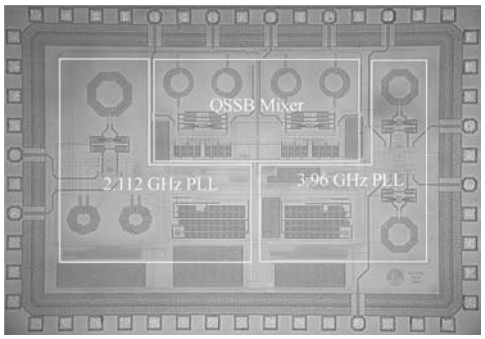

Fig. 7. Die photograph.

2 circuits that share a common load. So another function of this frequency multiplexer is to divide the input frequency (1056 MHz) by 2 and generate the quadrature frequency (±528 MHz) for the SSB mixer. This leads to two opposite phase sequences, i.e., +528 MHz or −528 MHz according to the control signal 'CW' and 'CCW'. When both control signals are low, the dividing function of this frequency multiplexer is disabled and there is no frequency output at all. The crossed-coupled pairs are also turned off while the circuit is producing DC signals. In this way the DC signal is generated and fed into the SSB mixer to generate a transparent 3960 MHz (band #2) carrier. Note that the control signal 'CW' and 'CCW' cannot be simultaneously high.

Polysilicon resistors are sometimes used as loads for the CML divider due to their lower parasitic capacitance. However, on-chip resistors are not as well controlled in CMOS processes. In this work, pMOS transistors are used as loads. The gates of the pMOS transistors are connected to ground. The current sources in conventional CML latches are omitted for low-voltage operation.

4. Experimental results

This fully integrated frequency synthesizer has been fabricated in a 0.13 μm CMOS technology with 8 metal layers. The die photograph is shown in Fig. 7. The core area is 1.0×1.8 mm^2, which is mainly occupied by LC resonators in the proposed architecture. The synthesizer draws 27 mA current from a single 1.2 V supply. Each building block is encircled by double guard rings to minimize the noise coupling. The layout is carefully optimized to provide good matching and to minimize the undesired coupling between digital and analog/RF parts.

The chip is directly bonded onto a 4-layer FR-4 PCB for measurement, as shown in Fig. 8. The performance of the proposed synthesizer was measured by Agilent E4440A spectrum analyzer. Figure 9 shows the measured output spectrum when generating band #1, i.e., 3432 MHz. The in-band spurious tone at 3960 MHz, caused by leakage through the SSB-mixer, is below −30 dBc. The spurious tone at 4488 MHz, caused by I/Q mismatch is also well below the required −30 dBc. The out-of-band spurious tones are also sufficiently attenuated. The tones falling in the 5 GHz WLAN band are well below the −50 dBc. The same holds for spurious tones in the 2.4 GHz ISM

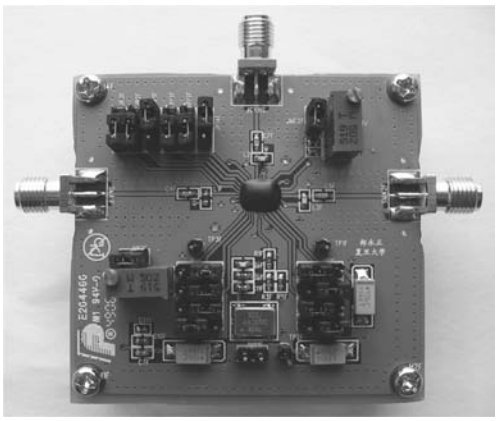

Fig. 8. Test PCB.

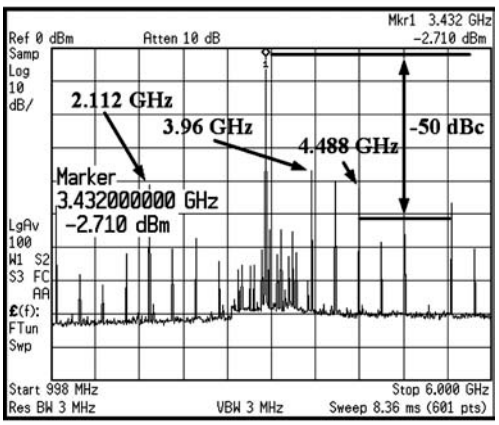

Fig. 9. Measured output spectrum of the synthesizer for 3432 MHz (band #1).

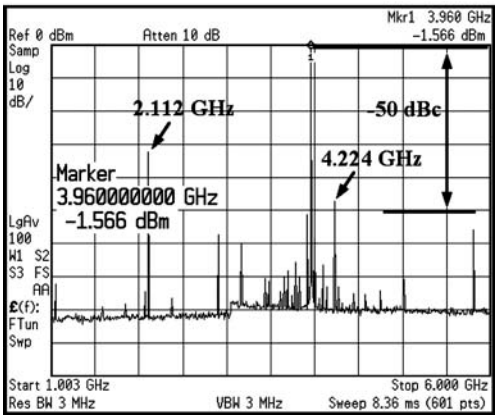

Fig. 10. Measured output spectrum of the synthesizer for 3960 MHz (band #2).

band. Figure 10 shows the measured output spectrum when generating band #2, i.e., 3960 MHz. Because this signal stems directly from the QVCO output, most spurious tones in the output spectrum are relatively low. Figure 11 shows the spectrum for band #3, i.e., 4488 MHz, again showing the specifications are met. Figure 12 shows the measured phase noise of the 4488 MHz carrier. The spot phase noise is −110.2 dBc/Hz at 1 MHz frequency offset. The integrated RMS phase error from 1 kHz to 10 MHz is below 3.5°, which meets the specification.

The band-switching behavior was measured by a Tektronix TDS 6604 Digital Storage Oscilloscope. Figure 13

Table 3. Performance summary and comparison.

Reference	Leenaerts[4]	Lee[5]	Zheng[8]	This work
Frequency (MHz)	3432–4488	3432–7920	6336–10560 2904 (IQ)	3432–4488
No. of bands	3	7	9	3
In-band spurs (dBc)	⩽–35	⩽ –37	−38.6 @ 6336 MHz	⩽ –34
Out-of-band spurs (dBc)	⩽ –45	⩽ –48	N.A.	⩽ –50
Phase noise (dBc/Hz) (@1-MHz offset)	< –103	−103	< –124 @ 10 MHz	−110
Switching time (ns)	< 1	1	< 1	< 2
Power consumption	27.2 mA	48 mW	59 mA	27 mA
Power supply (V)	2.7	2.2	1.5	1.2
Technology	0.25 μm SiGe BiCMOS	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS

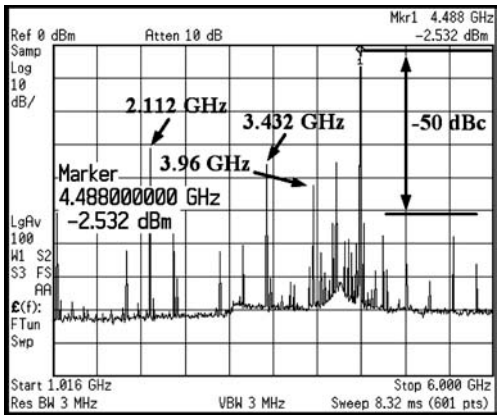

Fig. 11. Measured output spectrum of the synthesizer for 4488 MHz (band #3).

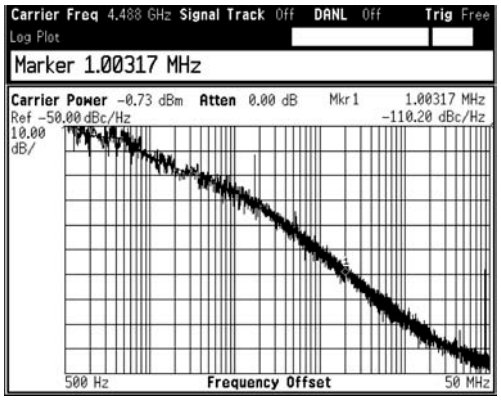

Fig. 12. Measured phase noise when generating 4488 MHz (band #3).

shows the measured result, where the bands were switched periodically and the synthesizer output was monitored. The settling time while hopping from band #1 to band #2 is within 2 ns, a value much less than the required 9.5 ns. The LO has the measured single-ended voltage swing larger than 400 mVp–p. Table 3 summarizes the measured performance of the proposed frequency synthesizer and presents a performance comparison with some other UWB synthesizers recently published in the literature. As the results in Table 3 demonstrate, the proposed synthesizer satisfies the MB-OFDM in-band and out-of-band spur suppression requirements with no more DC current consumption

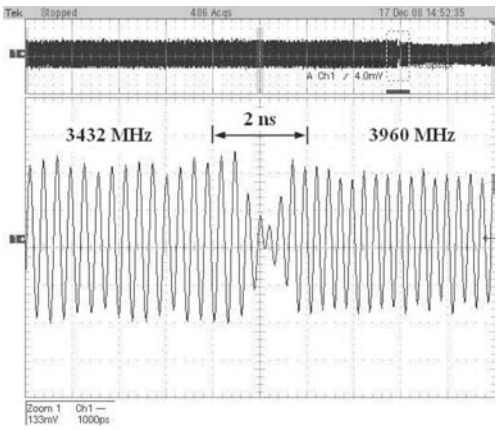

Fig. 13. Measured output waveform while hopping from band #1 to band #2.

than other previous works. With the lowest power supply and the use of few nonlinear components, the proposed synthesizer provides a low-voltage and low-power design which generates fewer spurs for MB-OFDM UWB transceivers.

5. Conclusion

A fast hopping 3-band frequency synthesizer in a 0.13 μm CMOS process has been presented. This synthesizer uses two PLLs for generating frequencies of 3960 MHz and 528 MHz, respectively. It provides quadrature (I/Q) signals for the 3-band carriers through a QSSB mixer. Measurement shows that this chip meets the performance requirements for mode-1 MB-OFDM UWB system. It consumes 27 mA current from a single 1.2 V supply.

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