# Wafer level hermetic packaging based on Cu–Sn isothermal solidification technology*

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**Abstract:** A novel wafer level bonding method based on Cu–Sn isothermal solidification technology is established. A multi-layer sealing ring and the bonding processing are designed, and the amount of solder and the bonding parameters are optimized based on both theoretical and experimental results. Verification shows that oxidation of the solder layer, voids and the scalloped-edge appearance of the $Cu_6Sn_5$ phase are successfully avoided. An average shear strength of 19.5 MPa and an excellent leak rate of around $1.9 \times 10^{-9}$ atm cc/s are possible, meeting the demands of MIL-STD-883E.

**Key words:** wafer level package; Cu–Sn isothermal solidification technology; hermeticity
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## 1. Introduction

In recent years wafer level chip scale packaging technology (WL-CSP) has been widely used for its advantages of small size and low cost. A reliable wafer level bonding technique is key to accomplishing a successful WL-CSP packaging structure. Wafer level bonding techniques can be roughly divided into three categories[1]: (1) anodic bonding, (2) silicon fusion bonding, and (3) intermediate film bonding, while the intermediate film bonding technique can be further divided according to the films used as bonding media. Such films can either be low temperature sealing materials such as organic materials (BCB, etc.) and solder, or high temperature sealing materials such as glass frit and metal. Anodic fusion bonding can be done directly by attaching silicon to sodium-rich glass, or silicon fusion bonding by attaching silicon to silicon; however, their usage is limited because of the requirements of a higher temperature during the bonding process and a rigorously clean flat surface. By contrast, intermediate film bonding can be carried out at a lower temperature, eliminating the requirement of flatness of the bonding surface. However, some disadvantages such as bad thermal stability and hermeticity of the cured BCB film, and a wide bonding area for the glass frit limit their applications.

In this paper, we propose a wafer level hermetic bonding technique based on Cu–Sn isothermal solidification. It is such a process that employs a low melting point metal interlayer as solder between the base metals to be jointed and relies on interdiffusion for isothermal solidification at the bonding temperature[2]. The integrity of the bonding is enhanced by the liquid phase during bonding. Currently a great deal of literature about Cu–Sn bonding has been reported, but some are just based on bulk materials with process methods diverging from flip-chip assembly[3], and some utilize thick Sn layers as solder[4]. Using a thick Sn layer as solder has two main disadvantages: on one hand, the remaining Sn layer after bonding will re-melt during the operation once the temperature surpasses the melting point of Sn (232 °C), which restricts further processes and applications. On the other hand, using a thick Sn layer will increase the packaging cost. To overcome such disadvantages, we propose a method utilizing a thin film of Sn with merely a thickness of 6 $\mu$m. After the bonding process, Sn is completely depleted, leaving only Cu and Cu–Sn intermetallic compound (IMC) layers, so that the bonds are able to withstand further operations at temperatures above the melting point of Sn.

## 2. Experiment

In the experiment, the pattern of the sealing ring and its constitutional materials were designed, optimized and fabricated. The quality of the hermetic packaging structure was finally verified.

### 2.1. Design

In the experiment, a 4 inch, 450 $\mu$m thick N (100) silicon wafer is used. The sealing pattern is a $1.5 \times 1.5$ mm$^2$ closed square loop with a width of 0.2 mm, as shown in Fig. 1. For the bonding structure, including substrate wafer and cap wafer, different multiple layers of metallization are deposited on the wafers by sputtering and electroplating. Details of the fabrication process will be mentioned in the following sections. Cu and Sn are chosen as the base metal and solder for the sealing ring due to their widespread use in electronic products, especially with Sn having a lower melting point and relative high solubility in Cu. Cu/Sn isothermal solidification is utilized for

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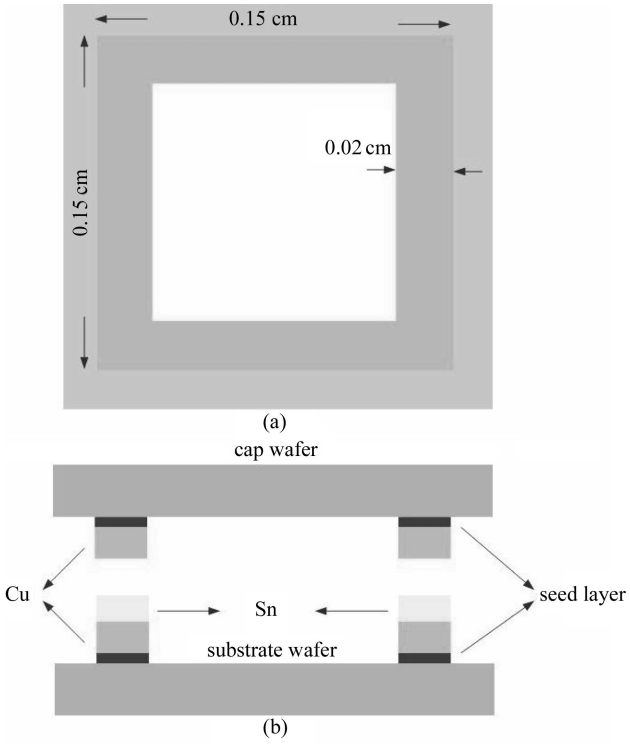


Fig. 1. (a) Top view of the cap wafer; (b) Schematic structure of the bonding structure (drawing not to scale).

the bonding. The thickness of the Cu and Sn layers as well as the parameters of the bonding process is to be optimized from both theoretical calculation and experimental examination.

### 2.2. Fabrication process

#### 2.2.1. Dummy device wafer fabrication

50 nm TiW / 150 nm Cu is firstly sputtered on the cap wafer as seed layer. 13–14 $\mu$m thick photoresist is spin coated and patterned. The parameters of the photoresist, Shipley AZ4620, such as spin speed, spin time, soft bake time, cure time and exposure time corresponding to the thickness can be found on the website of Microchemicals GmbH[5]. In the following step, 6 $\mu$m Cu and 4 $\mu$m Sn are separately electroplated as the base layer and the solder layer. Such thickness is optimized both theoretically and experimentally and will be discussed in the following section. Finally the photoresist is removed and the thin seed layer can be directly etched away by ion beam etching.

#### 2.2.2. Cap wafer fabrication

The fabrication process of the cap wafer is the same as the dummy device wafer except that no Sn layer is electroplated. The reason for this has already been reported in our previous work[6].

#### 2.2.3. Bonding procedure

Prior to bonding, the surface treatment process is an important step for good bonding quality[7]. Because Sn is easily oxidized in open air even at room temperature and both wafers have gone through a photolithographic process after which a small amount of photoresist probably remains at the surface, Ar plasma cleaning is applied to remove the natural oxide and other contaminations on the surface. The power of the plasma is controlled to be 500 W and the cleaning time is set as 170 s to avoid melting the Sn layer.

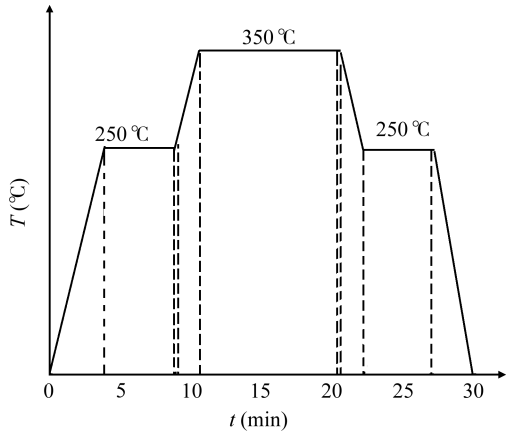


Fig. 2. Temperature–time profile for Cu/Sn bonding in experiment.

After the surface treatment, the wafers are firstly prealigned using KarlSuss MA6 which provides a critical resolution of $\pm 1$ $\mu$m. Then, the aligned wafers are brought to the SB6 bonding system to complete the bonding process. Static pressure of 200 mbar is applied on the wafers throughout the whole bonding process with its main utility to break the hump of liquid Sn formed by conglomeration at the melting point to achieve a good wetting condition. The temperature-time profile designed is as shown in Fig. 2 and the vacuum of the chamber is kept around $5 \times 10^{-4}$ mbar during the whole process. Parameter optimization for the temperature-time profile will be discussed in the following sections in detail. In the last step of the bonding process, $N_2$ is filled up to cool the chamber. The temperature drop rate should be as fast as possible because the grain size at low temperature is always smaller than that at higher temperatures.

## 3. Optimization of the bonding structure and the bonding process parameters

### 3.1. Optimization of the thickness of the metal layer

#### 3.1.1. Optimization of the thickness of the Sn layer

Since the bonding process is fluxless, control of the Sn layer thickness becomes very important. On one hand, too thick a layer will cause molten Sn overflow from the edge of bonding interfaces during the bonding process. Sometimes such an overflow is too disastrous and causes a short circuit. On the other hand, if the Sn layer is too thin it will lead to poor wetting during the bonding process which affects the bonding quality. So the thickness of Sn should be optimized. According to the theory of Bosco *et al.*[8], the critical thickness of the Sn layer can be theoretically estimated. In our experiment, the situation is a little different for only the dummy device wafer includes a Sn solder layer. So a new model is established as shown in Fig. 3 and the critical thickness of the Sn

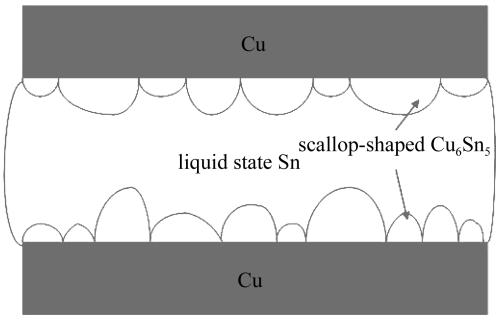


Fig. 3. Schematic drawing of the morphology of the Cu–Sn reactive layer with the Sn layer in the melting state. The maximum $\eta$-grain height determines the critical thickness of the Sn layer (drawing not to scale).

layer needed in our experiment should be:

$$h_c^* = \Omega h_\eta C_\eta \left(\frac{\rho_\eta}{\rho_{Sn}}\right), \tag{1}$$

where $h_c^*$ is the critical thickness of Sn, $\Omega$ is an non-dimensional parameter characterizing the non-uniform morphology of the $\eta$-phase, $h_\eta$ is the average thickness of the scallop-shaped $\eta$-phase (the $Cu_6Sn_5$ phase) when the melting point temperature of Sn is reached , $C_\eta$ is the mass fraction of Sn in the $\eta$-phase, and $\rho_\eta$, $\rho_{Sn}$ are the mass densities of the $\eta$-phase and Sn respectively.

$$\Omega = 1 + \frac{H_\eta - h_\eta}{h_c}, \tag{2}$$

where $H_\eta$ is the largest height of the scallop-shaped $\eta$-phase layer when the melting point of Sn is reached, and $h_c$ is the critical thickness of Sn layer needed assuming the $\eta$-phase layer grows in a planar manner which can be expressed as

$$h_c = h_\eta C_\eta \left(\frac{\rho_\eta}{\rho_{Sn}}\right). \tag{3}$$

The average thickness of the scallop-shaped $\eta$-phase is ascertained from experimental results showing a form of power law relationship with heating time[9]:

$$h_\eta = k t_h n, \tag{4}$$

where $t_h$ is the heating time, and $k$ and $n$ are constants characterizing the relationship between $h_\eta$ and $t_h$.

Combining Eqs. (1) and (4) yields:

$$h_c^* = \Omega k t_h^n C_\eta \left(\frac{\rho_\eta}{\rho_{Sn}}\right). \tag{5}$$

The value of $\Omega$ is 3.2 ± 0.4[8] (here the value is directly used because it is time-independent), and $k$ and $n$ is set to be 3.7 $\mu$m/min$^{0.3}$ and 0.3 from the previous work[9]. Finally the critical thickness can be calculated as 2.6 ± 0.3 $\mu$m; considering the roughness of the Cu layer surface, the layer thickness is taken to be 50% greater than the calculated value: $1.5h_c^*$ = 3.9 ± 0.4 $\mu$m. Such a theoretical result will be further examined by experiments.

### 3.1.2. Optimization of the thickness of the Cu layer

As for the Cu layer, firstly it should be thick enough to ensure that the remaining Cu is left after the bonding process because once the copper layer is consumed the IMC layer will be in direct contact with the underlying non-solderable layer and a poor adhesion between the IMC and the non-solderable layer will occur.

Assuming that only the $\varepsilon$-phase (the $Cu_3Sn$ phase) forms during the bonding process, the thickness of the Cu layer should be:

$$h_{Cu} = \frac{3h_{Sn}M_{Cu}}{M_{Sn}}, \tag{6}$$

where $h_{Cu}$, $h_{Sn}$ are the total thicknesses of the Cu and Sn layers, and $M_{Cu}$, $M_{Sn}$ are the molar volumes of Cu and Sn, respectively. $h_{Sn}$ is determined to be 4 $\mu$m by the discussion above, and $M_{Cu}$, $M_{Sn}$ are given by the related literature[10]. Finally $h_{Cu}$ is calculated to be about 8.3 $\mu$m, indicating that a Cu layer of at least 4 $\mu$m should be electroplated on each wafer (supposing the Cu consumption rate is equal at both sides for simplification).

Additionally, the remaining Cu layer can also be used as a spacer to alter the space for the device inside. In view of all the above-mentioned points and considering that the amount of Cu consumed on each wafer is actually not equal, it is determined that a 6 $\mu$m thick Cu layer should be deposited on both wafers.

### 3.1.3. Experimental examination

Figures. 4 and 5 show cross-sectional views of bonding with different Sn layer thicknesses after the same bonding process. Figure. 4 is the bonding structure with 2 $\mu$m thick Sn and Figure. 5 is the bonding structure with 4 $\mu$m thick Sn. Considerable amounts of void-like defects can be seen in Fig. 4, indicating that the Cu layer surface had not been well wetted by the liquid Sn during the bonding. The reason for this is thought to be the rough and not flat surface of the electroplated Cu layer which could not be well wetted by the insufficient amount of molten Sn. In contrast, no voids can be seen in Fig. 5. This proves that the theoretically calculated thickness 4 $\mu$m is a moderate value.

### 3.2. Optimization of the bonding parameters

Figure. 6 shows the phase diagram for the Cu–Sn system. It can be seen that as long as the reactive temperature exceeds 415 °C there will be no $\eta$-phase in IMC. That is why in some literature, the peak temperature of bonding process is set to be 600 °C[11]. But such a high temperature is not compatible with most MEMS device processes. In this work, the peak temperature is set as 350 °C because the peak in the solubility curve of Cu in Sn appears at this point[6]. Besides, this temperature is compatible with most MEMS processes. The temperature-time profile for Cu/Sn TLP bonding is shown in Fig. 2. The rate of temperature rise from RT to the Sn melting point (232 °C) should be rapid enough to avoid large-size $\eta$-grain growth which will cause void formation. A dwelling

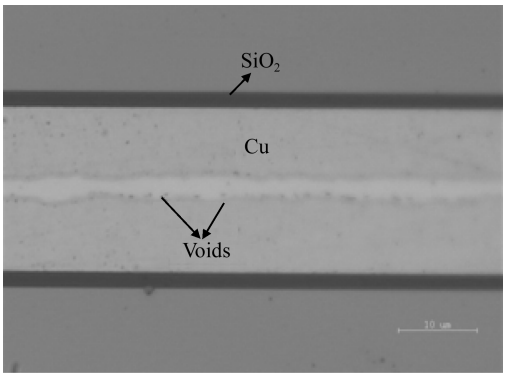


Fig. 4. Cross-sectioned view of the Cu/Sn interlayer after bonding with obvious voids can be seen (2 $\mu$m Sn; the light gray colored layer is examined by EDS analysis to be $Cu_6Sn_5$, and the dark gray colored layer is too thin to be examined but inferred to be $Cu_3Sn$ according to theory).

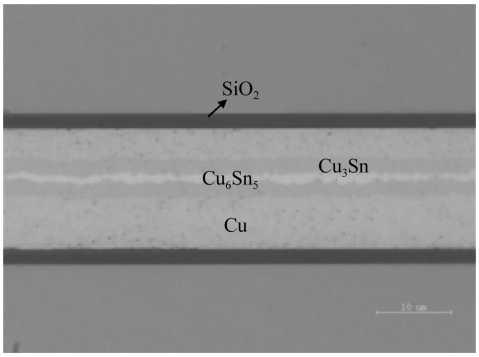


Fig. 5. Cross-sectional view of the Cu/Sn interlayer after bonding (4 $\mu$m Sn).

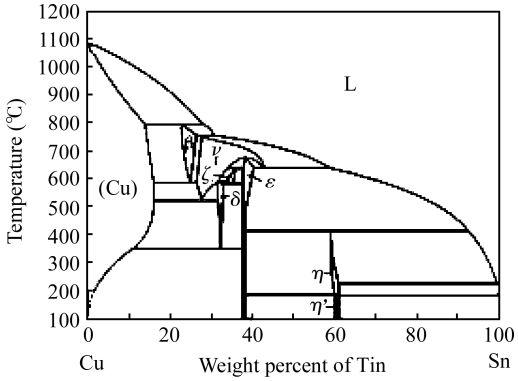


Fig. 6. Phase diagram for the Cu/Sn system.

time of 10 min is decided on for sufficient interdiffusion and reaction. In our experiment, the optimized thickness of the Sn layer is 4 $\mu$m. The diffusion coefficient D of Cu in liquid state Sn is as high as $10^{-5}$ $cm^2/s$ according to some literature[9]. From the simple parabolic relationship between diffusion distance and time ($x \sim \sqrt{Dt}$)[12], reaction time can be roughly estimated to be on the order of seconds. However, we set it to 10 min to encourage the $\eta$-phase to grow in a planar manner[13].

## 4. Results and discussion

### 4.1. Composition of the bonding interlayer

Figure 5 shows a cross-sectional view of the Cu/Sn interlayers after the bonding process. It can be seen that Sn is totally consumed while remaining Cu is left on both sides. The IMC formed after bonding is composed of two components: a light gray colored layer and a dark gray colored layer. EDS analysis shows that the light gray colored layer is $Cu_6Sn_5$ and the darker gray colored layer is $Cu_3Sn$. The morphology of the $Cu_6Sn_5$ phase is not scallop-shaped but flat because during the isothermal aging process the scallops of $Cu_6Sn_5$ were flattened as a layer. The $Cu_3Sn$ phase grows a lot and its thickness becomes comparable to that of $Cu_6Sn_5$. It can be seen that the surface of the electroplated Cu layer is rough and not flat, but there is no obvious void formed at the interface between the Cu and IMC layers, indicating good wetting during the bonding. The future plan is to achieve having only the $Cu_3Sn$ phase left after bonding by increasing the dwelling time and heating rate. Pure $Cu_3Sn$ IMC is considered to be beneficial to the reliability because $Cu_6Sn_5$ is an unstable Sn-rich source phase and the formation of the $Cu_3Sn$ phase during solid state aging is accompanied by Kirkendall void formation, which tends to cause reliability problems[13]. An infrared microscope picture is also shown in Fig. 7 to prove that no melting Sn overflow occurred during the bonding process.

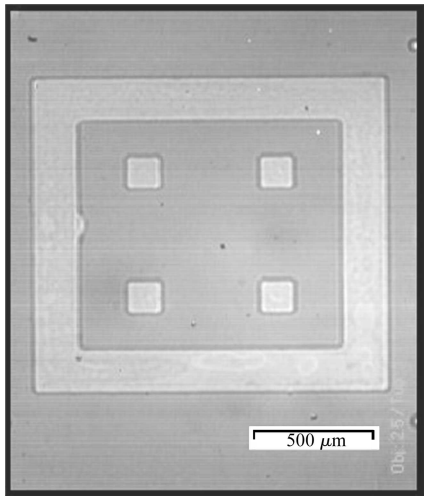


Fig. 7. Infrared microscope picture of the bonding structure (the four squares inside the sealing ring are bonding points).

### 4.2. Shear strength test

The shear strength of the samples was measured using a Dage series 4000B Bondtester. As a reference, in MIL-STD-883E, a shear strength of 6 MPa is needed. Measurement results of 20 samples show that the maximum shear strength is 25.3 MPa, the minimum is 13.4 MPa, and the average is 19.5 MPa. The result demonstrates that the shear strength of the samples satisfies the MIL-STD-883E requirements.

### 4.3. Hermeticity test

#### 4.3.1. Fine-leak test

Fine-leak tests as well as gross-leak tests have been done on the samples in order to characterize the hermeticity of the bonded wafers.

The cavity volume of the bonded sample is less than 0.001 $cm^3$ and, according to MIL-STD-883E, the leakage limit is $5 \times 10^{-8}$ atm cc/sec. In our test, the samples are first placed in a chamber, pressurized with helium soaked for 3 h at 5 bar, and transferred to the helium leak detector to be monitored. The reject limit is $1.9 \times 10^{-9}$ atm cc/s which is well below the leakage limit.

#### 4.3.2. Gross leak test

The gross leaks are tested using fluorocarbon and are based on the "bubble method". The samples are placed under fluorocarbon liquid FC-84 in a vacuum chamber full of $N_2$ with a pressure of 5 bar for 5 h. The samples are removed from the bath, dried in air and immersed in fluorocarbon FC-40 which is maintained at 125 °C. If a gross leak is present, any trapped helium will have ample time to escape from the cavity to be inspected. In our test, all 20 samples pass the gross-leak test successfully.

## 5. Conclusions

In this paper, wafer level hermetic bonding based on the Cu–Sn isothermal solidification technique is realized. The pattern of the sealing ring, the constitutional multi-intermediate layer bonding structure, the amount of solder used and the bonding procedure parameters are designed and optimized. Oxidation of the solder layer and scallop-shaped $Cu_6Sn_5$ phase appearance are successfully avoided. High shear strength and excellent hermeticity are achieved, both reaching the demands of MIL-STD-883E.

In further work, a MEMS resonator will be encapsulated in such a bonding structure. *Q*-factor extraction techniques will be utilized to monitor the long term stability of vacuum of the sealed chamber.

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