Effect of annealing on characteristics of a HfO_xN_y–HfO_2–HfO_xN_y sandwich stack compared with HfO_2 film*

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Abstract: HfO_xN_y–HfO_2–HfO_xN_y sandwich-stack (SS) film was investigated in comparison with HfO_2 film of the same thickness. Higher thermal stability and better surface morphology can be observed for the SS film. This structure also shows stronger immunity to interfacial oxidation compared with HfO_2 film. Meanwhile, unlike the HfO_xN_y dielectric, the capacitance performance of SS film was not worse (but was even better) than a pure HfO_2 film of the same thickness. The SS structure appears to be a promising high-*k* gate dielectric compared with both pure HfO_xN_y and HfO_2 dielectrics for future ULSI devices. Additionally, PDA treatment plays an important role in improving the characteristics of SS film, which is confirmed by effective channel electron mobility and stress induced leakage current (SILC) investigations.

Key words: hafnium oxynitride; dielectrics; diffusion; electrical properties; permittivity
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1. Introduction

In order to overcome the limitations of SiO_2 in advanced semiconductor technologies, such as excessive leakage current and reliability concerns[1], high-*k* materials have received more attention than ever[2–4]. Among them, HfO_2 has been highlighted, and seems to be the most promising high-*k* dielectric due to its moderate *k* value (~25) and large band gap (5.7 eV)[5]. Although HfO_2 has been given much attention, some critical issues still exist. One of the most important problems is the diffusion of oxygen though bulk film[6] which leads to the formation of an unnecessary interface layer. The formed interface layer greatly reduces the integrated *k* value of high-*k* films. At the same time, due to the great interface state density for the thick interfacial layer, the hysteresis phenomenon is also easily observed in capacitance–voltage (*C*–*V*) curves of these high-*k* gate dielectrics[7–9]. This hysteresis can cause a flatband voltage shift, resulting in threshold voltage instability. To resolve these problems, N incorporation is a effective method including passivating the surface of Si via NH_3[10, 11], using special electrodes such as TaN or incorporating N into the HfO_2 films[12]. However, passivation of the top electrode or the bottom substrate is at the cost of the sensitivity of the holistic MOS structure and reduces the electrical performance. When it comes to the entire incorporation of N into HfO_2 with the result of HfO_xN_y-bulk film formation, which is successful in increasing thermal stability and preventing oxygen diffusion at the interface[13], the serious lowering of the *k* value compared to that of pure HfO_2 is still unacceptable. On the other hand, due to the extensive presence of incorporated N, the special conductive HfN component is easily formed[13, 14], which when embedded in films leads to a large leakage and the lowering of the breakdown voltage. In order to not only solve these problems but also retain the merits of N incorporation, we have previously reported a HfO_xN_y-HfO_2-HfO_xN_y sandwich-stack (SS) structure using HfO_xN_y layers enwrapping HfO_2 bulk film. This is an effective way to confine the oxygen diffusion and to passivate the interfaces[15], and exhibits excellent electrical properties such as lower leakage current density and higher breakdown voltage compared with that of a pure HfO_xN_y film[15]. However, its characteristics in comparison to a pure HfO_2 film were not considered further. Here, the characteristics of SS film compared with HfO_2 film of the same thickness are evaluated, especially during thermal treatment, since a high-temperature process is required in SLSI device fabrication.

In this paper, HfO_xN_y layers are fabricated as barriers in top electrode/HfO_2 and HfO_2/Si interfaces with the formation of a sandwich-stack (SS) structure. A schematic diagram of the MOS device made by SS film is shown in Fig. 1, which has been illuminated in Ref. [15]. It is confirmed that SS film retains the merits of the HfO_xN_y dielectric, such as increasing crystalline temperature, blocking oxygen diffusion, and passivating interface defects. Meanwhile, it also possesses better

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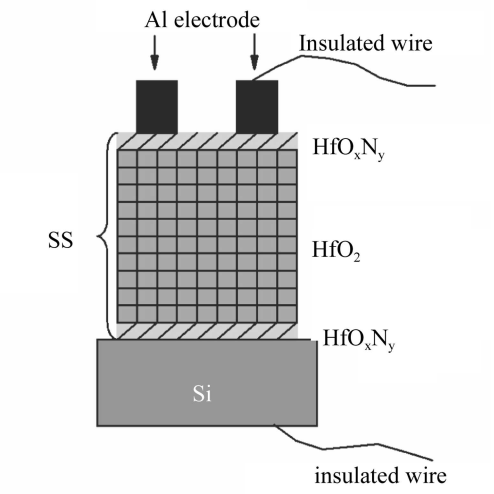

Fig. 1. Schematic diagram of the MOS capacitor made by SS film.

capacitance properties, such as lower hysteresis voltage and frequency dispersion compared with a pure HfO_2 film, which solves the shortcomings of the HfO_xN_y dielectric. Additionally, high-temperature treatment can greatly enhance the advantages of SS film. This is because high temperature annealing can induce a better interface between HfO_2 with HfO_xN_y layers, which is confirmed by mobility and leakage measurements.

2. Experimental details

The fabrication method is described elsewhere[15]. The electrical properties were studied using basic metal-oxide semiconductor (MOS) capacitor electrical characterization. Capacitance–voltage (*C*–*V*) measurements were performed on a HP4284A LCR meter. Current–voltage (*I*–*V*) characteristics were measured using a HP4155B semiconductor parameter analyzer. The film thickness was measured by an ellipsometer.

3. Results and discussion

As mentioned above, N incorporation can improve the thermal stability of HfO_2 films. Figure 2 shows AFM micrographs of two kinds of samples (HfO_2 and SS) indicating surface morphology before and after 900 °C PDA for 60 s in N_2 ambient. The RMS values are 1.6, 2.0, 2.8, 3.4 nm in Figs. 1(a)–1(d), respectively. After annealing at 900 °C, the HfO_2 sample shows a significant change in surface morphology and an increase in RMS roughness. However, in the SS sample, the change is smaller either in surface morphology or in surface roughness. This structural change during annealing was also verified by XRD analysis (data not shown here) that the HfO_2 sample has heavily crystallized after 900 °C anneal. From Fig. 2, we can see that the SS sample increases the thermal stability and keeps the stability of the morphology, though the barrier layers of HfO_xN_y in the SS sample are much thinner than the enwrapped HfO_2 bulk. Meanwhile, the decrease in surface roughness of SS could be due to not only the increase in crystallization temperature but also the reduced oxygen diffusion, since the reactive oxygen movement could induce poor surface features[16]. This assumption is confirmed by FIIR measurements of the comparative HfO_2 and SS samples as shown in Fig. 3. The Si–O peak is shown as a dashed line. From the change in this peak, one can conclude that after 900 °C annealing, the HfO_2 sample underwent obvious interface oxidation leading to the formation of SiO_2, due to oxygen diffusing into the HfO_2/Si interface. However, in comparison with the HfO_2 sample, the SS sample does not show such an obvious increase in Si–O, indicating that the SS sample can enhance the resistance to oxygen diffusion. Additionally, the interfacial SiO_2 in both as-deposited films is from the remnant oxide on the substrates after pretreatment according to their comparability in intensity.

From Figs. 2 and 3, it can be seen that SS films retain the merits of the HfO_xN_y dielectric, i.e., better thermal stability and immunity to oxygen diffusion compared with a pure HfO_2 film. However, the electrical properties of a pure HfO_xN_y film are poor compared with those of a pure HfO_2 film, including capacitance and leakage indicators of MOS devices. Since the HfO_xN_y component is limited at the surface region and the main body of the SS film bulk is HfO_2 dielectric, with its good thermal stability and limitation of interfacial oxidation, the electrical properties of SS film are as good as (even better than) HfO_2 film. The left inset in Fig. 4 plots the hysteresis voltage versus different annealing temperatures for SS and HfO_2 dielectrics. As the annealing temperature of the SS film is increased, the hysteresis voltage of the *C*–*V* curve is basically decreased. This suggests that the interface state and fixed charge are reduced after the PDA process. However, for HfO_2 film, in the lower annealing temperature region, it retains a lower hysteresis compared with SS film. When it comes to higher temperature annealing, due to the earlier crystallization, the quality of the HfO_2 interface is degraded, leading to an increase of hysteresis value. The slight re-rise of the SS sample at the highest annealing temperature should also be due to the occurrence of crystallization, since the HfO_xN_y layers are relatively thin compared with the enwrapped HfO_2 bulk. The frequency dependences of the capacitance values for 900 °C annealed SS and HfO_2 gate dielectrics are shown in the right inset. It is obvious that the capacitance value of SS film is almost independent of frequency, suggesting that the SS samples possess fewer interface states. However, the capacitance value of HfO_2 film clearly decreases as frequency increases from 100 kHz to 1 MHz, interpreted as showing the presence of excessive interface traps even after PDA treatment. In any case, considering the inevitability of high-temperature heat treatment in the semiconductor industry, the SS sample possesses obvious advantages. Additionally, this improvement of SS sample

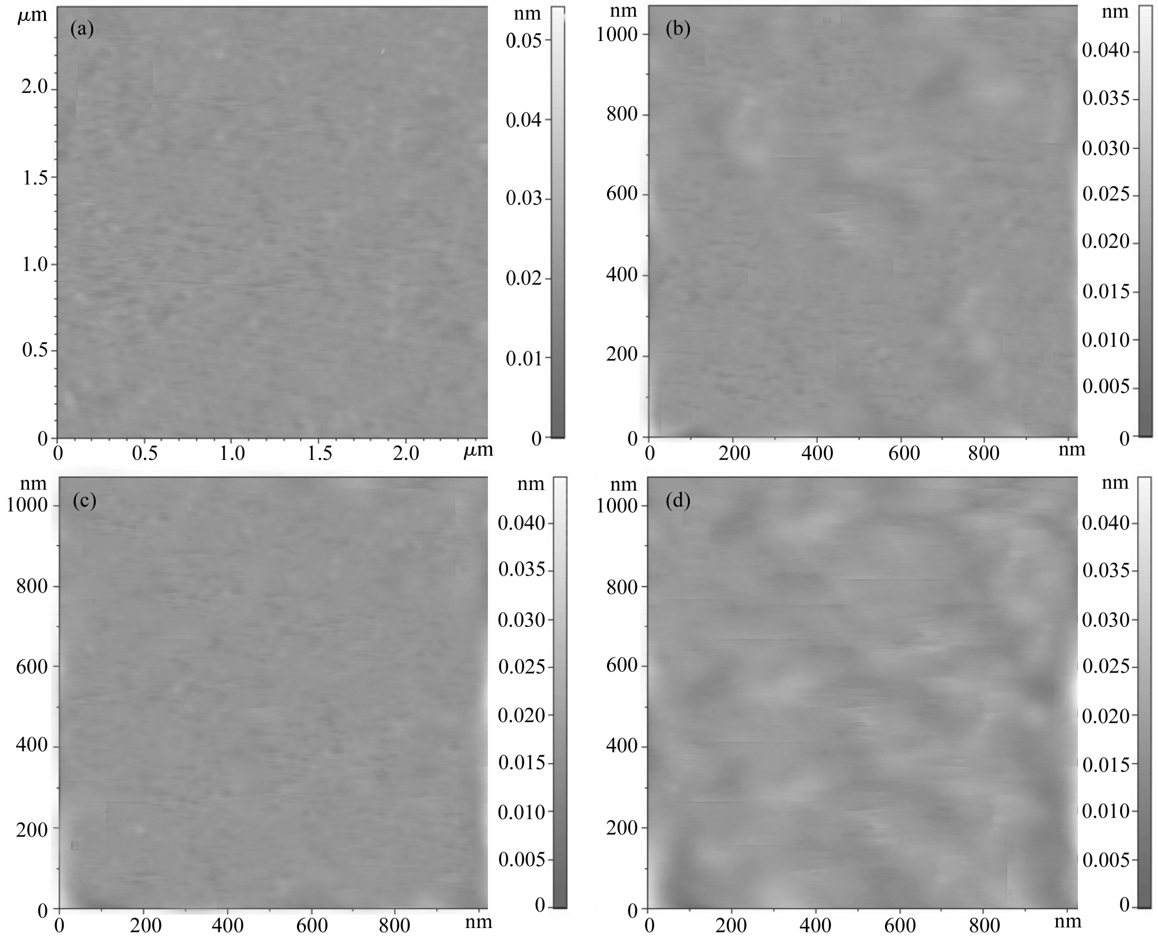

Fig. 2. AFM micrographs of HfO_2 and SS samples annealed at 900 °C in N_2 atmosphere for 60 s compared with respective as-deposited samples. (a) SS sample without annealing; (b) SS sample annealed at 900 °C; (c) HfO_2 sample without annealing; (d) HfO_2 annealed at 900 °C. The scan size for the HfO_2 sample (Figs. 1(c) and 1(d)) is from the same scan area. The scan for the SS sample is intentionally chosen to be different. Even though the scan area of the SS sample before annealing is much larger than that after annealing, the latter (Fig. 1(b)) does not yet visually show apparent rough morphology compared with the former (Fig. 1(a)).

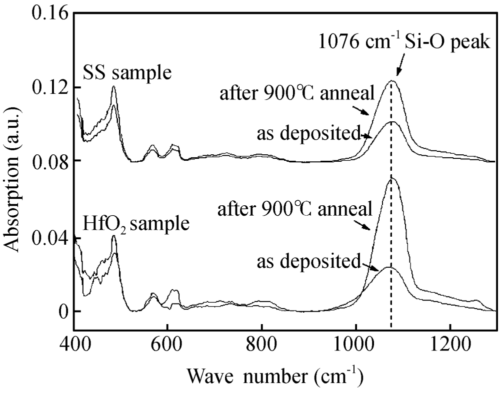

Fig. 3. FTIR spectra of HfO_2 and SS samples annealed in N_2 atmosphere for 60 s at 900 °C compared with respective as-deposited samples.

could be enhanced by high temperature annealing. Figure 4 plots high-frequency *C–V* curves measured on the MOS capacitors with SS film as-deposited and annealed at 900 °C in N_2 ambient for 60 s. The as-deposited film revealed large counterclockwise hysteresis due to the interface states and trapped charges at defect sites. It should be noted that the SS gate dielectric annealed at 900 °C in N_2 ambient shows a very small hysteresis voltage at flatband. This phenomenon is believed to be due to the fact that harbor trapped charges at defect sites are apparently passivated. It also implies that the SS structure needs thermal treatment to obtain better device performance.

As is well known, carrier mobility and leakage current are the basic indicators for MOS devices. To further investigate the influence of thermal treatment on device performance with SS film, carrier mobility and leakage properties were investigated as shown in Fig. 5. Using the split *C–V* method with inversion capacitance and output current in MOS devices, the effective channel electron mobility (μ_{eff}) could be calculated using the following equation:

$$\mu_{\mathrm{eff}}\left(V_{\mathrm{g}}\right)=\frac{L^2}{V_{\mathrm{d}}}\frac{I_{\mathrm{d}}\left(V_{\mathrm{g}}\right)}{\displaystyle\int_{V_0}^{V_{\mathrm{g}}}C_{\mathrm{gc}}\left(V_{\mathrm{g}}\right)\mathrm{d}V_{\mathrm{g}}}, \tag{1}$$

where C_{gc} is the gate-to-channel capacitance; I_{d} is the drain current; V_{g} is the gate voltage; L is the device length and V_0

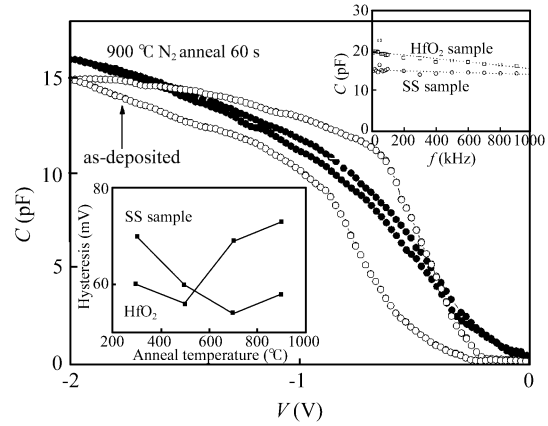

Fig. 4. C–V curves of as-deposited and annealed SS dielectric films measured at 1 MHz by sweeping the voltage from inversion to accumulation and back again. The left inset shows hysteresis versus various annealing temperatures for comparative HfO$_2$ and SS samples. The right inset shows the capacitance value versus frequency for 900 °C annealed HfO$_2$ and SS films from 10 kHz to 1 MHz.

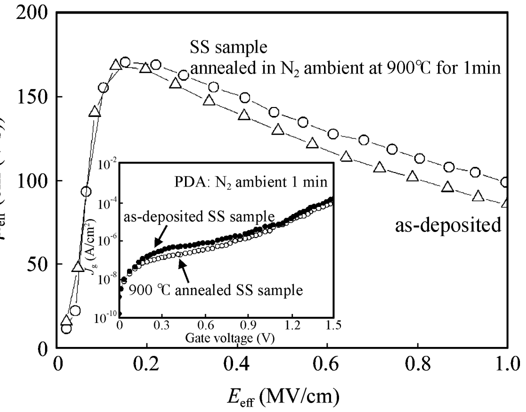

Fig. 5. Effective channel electron mobility as a function of effective electric field in as-deposited and annealed SS samples. Annealing was performed at 900 °C in N$_2$ ambient for 1 min. The inset shows the SILC characteristics of the SS dielectric before and after 900 °C annealing. Samples were stressed under 0.5 MV/cm for 1000 s.

is the gate voltage at which $C_{\rm gc}$ is negligible. Here V_0 was assumed to be zero. $L = 2\ \mu$m, and $V_{\rm d} = 50$ mV. To suppress the influence of GIFBE[17] on extracted values of $\mu_{\rm eff}$, $I_{\rm d}$ was replaced by the integral of the gate transconductance measured at high frequency:

$$I_{\rm d} = \int_{V_0}^{V_{\rm g}} G_{\rm m}(V_{\rm g}){\rm d}V_{\rm g} + I_{\rm d0},\ \ \text{where } I_{\rm d0} = I_{\rm d} \text{ at } V_{\rm g} = V_0. \quad (2)$$

One can see from Fig. 5 that the channel mobility of the annealed sample is higher than that of the as-deposited one. The results demonstrate that both the fixed charges in the bulk of the SS film and the interface states decreased due to annealing, since more fixed charges and trap defects could enhance Coulomb scattering which further results in mobility degradation. This result also confirms the fact that thermal annealing treatment is necessary for SS film to form better interface morphology and to reduce defects in bulk. However, the increase of channel mobility is not so obvious after annealing in Fig. 5, which could be due to the screening of the inversion layer since at large inversion densities ($N_{\rm inv}$) the effect of Coulomb scattering will be effectively suppressed due to the electron screening effect. Therefore, the improvement effect due to annealing cannot be entirely reflected by the mobility behavior. Additionally, stress induced leakage current (SILC) characteristics of SS dielectric are shown in the inset. The annealed sample shows lower SILC characteristics. In other words, SILC characteristics are improved on increasing the annealing temperature. Since the overall trap density of the film decreases with increasing anneal temperature, the leakage current by trap-assisted tunneling of electrons also decreases. Better SILC characteristics means that the films possess higher immunity to stress and breakdown. Therefore, it is important to retain the PDA process after the deposition of SS films.

4. Conclusion

In this paper, the characteristics of SS film were investigated compared with pure HfO$_2$ films of the same thickness. It is revealed that SS film can effectively increase thermal stability and block oxygen diffusion. Meanwhile, a MOS capacitor with an SS gate dielectric shows a lower hysteresis voltage and excellent capacitance stability in C–V curves. Therefore, SS film shows the merits of both the HfO$_x$N$_y$ and HfO$_2$ dielectrics. Meanwhile, high-temperature annealing treatment is necessary for the SS film to achieve better device performance including higher channel mobility and lower SILC.

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