A multiple-pass ring oscillator based dual-loop phase-locked loop[*]

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Abstract: A dual-loop phase-locked loop (PLL) for wideband operation is proposed. The dual-loop architecture combines a coarse-tuning loop with a fine-tuning one, enabling a wide tuning range and low voltage-controlled oscillator (VCO) gain without poisoning phase noise and reference spur suppression performance. An analysis of the phase noise and reference spur of the dual-loop PLL is emphasized. A novel multiple-pass ring VCO is designed for the dual-loop application. It utilizes both voltage-control and current-control simultaneously in the delay cell. The PLL is fabricated in Jazz 0.18-μm RF CMOS technology. The measured tuning range is from 4.2 to 5.9 GHz. It achieves a low phase noise of –99 dBc/Hz @ 1 MHz offset from a 5.5 GHz carrier.

Key words: coarse-tuning; dual-loop; fine-tuning; phase-locked loop; phase noise
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1. Introduction

The challenge for broadband phase-locked loops (PLL) is to achieve a wide frequency tuning range, while providing a low integrated phase noise and spurious tone level. A wide tuning range requires a large voltage-controlled oscillator (VCO) gain. However, a small VCO gain is appreciated for good phase noise and low spur level. One way to reduce the VCO gain while maintain a moderate tuning range is to use switched capacitors[1]. But a serious disadvantage of the switched tuning scheme is that digital circuitry is needed to select the right VCO tuning curve before starting the PLL operation. The digital logic system that controls the switching must be carefully integrated into the design in order to guarantee correct locking automatically and stability over the complete range[2, 3].

In this paper, an architecture which retains the advantages of a low VCO gain and wide tuning range, without the need of a digital calibration circuit is presented. This is achieved by continuously adjusting the VCO characteristic with an analog coarse control. A resistor-less coarse-tuning loop and a stabilizing fine-tuning loop are combined in parallel without switching[4]. Modeling and analysis of the phase noise and reference spur for the dual-loop PLL is developed here. It shows a better noise performance compared to a single-loop PLL, while the coarse-tuning loop hardly affects the spur level of the PLL.

The ring VCO excels in the small size and large tuning range compared to the LC-VCO. A novel ring VCO is designed for the dual-loop PLL. It has a large VCO gain for a wide tuning range. An even smaller VCO gain can be got for better phase noise and reference spur suppression.

Also, the dual-loop architecture is introduced. A detailed analysis of the phase noise and reference spur performance of the unique structure is performed. The circuit design of the VCO is described.

2. Dual-loop architecture

A block diagram of the dual-loop PLL architecture is shown in Fig. 1. The PLL is composed of two parallel loops sharing the same phase-frequency detector (PFD) and frequency divider (DIV). The charge pump (CP) of the coarse-tuning loop is capacitively loaded, whereas the charge pump of the fine-tuning loop is loaded with a second-order low-pass filter. The coarse-tuning loop cannot be stable on its own, but when combined with the fine-tuning loop in parallel, a stable system can be achieved. The two loops work together all the time, that is, switching is not required at all.

The VCO has two control inputs with the VCO gain K_{v1} and K_{v2}. Analysis shows that if C_2 meets Eq. (1), the small-signal behavior of the dual-loop PLL has little relationship with the coarse-tuning loop[4].

$$C_2 \gg \frac{I_2 K_{v2}}{I_1 K_{v1}} C_1, \tag{1}$$

wherein I_1, C_1, K_{v1} and I_2, C_2, K_{v2} are the charge pump current, filter capacitor, and the VCO gain of the fine-tuning loop
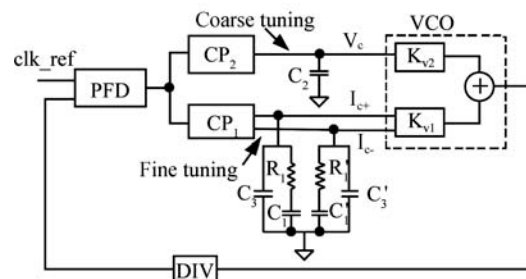

Fig. 1. Block diagram of dual-loop PLL.

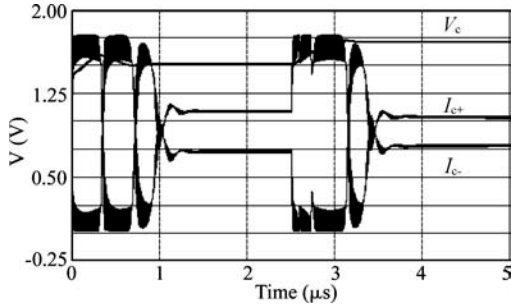© 2009 Chinese Institute of Electronics
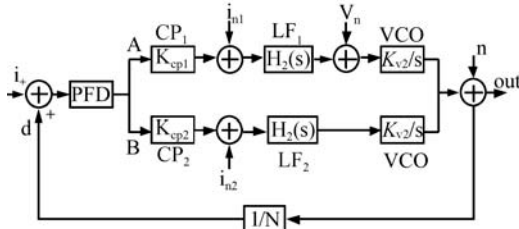
Fig. 2. Transient response of the PLL.

Fig. 3. Phase noise modeling.

and coarse-tuning loop, respectively. That is, the Bode plot, bandwidth, and phase margin are the same as for the fine-tuning loop only, representing a traditional single-loop PLL. Adding in a coarse-tuning loop just helps to enlarge the tuning range. Hence, a large VCO gain K_{v2} is used in the coarse-tuning loop for a wide frequency tuning range. A small VCO gain K_{v1} is used in the fine-tuning loop, which is important for reduction of both the reference spur and phase noise.

In this design, the coarse-control signal vc is single-ended whereas the fine-control signal (I_{c+}, I_{c-}) is differential to provide better suppression of noise. Figure 2 is the transient response of the PLL. At the time of 2.5 μs, the division ratio changes. v_c adjusts continuously until the PLL reaches a new stable state with the fine-control signal (I_{c+}, I_{c-}).

3. System analysis

Phase noise and spur are the critical problems taken into account in the PLL designs. The characteristics of this unique dual-loop architecture on the aspects of phase noise and reference spur are fully investigated in the following.

3.1. Phase noise evaluation

Figure 3 shows the modeling of the phase noise in this dual-loop PLL. Noise sources are added in the loop. i_{n1} and i_{n2} represent the current noise source caused by CP_1 and CP_2 respectively. V_n represents the voltage noise source of loop filter 1 (LF_1). Since no resistor is used in the loop filter of the coarse-tuning loop, there is no corresponding voltage noise source added after LF_2. θ_n represents the phase noise of VCO. As only one VCO is used, this noise source is presented in the common path.

The open loop transfer function is given by:

$$H_o(s) = \frac{K_{cp1}H_1(s)\dfrac{K_{v1}}{s} + K_{cp2}\dfrac{1}{sC_2}\dfrac{K_{v2}}{s}}{N}, \quad (2)$$

where N is the division ratio, K_{cp} is the gain of PFD and CP, $K_{cp1} = I_1/2\pi$, $K_{cp2} = I_2/2\pi$, and $H_1(s)$ is the transfer function of LF_1. If the small capacitance C_3 is neglected for simplicity, then $H_1(s) = R_1 + 1/sC_1$.

The closed loop transfer function $H_c(s)$ could be written as:

$$H_c(s) = \frac{sK_{cp1}K_{v1}H_1(s)C_2 + K_{cp2}K_{v2}}{s^2C_2 + (sK_{cp1}K_{v1}H_1(s)C_2 + K_{cp2}K_{v2})/N}. \quad (3)$$

Hence the noise transfer function of DIV, CP_1, CP_2, LF_1, and VCO, which are marked as H_d, H_{i1}, H_{i2}, H_v, and H_n respectively, could be derived as follows:

$$H_d = \frac{sK_{cp1}K_{v1}H_1(s)C_2 + K_{cp2}K_{v2}}{s^2C_2 + (sK_{cp1}K_{v1}H_1(s)C_2 + K_{cp2}K_{v2})/N}, \quad (4)$$

$$H_{i1} = \frac{K_{v1}H_1(s)}{s + [K_{cp1}K_{v1}H_1(s) + K_{cp2}K_{v2}/sC_2]/N}, \quad (5)$$

$$H_{i2} = \frac{K_{v2}/sC_2}{s + [K_{cp1}K_{v1}H_1(s) + K_{cp2}K_{v2}/sC_2]/N}, \quad (6)$$

$$H_v = \frac{K_{v1}}{s + [K_{cp1}K_{v1}H_1(s) + K_{cp2}K_{v2}/sC_2]/N}, \quad (7)$$

$$H_n = \frac{s}{s + [K_{cp1}K_{v1}H_1(s) + K_{cp2}K_{v2}/sC_2]/N}. \quad (8)$$

The total noise contribution at output is given by

$$S_o(s) = S_{d,n}(s)|H_d|^2 + S_{i1,n}(s)|H_{i1}|^2 + S_{i2,n}(s)|H_{i2}|^2$$

$$+ S_{v,n}(s)|H_v|^2 + S_{vco,n}(s)|H_n|^2, \quad (9)$$

where $S_{d,n}$, $S_{i1,n}$, $S_{i2,n}$, $S_{v,n}$, and $S_{vco,n}$ is the equivalent noise sources' power spectral density (PSD) of DIV, CP_1, CP_2, LF_1, and VCO, respectively.

If C_2 meets Eq. (1) and $I_1 = I_2$, then $K_{v2}/sC_2 \ll K_{v1}/H_1(s)$. Comparing Eqs. (5) and (6) gives that $|H_{i2}| \ll |H_{i1}|$. Given the same charge pump current which results in $S_{i1,n} = S_{i2,n}$, the noise contribution of CP_2 is negligible compared to that of CP_1. Note that CP_2 is the only added noise-contribution component of the dual-loop architecture to a single one.

For a single-loop PLL, i.e. the PLL without the coarse-tuning loop in Fig. 1, the noise transfer function of CP_1, LF_1, and VCO, which are marked as H'_{i1}, H'_v, and H'_n respectively, could be derived as follows.

$$H'_{i1} = \frac{K_{v1}H_1(s)}{s + K_{cp1}K_{v1}H_1(s)/N}, \quad (10)$$

$$H'_v = \frac{K_{v1}}{s + K_{cp1}K_{v1}H_1(s)/N}, \quad (11)$$

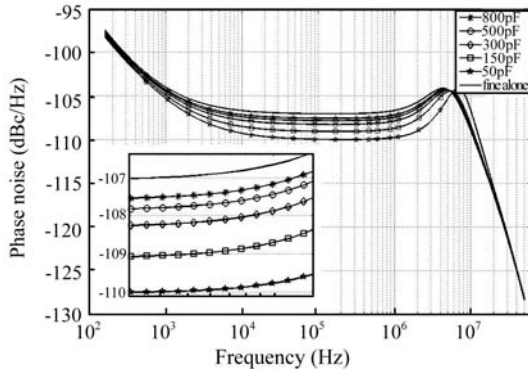$$H'_n = \frac{s}{s + K_{cp1}K_{v1}H_1(s)/N}. \quad (12)$$

Fig. 4. Phase noise performance with different C_2.

Fig. 5. Schematic view of the delay cell.

In most cases, the phase noise within the loop bandwidth is dominated by CP, the phase noise outside the bandwidth is dominated by VCO, and LF has important noise contribution around the bandwidth. It is easy to find an item of $K_{cp2}K_{v2}/sC_2N$ included in the denominator of H_{i1}, H_v, and H_n while other items are the same compared to H'_{i1}, H'_v, and H'_n. This implies a smaller noise transfer function of CP, LF and VCO in the dual-loop PLL than that in a single one. Hence, instead of deteriorating the noise performance of the single loop as initially thought, the presence of the coarse-tuning loop even improves the noise performance slightly. Referring to Eqs. (5)–(8), a small value of C_2 results in a small transfer function and a better noise performance. But C_2 can not be too small for the consideration of stability. Figure 4 shows the phase noise of a certain design with different values of C_2 compared to that of fine-tuning alone. The phase noise around the 1 MHz offset is enlarged at the bottom-left.

3.2. Spur evaluation

Reference spurs are a problem in PLL designs. These spurs appear at multiples of the comparison frequency. Dead-zone elimination circuitry, charge pump mismatches, and unequal transistor turn on times influence the time that the charge pump is on, which dominates the reference spurs in modern PLLs, except at low comparison frequencies where the leakage currents dominate the spurs.

To predict reference spurs caused by the pulsing action of charge pump, the following rule applies[5]:

$$\text{Spur} = \text{BaseSpur} + \text{SpurGain} + 40\lg\left(\frac{F_{\text{spur}}}{1\,\text{Hz}}\right), \qquad (13)$$

where BaseSpur is related to the charge pump current mismatch or turn on time mismatch. F_{spur} is the spur offset frequency of interest. SpurGain is the closed loop transfer function evaluated at F_{spur}. In cases where F_{spur} is outside the loop bandwidth, the SpurGain can be approximated using the open loop transfer function instead of the closed loop transfer function.

Both the fine-tuning loop and the coarse-tuning loop have an influence on spurs. If the charge pump circuit and current are same in the fine-tuning and coarse-tuning loops, the BaseSpur would be same as well. However the SpurGain of the two loops would be quite different as shown in Eqs. (14)
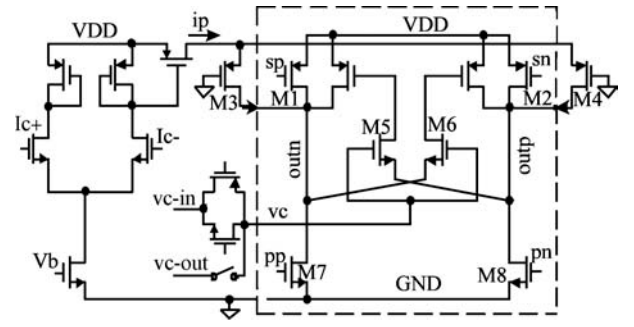
and (15). It is easy to see that $\text{SpurGain}_f \ll \text{SpurGain}_c$. This means that the fine-tuning loop dominates spur performance.

$$\text{SpurGain}_f = 20\lg\left|K_{cp1}K_{v1}H_1(s)/(Ns)\right|_{s=jF_{\text{spur}}\cdot 2\pi}, \qquad (14)$$

$$\text{SpurGain}_c = 20\lg\left|K_{cp2}K_{v2}/(Ns^2C_2)\right|_{s=jF_{\text{spur}}\cdot 2\pi}. \qquad (15)$$

The spur of the dual-loop PLL could be written as:

$$\text{Spur} = \text{BaseSpur} + 20\lg(10^{\text{spurGain}_f/20} + 10^{\text{spurGain}_c/20})$$
$$+ 40\lg\left(\frac{F_{\text{spur}}}{1\,\text{Hz}}\right) \qquad (16)$$

The difference in spur may be within 1 dBc with or without the coarse-tuning loop, so the presence of the coarse-tuning loop has little effect on the reference spur level. Intuitively, since a low-pass filter instead of a single capacitor is used as the loop filter, the fine-tuning loop has a much wider bandwidth than the coarse-tuning loop. Hence, the pulse-induced ripple on the control signal of the coarse-tuning loop would be much more attenuated. As a result, the coarse-tuning loop hardly affects the spur performance of the PLL.

4. Circuit design

A novel ring oscillator is designed for the dual-loop PLL. It utilizes voltage control and current control simultaneously to provide dual-controlled inputs. The single-stage delay cell of the ring oscillator is shown in Fig. 5. In the dashed pane is a full swing delay cell. Frequency is controlled by varying the strength of the latch. The positive feedback gain in the latch increases with v_c by reducing the MOS resistance of M5 and M6, which makes it difficult to change the output voltage, thus reducing the oscillation frequency. Two transmission gate switches are added to toggle between the coarse-tuning loop vc_in and the outside vc_out for measurement purposes.

A pair of transistors M3 and M4 is applied to the basic delay cell. They provide an additional amount of current to the output nodes (outn, outp), hence the charging and discharging current at these nodes is varied, and so is the oscillating frequency. The left part of the circuit in Fig. 5 is a voltage-to-current module. It changes the total injected current i_P according to the differential input control signal (I_{c+}, I_{c-}). The gates of PMOS transistors M3 and M4 are connected to GND. These two transistors are always on, undergoing linear region or saturated region. The injected current i_P is split into two ways, one to outn and the other to outp. The amount of each depends on the voltage of the output node. Since the injected current
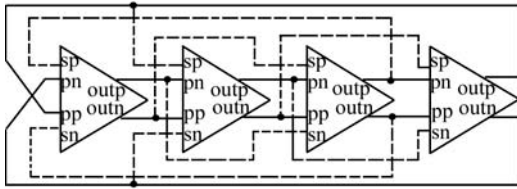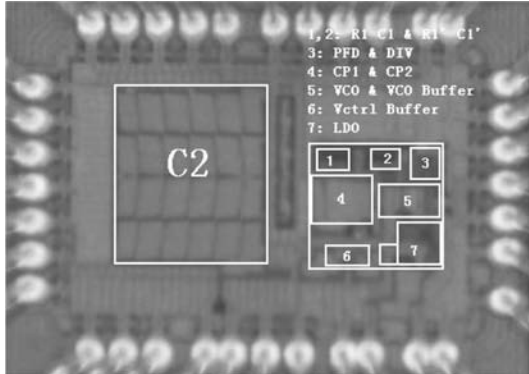
Fig. 6. Multiple-pass ring VCO topology.

Fig. 7. Die photograph.

Fig. 8. Measured VCO tuning curves.

Fig. 9. Output spectrum at 5.5 GHz with both loops on.

is rarely small compared to the inherent current in the delay cell, a small variation in frequency is obtained, corresponding to a small VCO gain. With this structure, the latch feedback control provides coarse-tuning, while the fine-tuning is done using a differential input current control. A differential control network is helpful to reduce the susceptibility to noise on the control lines.

The VCO topology in this design is shown in Fig. 6. A fully differential multiple-pass loop with four stages is adopted for high frequency operation and quadrature outputs. Multiple-pass loops are often based on feed-forward theory[6]. That is, besides the normal path, there is a fast auxiliary path which transmits input to output end. Multiple-pass structure takes the advantages of the fast path to reduce the delay time from VCO. The solid lines in Fig. 6 are the normal path for a four-stage differential ring VCO while the dashed lines are the fast auxiliary path. The transistors M1 and M2 in Fig. 5 are added for the fast auxiliary path[7].

A differential charge pump with its common mode feedback circuit is utilized to generate the two differential control signals (I_{c+}, I_{c-}). A low drop output (LDO) circuit is used to provide a clean and stable power for the VCO. A low-power truly modular programmable divider is designed to change the division ratio N[8].

5. Implementation and measurement

A dual-loop PLL is implemented in Jazz 0.18-μm RF CMOS technology. A die photo is shown in Fig. 7. The total area and the active region occupy 1.5×1.1 mm^2 and 0.36×0.4 mm^2, respectively. The value of the large capacitor in the coarse-tuning loop C_2 is 500 pF, which occupies more than half of the die area. It could be made off chip to reduce cost[4].

The four-stage multiple-pass ring oscillator is tested separately. Figure 8 shows the tuning characteristic of the VCO.
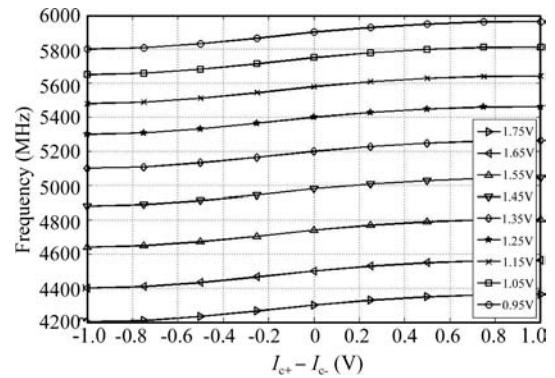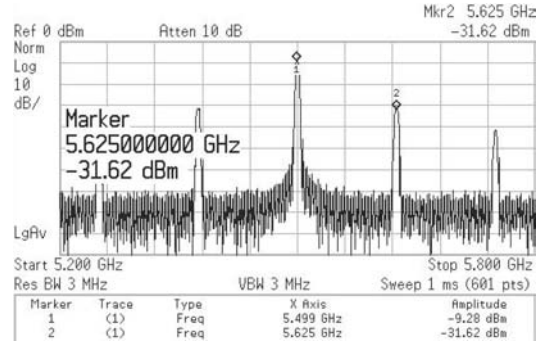
The x-axis is the differential control voltage in the fine-tuning loop. Different tuning lines correspond to different coarse-control voltages. The small gain of VCO in the fine-tuning loop is about 120 MHz/V. The large gain of VCO in the coarse-tuning loop is about 2 GHz/V. The VCO covers a wide tuning range from 4.2 to 5.9 GHz. It is worth pointing out that the coarse-tuning voltage is not limited to those shown in Fig. 8. In closed loop operations, it is determined by combining the coarse-tuning loop and the fine-tuning loop to a stable point.

The v_c signal could be generated by the coarse-tuning loop or directly input from outside through a switch as shown in Fig. 6. Measured by an Agilent PSA Spectrum Analyzer E4440A, it shows that the levels of reference spurs in the fine-tuning loop alone and the dual-loop simultaneously are almost the same. Figure 9 shows the PLL output spectrum at the center frequency of 5.5 GHz when both loops are on. The reference spurs occur at an offset of comparison frequency of 125 MHz or multiples of the comparison frequency to the carrier.

The first spur level is –22 dBc, which is a little too large. But it is not caused by the coarse-tuning loop. Actually, the spurs can also be observed in the spectrum at an offset of division frequency and multiples of that when only the VCO and DIV are on, with a level of –30 dBc. The offset changes when the VCO frequency varies. Obviously, it is mainly caused by the cross talk both within the chip and on the test board. A pad connected to the divider's output was set too close to that of the VCO. The parasitic capacitances will allow high frequency signals to travel from one trace to another. Removing of that pad or putting it far away from the VCO output should lead to a much better spur performance.
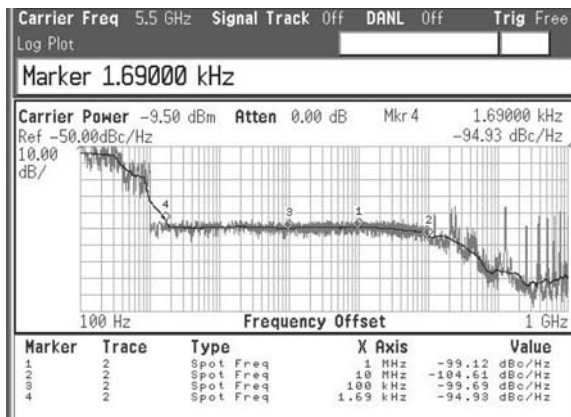
Fig. 10. Measured phase noise of the PLL.

Table 1. Comparison of the proposed PLL with prior work.

Reference	Ref. [4]	Ref. [7]	This work
PLL loop	Dual	Single	Dual
VCO	LC	Ring	Ring
Process (μm)	0.25 SiGe	0.18 CMOS	0.18 CMOS
Supply (V)	2.5	1.8	1.8
Frequency (GHz)	4.12–4.72	5.16–5.93	4.2–5.9
Phase noise (dBc/Hz) @1 MHz	NA	−99.5*	−99.1
Power (mA)	47	NA	58

*Simulation result of the VCO from a 5.79 GHz center frequency

The measured phase noise at a carrier frequency of 5.5 GHz is shown in Fig. 10, when both loops are on and the division ratio is 44. It achieves –99.12 dBc/Hz @ 1 MHz. The bandwidth is designed to be about 10 MHz, as 125 MHz reference frequency applied. The PLL draws a current of 58 mA from a 1.8 V supply at this frequency. Table 1 summarizes a comparison of this dual-loop PLL to previous work reported on integer-N frequency synthesizers. The frequency tuning range is much wider than previous publications. The phase noise is comparable to the ring-based one at comparative frequencies. The power consumption is a little more than the LC-based one. But with the process scaling down, the power of the proposed PLL could be reduced by a large amount.

6. Conclusions

A multiple-pass ring oscillator based dual-loop PLL is designed. The dual-loop architecture combines a coarse-tuning loop with a fine-tuning one for a wide tuning rang and low VCO gain. The phase noise of the dual-loop PLL is derived, which shows a better noise performance compared to the single-loop PLL. Analysis shows that the deterioration in reference spur by the coarse-tuning loop can be neglected. A novel VCO is designed for the dual-loop application. It utilizes voltage-control and current-control simultaneously in the delay cell and provides a large VCO gain of 2 GHz/V and a small VCO gain of 120 MHz/V for coarse tuning and fine tuning respectively. This dual-loop PLL architecture is desirable in wideband operation.

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