Influence of body contact of SOI MOSFETs on the thermal conductance of devices

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Abstract: The thermal conductance of devices with different body contacts is studied. A new analytical expression is proposed. This expression can be used in parameter extraction, which gives both good efficiency and high precision. The ratio of thermal conductance of the body contact region to that of the body region is nearly equal to the ratio of the area. The use of an H shape gate body contact is suggested to aid power dissipation in SOI MOSFETs.

Key words: thermal conductance; body contact; parameter extraction; power dissipation
DOI: 10.1088/1674-4926/30/9/094001 **EEACC:** 2530F; 2560B

1. Introduction

Silicon-on-insulator (SOI) technology is becoming a mainstream technology for future VLSI applications due to its potentially increased circuit speeds and simpler fabrication process. These advantages arise from the presence of the buried insulating layer, most commonly silicon dioxide, which reduces the parasitic source/drain-to-substrate junction capacitance, limits the depth of the source/drain junction to form simple shallow junctions, and allows full dielectric isolation of the device to eliminate latchup[1–3]. But the low thermal conductivity of the underlying silicon dioxide layer, which is about two orders of magnitude less than that of silicon, inhibits cooling in SOI devices and causes severe self-heating. This results in higher channel operating temperatures and is evidenced by the negative differential conductance at high gate biases that is characteristic of most SOI devices. Even with a 100 nm thin BOX (buried oxide), the SOI MOSFET's DC I–V characteristics, from which the SPICE simulation model parameters are extracted, suffer current loss due to the SHE (self-heating effect)[4–6]. On the other hand, for most logic circuits in VLSI, SHE is insignificant. Since the average power consumption per device is low and its switching time, ∼10 ps, is much shorter than the thermal time constant, ∼100 ns, the time-averaged and transient device temperature increases due to SHE are quite small. Therefore, for accurate logic circuit simulation, there is a thermal auxiliary circuit in SOI SPICE models[7, 8]. Once the SHE-free parameters are obtained, one can execute accurate circuit simulation by a model flag, SHMOD, the "self-heating mode", SHMOD = 1 or 0 for the thermal auxiliary circuit's inclusion or exclusion, respectively, depending on the type of circuit. In this thermal auxiliary circuit, an important parameter, the thermal conductance, $G_{\rm th}$, should be known. Although there have been some methods to measure the thermal conductance, they are not suitable for use when there are too many devices, such as in parameter extraction. The current method in common use is to measure $G_{\rm th}$ of some devices and compute $G_{\rm th}$ of other devices via its dependence on geometry[9]. Early research considers that $G_{\rm th}$ is proportional to the gate width, $W_{\rm g}$[8, 10, 11]. Recent research considers that $G_{\rm th}$ is made up of two parts[12, 13]. The first part represents the dissipation via source/drain films and is proportional to $W_{\rm g}$. The second part is introduced to represent dissipation via the gate electrode and body contact region and is constant. For the common use of body contact in SOI MOSFETs, it is required to study the thermal conductance change arising from the body contact. In this paper, the thermal conductance of different devices is studied and a new analytical expression is proposed. There is also a comparison between $G_{\rm th}$ arising from different body contacts, and a determination of which kind of body contact should be used to aid heat dissipation.

2. Devices and simulation

We set the thickness of the gate oxide of NMOS devices for simulation as 20 nm, and the thicknesses of the bulk silicon and buried oxide are both 370 nm. The thickness of the substrate silicon is 450 μm, and that of the poly-silicon gate is 0.3 μm. The doping concentrations of boron in the bulk silicon and substrate silicon are 1×10^{16} cm^{-3}, and that of arsenic in the source and drain region is a Gaussian function, and the peak concentration is 1×10^{20} cm^{-3}. The doping concentration of arsenic in poly-silicon gate is 1×10^{18} cm^{-3}. These devices are partially depleted SOI MOSFETs. The channel length is 0.35 μm. There are four types of device: floating body (FB), body-tied-source (BTS), T shape gate body contact (TG), and H shape gate body contact (HG). Figure 1 shows the layouts of these four types of device. Each type has four devices, and their gate widths are 0.35, 0.7, 1.05, and 1.4 μm. The width of the body contact is 0.45 μm. These sixteen devices were simulated in ISE TCAD 10.0. A hydrodynamic model accounts for energy transport for the carriers and is suitable for devices with small active regions. In this simulation this model is used to compute the temperature of the device. A recombination model and a mobility model are also used. We set the voltage of drain as 2 V, and began the simulation. After the simulation is completed, the current and temperature can be read from the

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Received 18 February 2009, revised manuscript received 25 April 2009

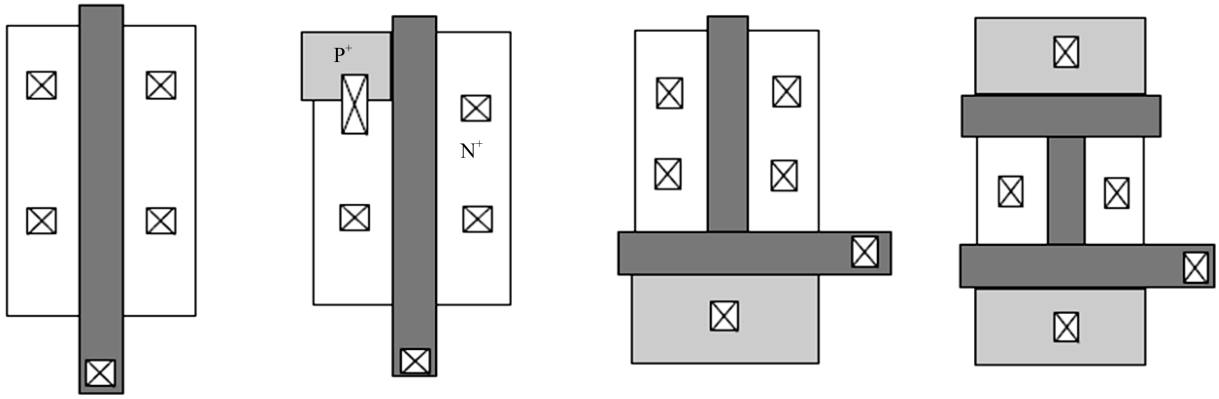

Fig. 1. Layout of four types of device: (a) Floating body (FB); (b) Body-tied-source (BTS); (c) T shape gate body contact (TG); (d) H shape gate body contact (HG).

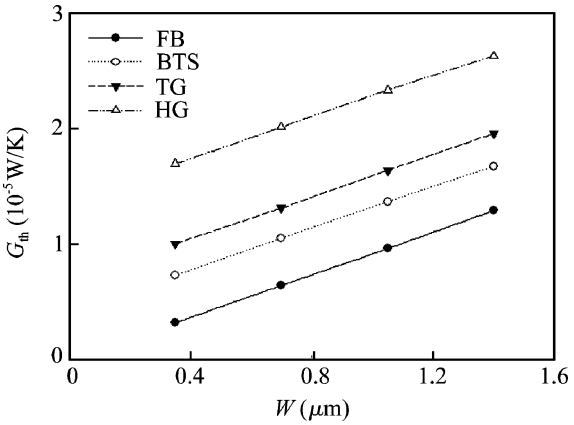

Fig. 2. Thermal conductance of the devices in the simulation results. The types corresponding to the four lines are HG, TG, BTS, and FB from top to bottom.

software. Then the thermal conductance can be computed:

$$G_{\text{th}} = \frac{P}{\Delta T} = \frac{IU}{T - T_0}. \tag{1}$$

P is the dissipated power, and I and U are the currents through the channel and the drain voltage, respectively. T_0 is the room temperature which equals 300 K, and T is the channel temperature after the simulation is completed, which means the power is dissipated on the device.

3. Results and discussion

3.1. Results

Figure 2 shows the thermal conductance of each device in the simulation results. Each type has four devices, and the curve of the thermal conductance (G_{th}) of these four devices versus the channel width (W) is nearly a straight line. Regarding W as the independent variable and G_{th} of the same type of device as the dependent variable, a group of fitting parameters is obtained. Then each straight line can be expressed analytically:

For FB, $G_{\text{th}} = 9.22 \times 10^{-6} \times W - 3.39 \times 10^{-8}$. (2)

For BTS, $G_{\text{th}} = 8.99 \times 10^{-6} \times W + 4.18 \times 10^{-6}$. (3)

For TG, $G_{\text{th}} = 9.07 \times 10^{-6} \times W + 6.82 \times 10^{-6}$. (4)

For HG, $G_{\text{th}} = 8.89 \times 10^{-6} \times W + 1.38 \times 10^{-5}$. (5)

For FB, because the second term is much less than the first term, it can be ignored. This means the thermal conductance of the floating body device is proportional to the gate width, which is proposed by earlier research. When there is a body contact, the expression can be divided into two terms. The first term represents the dissipation via source/drain films and is proportional to the gate width, W. The parameter of the first term can be seen as the thermal conductance of part of the corresponding device, and this part has a gate width of 1 μm. The second part is introduced to represent dissipation via the body contact region and is constant. It also can be seen as the thermal conductance of the body contact region.

The above expressions can be rewritten as follows:

For FB, $G_{\text{th}} = 9.22 \times 10^{-6} \times W$. (6)

For BTS, $G_{\text{th}} = 8.99 \times 10^{-6} \times (W + 0.46)$. (7)

For TG, $G_{\text{th}} = 9.07 \times 10^{-6} \times (W + 0.75)$. (8)

For HG, $G_{\text{th}} = 8.89 \times 10^{-6} \times (W + 1.56)$. (9)

These expressions are new analytical expressions of thermal conductance of the different types of devices. Considering the trait of simulation by software, the absolute value of thermal conductance may be incorrect, but the ratio of thermal conductance of the body contact region to that of the body region is credible. So Equations (6)–(9) can be rewritten as:

For FB, $G_{\text{th}} = G_{\text{th1}} \times W$. (10)

For BTS, $G_{\text{th}} = G_{\text{th2}} \times (W + 0.46)$. (11)

For TG, $G_{\text{th}} = G_{\text{th3}} \times (W + 0.75)$. (12)

For HG, $G_{\text{th}} = G_{\text{th4}} \times (W + 1.56)$. (13)

G_{th1}–G_{th4} should be obtained from actual measurement.

3.2. Use in parameter extraction

For the case of parameter extraction, we can measure the thermal conductance of two or three devices chosen from many devices which have the same channel length and device structure. Substituting the measurement value of thermal conductance and channel width to the corresponding equation, G_{th1}–G_{th4} can be computed. Then the thermal conductance of the other devices can be computed by Eqs. (10)–(13). The precision of thermal conductance can be improved by a new ex-

traction methodology[9], so accessing the thermal conductance of the devices for parameter extraction by this method not only saves time, but also has high precision.

3.3. Power dissipation in different devices

On the other hand, the ratio of thermal conductance of the body contact region to that of the body region is nearly equal to the ratio of the area. This is easy to understand. The main difference between the body region and the body contact region is the doping species and concentration, and the material and size of substrate between the different regions are the same. The determinant of thermal conductance is the thermal conductivity and thickness of the substrate material. The doping species and concentration make no difference to the thermal conductance. Since the low thermal conductivity of the underlying silicon dioxide layer causes a severe self-heating effect, to help the SOI devices dissipate power more quickly so that the temperature of channel is not high enough to cause invalidation, it is suggested that in SOI ICs the body contact should be used as much as possible and the H shape gate body contact has the best effect on power dissipation, although it uses the biggest area.

4. Conclusion

The thermal conductance of devices with different body contacts is studied. There are four types of device: FB, BTS, TG, and HG. A new analytical expression is proposed based on the simulation in ISE TCAD 10.0. For the case of parameter extraction, we can measure the thermal conductance of two or three devices chosen from many devices which have the same channel length and device structure. Then the thermal conductance of the other devices can be computed by the expressions obtained above. This method not only saves time, but also has high precision. It also can be seen from the analytical expressions that in SOI ICs the body contact should be used as much as possible, and the H shape gate body contact has the best effect on power dissipation, although it uses the biggest area.

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