10 Gb/s OEIC optical receiver front-end and 3.125 Gb/s PHEMT limiting amplifier*

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Abstract: A 10 Gb/s OEIC (optoelectronic integrated circuit) optical receiver front-end has been studied and fabricated based on the ϕ-76 mm GaAs PHEMT process; this is the first time that a limiting amplifier (LA) has been designed and realized using depletion mode PHEMT. An OEIC optical receiver front-end mode composed of an MSM photodiode and a current mode transimpedance amplifier (TIA) has been established and optimized by simulation software ATLAS. The photodiode has a bandwidth of 10 GHz, a capacitance of 3 fF/μm and a photosensitive area of 50 × 50 μm^2. The whole chip has an area of 1511 × 666 μm^2. The LA bandwidth is expanded by spiral inductance which has been simulated by software HFSS. The chip area is 1950 × 1910 μm^2 and the measured results demonstrate an input dynamic range of 34 dB (10–500 mVpp) with constant output swing of 500 mVpp.

Key words: OEIC; MSM photodiode; current mode; TIA; depletion mode PHEMT; limiting amplifier
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1. Introduction

A monolithic optoelectronic integrated circuit (OEIC) optical receiver front-end is a novel type of device that integrates a photodiode and pre-amplifier onto one chip. It can improve the performance and stability of the device because of the elimination of the bonding wire and parasitic[1,2]. It has the advantages of small size, cost-effectiveness and high reliability, and will be very widely used in the fields of large capacity optical fiber communications, optical access networks, photoelectric sensor arrays, miniature photoelectric sensors, optical computers, optical storage, optical switches, optical neural networks, and so on.

With the development of the technology and the market demand, OEICs have become more complex and contain more components. Ultimately, they will fully integrate optoelectronic devices, pre-amplifier, main amplifier and clock and data recovery circuits. In this paper, a limiting amplifier is designed and realized by using depletion mode PHEMT for the first time. It is not suitable for depletion mode (D mode) HEMT in limiting amplifier design because of its own limits and therefore the study abroad is based on a mixed process of enhancement mode (E mode) and D mode HEMT[3–7]. A differential structure is used in the limiting amplifier and a higher standard of process is demanded, which is considered in the circuit design. This is the technical basis for full integration of the OEIC optical receiver.

2. Design and simulation of OEIC device

In this paper, ATLAS software was used to simulate and optimize the characteristics of the device. ATLAS[8] is a physically based device simulator which applies a set of differential equations derived from physics of semiconductor devices to simulate the transport of carriers through the device. First, a structure of the optical receiver front-end was defined; the cross-sectional structure of the device is shown in Fig. 1. Then, the parameters of the physical models, including Schottky barrier height, absorption coefficient and so on, were generated through experimental data[9–15], though the effects of deep level defects have been neglected. Finally, the mathematic method was selected and the solution parameters were defined. Figure 2 shows the character of MSM PD: it has a bandwidth of more than 10 GHz and a capacitance of 3 fF/μm. It is shown that a general characteristic of MSM PD is that the capacitance values and dark current change little with bias.

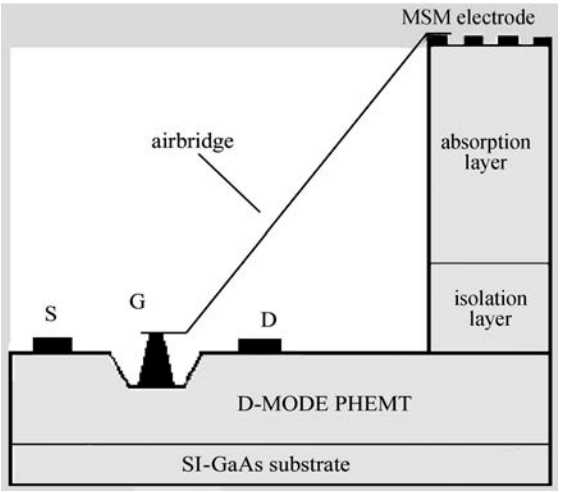

Fig. 1. Structure of the OEIC device.

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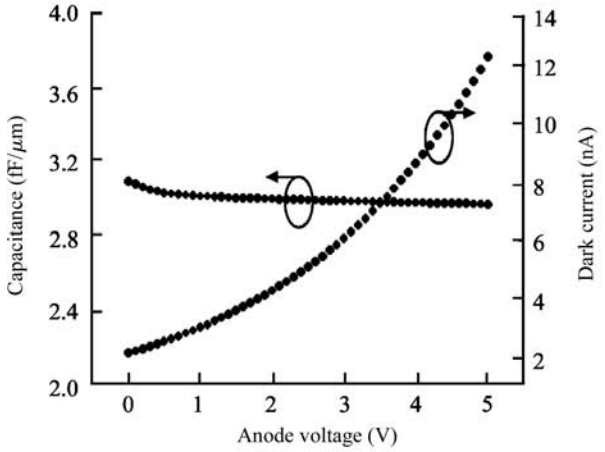

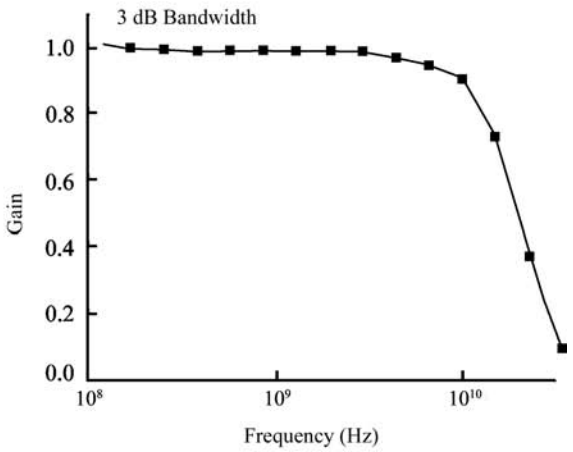

Fig. 2. Character of MSM PD.

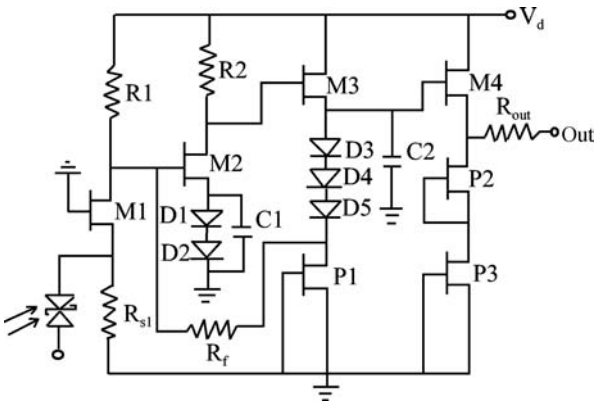

Fig. 3. Schematic of the current mode TIA.

Fig. 4. Small signal S parameter of the current mode TIA.

The device was grown by molecular beam epitaxy (MBE) on a semi-insulating (S.I.) 3-inch GaAs substrate, and consists of PHEMT, an isolation layer and an absorption layer. There is a compatibility problem between planar and mesa technology because the MSM photodiode is about 1 μm higher than the plane of the circuit device. So in terms of the whole process, mesa is one of the key technologies.

3. Current mode TIA design

A single power supply current mode TIA has been developed based on the GaAs PHEMT low noise amplifier (LNA) process. Figure 3 shows a schematic of the current mode TIA, which consists of a common-gate input stage, a common-source gain stage and two source followers. In this schematic, a feedback resistance $R_{\rm f}$ is applied from the source of M3 to the gate of M2, through which a shunt–shunt negative feedback is formed. To improve the gain shape and broaden the bandwidth, a peaking capacitor C2 is placed between the two source followers. The shunt capacitor C1 tends to reduce the negative feedback caused by D1 and D2 to improve the small signal gain, especially at high frequencies. The amplifier has a measured –3 dB bandwidth close to 8 GHz and a transimpedance gain of nearly 50 dBΩ. Figure 4 shows the small signal S parameter of the current mode TIA by using an Agilent 8720ES vector network analyzer (VNA).

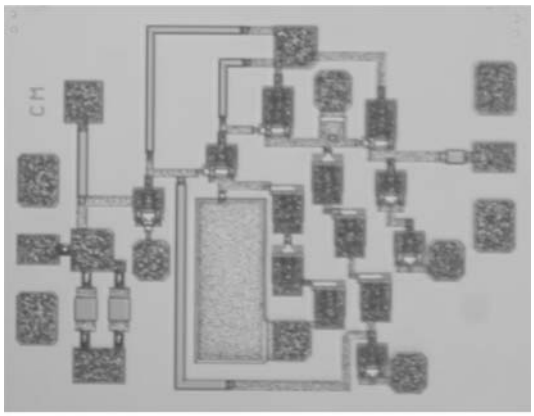

Fig. 5. Optical receiver

4. Measurement results of the OEIC optical receiver front-end

Figure 5 shows a micrograph of the OEIC optical receiver front-end, which has an area of $1511 \times 666\ \mu{\rm m}^2$. The bottom-left down corner of the chip is an MSM photodiode which connects with the current mode TIA through a 10 μm long air-bridge. The output eye diagram, shown in Fig. 6, was obtained at data up to 10 Gb/s with a pseudorandom bit sequence (PRBS) of length $2^{15}-1$. The integrated MSM photodiode exhibited a front-side illumination responsivity of 0.85 μm.

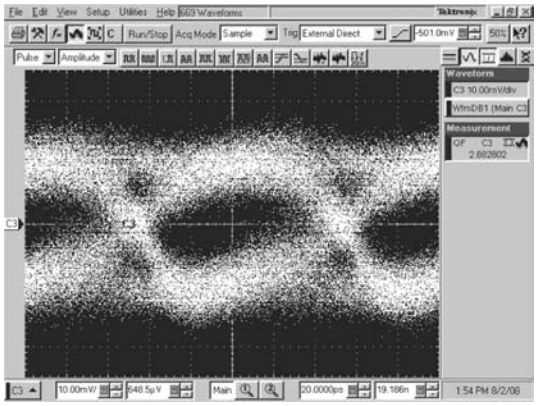

Fig. 6. Eye-diagram of optical receiver front-end.

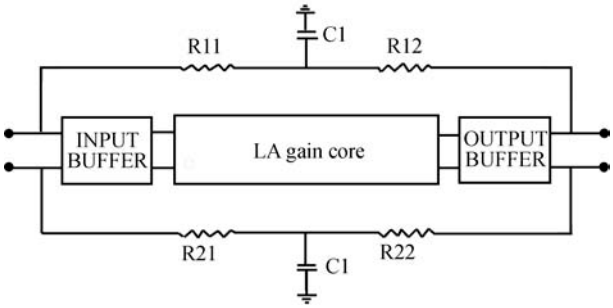

Fig.7. Block diagram of the limiting amplifier.

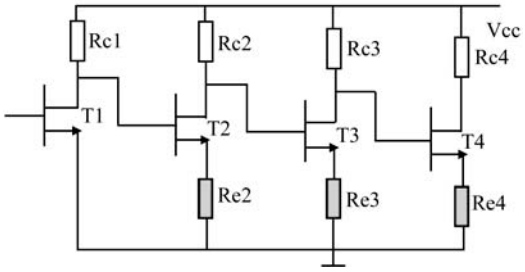

Fig. 8. Multi-stage

5. Design and test of the limiting amplifier

As shown in Fig. 7, the fully differential circuit consists of an input buffer for 50 Ω impedance match and level-shifting. The LA gain core includes several similar gain stages. An output buffer is used for driving 50 Ω transmission lines. A pair of RC feedback networks are used for DC offset compensation, which is very important to the LA. It is not suitable for depletion mode (D-mode) HEMT to design the limiting amplifier because of its own limit. Direct coupled gain stages are utilized to achieve high gain and low power as illustrated in Fig. 8. The DC bias will be enhanced by increasing the circuit stage, which will reduce circuit dynamic performance and stability.

Therefore, popular study is based on a mixed process of enhancement mode (E-mode) and D-mode HEMT. In this paper, a limiting amplifier is designed and realized by using depletion mode PHEMT, and it is used for full integration of an OEIC optical receiver.

The typical gain stage is difficult to operate at high bit rates due to its large load capacitance. An effective way to increase the gain-bandwidth product is to introduce an inductive component into the loads of the differential pairs, which is known as the shunt peaking technique. By partly tuning out the capacitive loading, the pole of each stage can be moved to a higher frequency. With a suitable choice of inductors, both a maximal flat response and a substantial bandwidth extension can be obtained simultaneously.

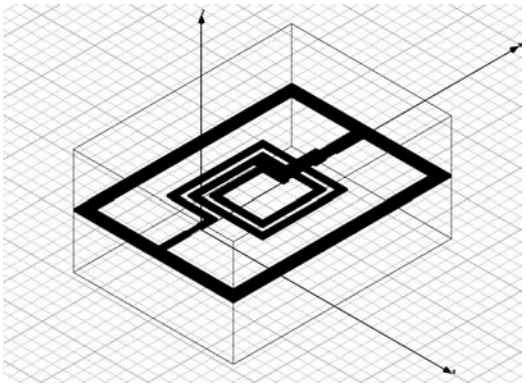

Fig. 9. Inductance structure in HFSS.

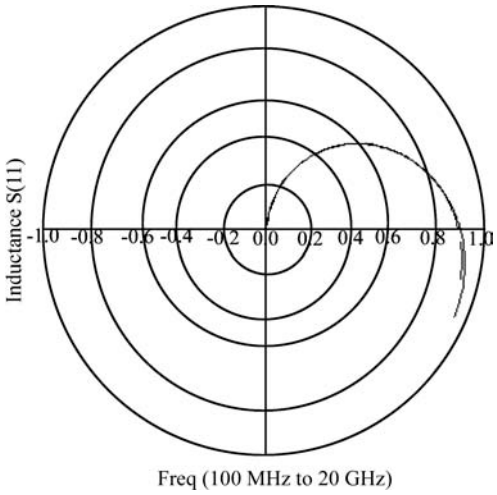

Fig. 10. Simulated and measured results of inductance.

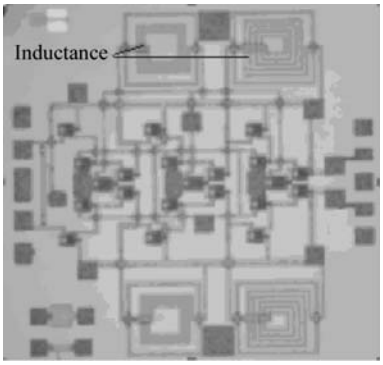

Fig. 11. Microphotograph of the LA.

It is difficult to design a spiral inductor because of the mutual inductance and parasitic transmission line. In this paper, the spiral inductor has been designed and simulated by software HFSS of the Ansoft Corporation, as shown in Fig. 9, and it shows a good match with the measured results of the device, as shown in Fig. 10.

A chip microphotograph of the LA is shown in Fig. 11 and its area is 1950 × 1910 μm^2. Figure 12 shows an eye-diagram of the LA measured at a bit rate of 3.125 Gb/s with

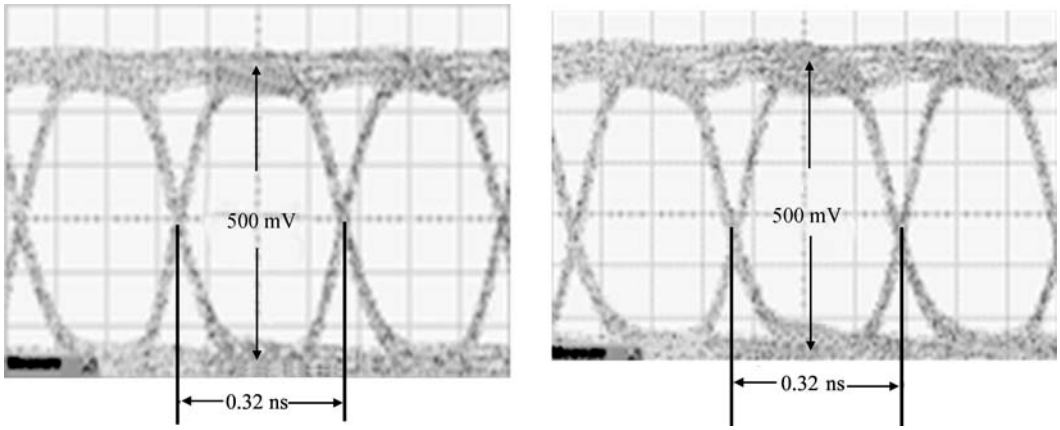

Fig. 12. Eye diagram measurement.

input signals of 10 mVpp and 500 mVpp, and the output voltage swing is kept at 500 mVpp.

6. Conclusion

A 10 Gb/s OEIC optical receiver front-end and limiting amplifier have been studied and fabricated based on the GaAs depletion mode PHEMT process. This is a very important experiment to realize full integration of the OEIC optical receiver. The structure of the device, process and circuit design should be optimized carefully to improve the characteristics of bandwidth and noise.

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