A new double gate SOI LDMOS with a step doping profile in the drift region*

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Abstract: A new double gate SOI LDMOS with a step doping profile in the drift region is proposed. The structure is characterized by one surface gate and another embedded gate under the P-body region. The broadened current flow path and the majority carrier accumulation layer on the side wall of the embedded gate reduce the specific on-resistance ($R_{\text{on, sp}}$). The electric field distribution is improved due to the embedded gate and step doping profile, resulting in a high breakdown voltage (BV) and low $R_{\text{on, sp}}$. The influences of device parameters on BV and $R_{\text{on, sp}}$ are investigated by simulation. The results indicate that BV is increased by 35.2% and $R_{\text{on, sp}}$ is decreased by 35.1% compared to a conventional SOI LDMOS.

Key words: SOI; embedded gate; electric field; breakdown voltage; specific on-resistance

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1. Introduction

Silicon-on-insulator (SOI) technology has attracted much attention due to its advantages such as high speed, low power consumption, superior isolation and latch-up immunity[1, 2]. However, the key issue in SOI power devices is to obtain a trade-off between breakdown voltage and specific on-resistance[3]. To solve this problem, several structures are proposed[4−10], in which SOI LDMOSFETs (lateral-double-diffusion- metal-oxide-semiconductor- field-effect-transistors) with a recessed source and trench drain or with a double epi-layer and trench electrodes are proposed[5, 6]. A step-thickness SOI layer or a step doping profile in the drift region can be used to enhance BV and maintain a low $R_{\text{on, sp}}$[8−10].

An asymmetrical double gate SOI LDMOS with a step doping profile (AsDG SOI LDMOS) is proposed in this paper. In blocking state, the embedded gate electrode improves surface field distribution and enhances the breakdown voltage. A broadened current flow path and a majority carrier accumulation layer on the side wall of the embedded gate reduce the $R_{\text{on, sp}}$ in on-state. Furthermore, a step doping profile in the drift region introduces a new peak electric field on the interface of step profile divisions[8−10]. Compared with a conventional SOI LDMOS, BV of AsDG SOI LDMOS is increased by 35.2% and $R_{\text{on, sp}}$ is lowered by 35.1% in the simulation.

2. Structure and mechanism

Figure 1 is a schematic cross section of an AsDG SOI LDMOS. t_s, t_{ox} are the thicknesses of the SOI layer and buried oxide layer, respectively. L_d is the drift region length. In this paper, L_d = 12 μm, t_s = 3 μm, t_{ox} = 2 μm. t_{g1} and t_{g2} are the vertical and lateral extension lengths of the embedded gate, respectively. t_d is the depth of the trench-drain electrode. For a surface drain electrode, t_d = 0. The drift region is divided into regions Ⅰ and Ⅱ, with their doping concentration $N_{d1} < N_{d2}$.

In the blocking state, the step doping profile introduces a new surface electric field peak on the interface between regions Ⅰ and Ⅱ, which reduces the electric field peaks at source- and drain-ends and thus avoids premature breakdown there. So a high BV is obtained. The following three causes contribute to a reduced $R_{\text{on, sp}}$: (1) the broadened current flow path; (2) the majority carrier accumulation layer on the side wall of the embedded gate; (3) the step doping profile which raises the total charges in the drift region. The AsDG SOI structure can obtain a trade-off between BV and $R_{\text{on, sp}}$.

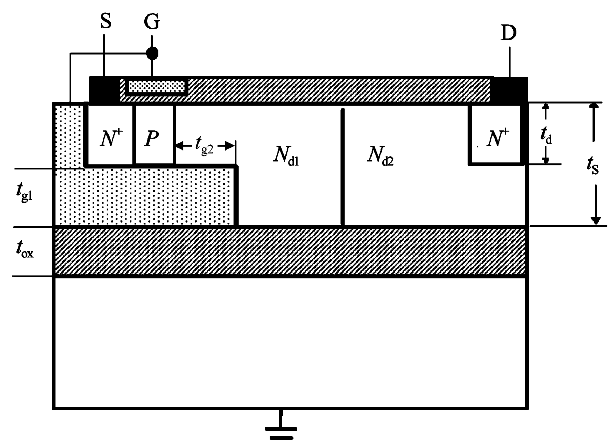

Fig. 1. Schematic cross section of an AsDG SOI LDMOS.

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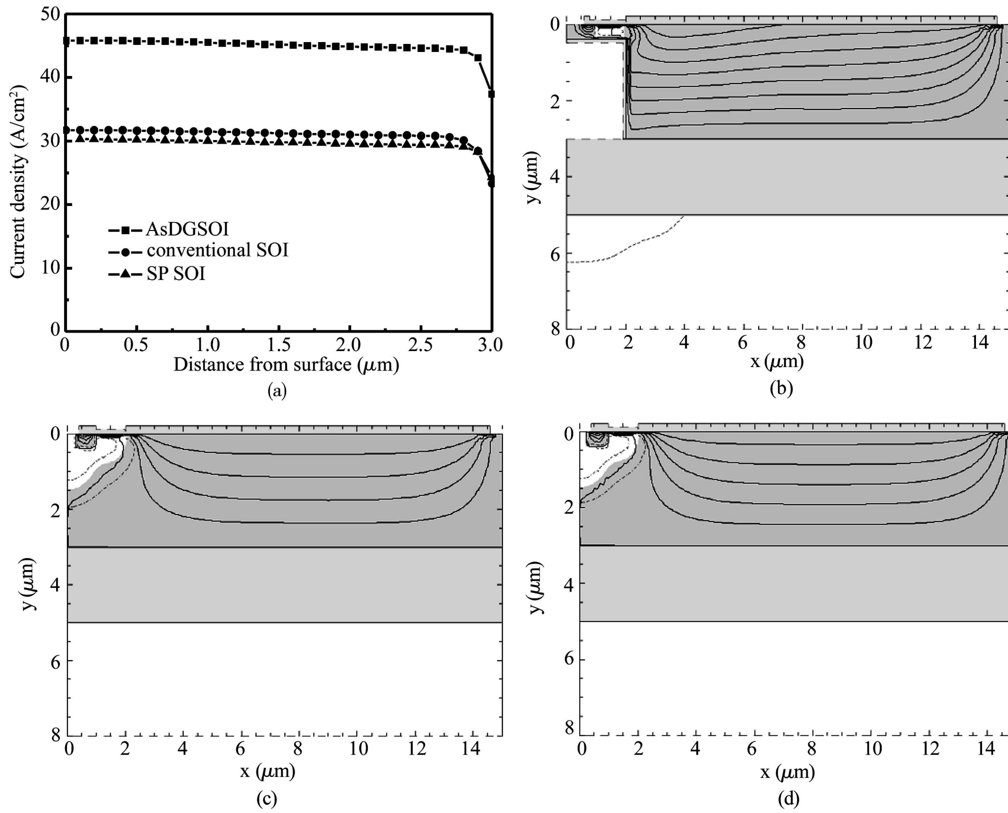

Fig. 2 (a) Vertical current density along $x = 10\ \mu$m in the SOI layer ($V_G = 10$ V and $V_D = 0.1$ V); (b) Current flow lines of AsDG SOI LDMOS; (c) Current flow lines of SP SOI LDMOS ($N_{d1} = 2 \times 10^{15}$ cm^{-3} and $N_{d2} = 5.5 \times 10^{15}$ cm^{-3}); (d) Current flow lines of conventional SOI LDMOS ($N_d = 3 \times 10^{15}$ cm^{-3}).

3. Results and discussion

Figure 2 gives the vertical current distribution of the AsDG SOI LDMOS, conventional SOI LDMOS and conventional SOI LDMOS with step profiles (SP SOI) along $x = 10$ μm (in the middle of the drift region). As shown in Fig. 2(a), the current density of the conventional SP SOI is almost the same as that of the conventional SOI for their respective optimized doping concentrations. The optimized doping concentrations of $N_{d1} = 3 \times 10^{15}$ cm^{-3} and $N_{d2} = 6 \times 10^{15}$ cm^{-3} reduce the drift region resistance for the AsDG SOI LDMOS, therefore, the maximum value of current density is raised by 43.7% and its minimum value is increased by 63% compared with those of the conventional SOI. The corresponding values are 53% and 56% compared with those of SP SOI. The broadened current flow path by the extended embedded gate and the majority carrier accumulation layer on the side wall of the embedded gate increase the current density for the AsDG SOI, as illustrated in Figs. 2(b), 2(c), 2(d). Figure 2 confirms the fact that AsDG SOI can enhance BV and reduce $R_{on,sp}$.

Figure 3 gives the surface electric field distributions for the above three SOI devices. Compared with the conventional one, both the AsDG SOI and conventional SP SOI have a new electric field peak on the interface of step profile divisions. Furthermore, the embedded gate also raises the surface electric field in the first division of the drift region. Due to the modulation effect of the embedded gate, the electric field peaks at the source- and drain-ends of AsDG SOI are reduced, avoiding premature breakdown. Both lead to a higher BV than that of the conventional SP SOI. When the doping concentration of the AsDG SOI is applied to the conventional SP SOI, BV for the latter is only 110 V due to the undepleted SOI layer. This shows that the embedded gate electrode also raises the optimized concentration of the drift region, and thus reduces $R_{on,sp}$.

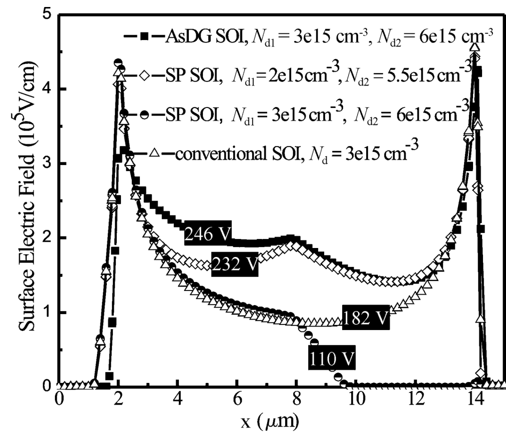

Fig. 3. Surface electric field profiles for AsDG SOI, conventional SP SOI and conventional SOI devices.

Figure 4 gives the dependences of BV and $R_{on,sp}$ of AsDG SOI on t_{g1} and t_{g2}, where $N_{d1} = 3 \times 10^{15}$ cm^{-3} and $N_{d2} = 6 \times 10^{15}$ cm^{-3} in the drift region. BV and the $R_{on,sp}$ would not change significantly until $t_{g1} > 2\ \mu$m at $t_{g2} = 0\ \mu$m and

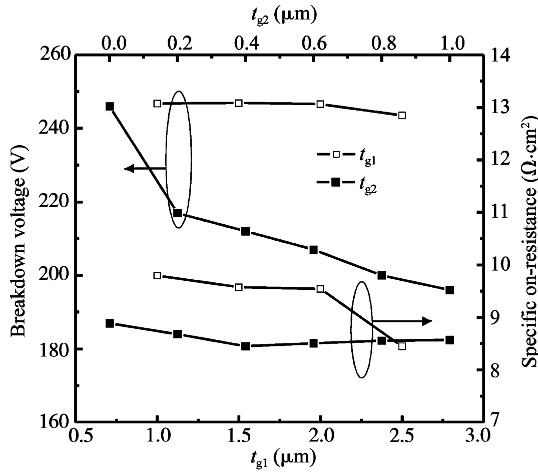

Fig. 4. Dependences of BV and $R_{on,sp}$ on t_{g1} and t_{g2}.

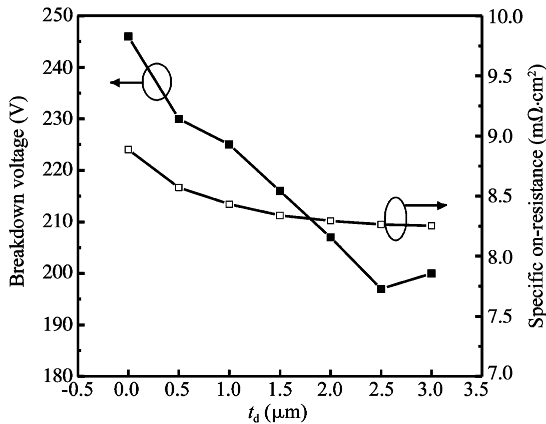

Fig. 5. Dependences of BV and $R_{on,sp}$ on t_d.

t_d = 0 μm (surface drain electrode) in Fig. 4 because the modulation effect on the electric field is weak when the embedded gate is far away from the surface (t_{g1} is small). Both BV and $R_{on,sp}$ decrease sharply at t_{g1} = 2.5 μm. BV decreases significantly while $R_{on,sp}$ slightly changes with a increasing t_{g2}. When t_{g2} is increased, equipotent lines tend to gather in the corner of the embedded gate where premature breakdown occurs. Owing to t_{g2} (1 μm) $\ll L_d$ (12 μm), so a t_{g2} increase contributes little to the accumulation of electrons and the change of $R_{on,sp}$.

Figure 5 shows the dependence of BV and $R_{on,sp}$ on t_d. The concentration of electric field causes premature breakdown in the corner of the drain electrode with increasing t_d, leading to a decreased BV. $R_{on,sp}$ decreases as t_d increases because a large electrode area can effectively collect the carriers. Compared to AsDG LDMOS with t_d = 0 μm, BV is reduced by 18.7% while $R_{on,sp}$ decreases only by 7.0% at t_d = 3 μm.

Figure 6 shows that the optimized doping concentration N_{d2} decreases if N_{d1} increases for the AsDG SOI LDMOS. When $N_{d1} = 2 \times 10^{15}$ cm^{-3} and $N_{d2} = 7 \times 10^{15}$ cm^{-3}, the maximum BV (BV_{max}) is 255 V and $R_{on,sp}$ = 10.1 mΩ· cm^2; but BV_{max} = 246 V and $R_{on,sp}$ = 8.3 mΩ· cm^2 at $N_{d1} = 3 \times 10^{15}$ cm^{-3} and $N_{d2} = 6 \times 10^{15}$ cm^{-3}. Even though BV_{max} for the latter is reduced by 3.5%, its $R_{on,sp}$ decreases by 17.8%. BV of the AsDG SOI LDMOS is increased by 35.2% and $R_{on,sp}$ is reduced by 35.1% compared with those of the conventional

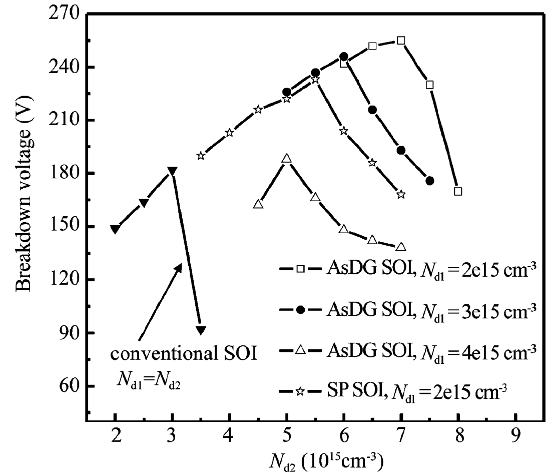

Fig. 6. Breakdown voltage versus doping concentration in drift region (AsDG SOI LDMOS, at t_{g1} = 2.5 μm, t_{g2} = 0 and t_d = 0 μm).

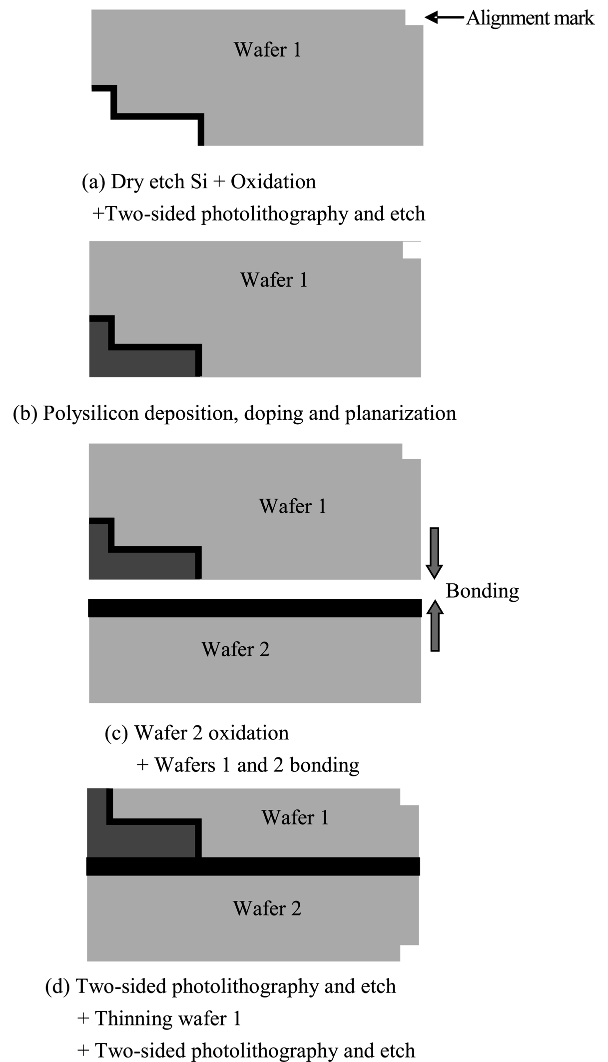

Fig. 7. Process flow charts of SOI wafer with an embedded gate.

SOI LDMOS. BV is increased by 6% and $R_{on,sp}$ is decreased by 38.5% compared with an SP SOI LDMOS. Premature breakdown occurs at the source-end surface at $N_{d1} = 4 \times 10^{15}$ cm^{-3}[9], resulting in a low breakdown voltage.

The key processes of SOI wafers with embedded gates are given in Fig. 7, including wafer 1: dry etch Si to form Si-

trenches, oxidation of Si-trenches to form gate oxide, polysilicon deposition, doping and planarization; wafer 2: oxidation; wafer 1 and 2 bonding; thinning wafer 1, in which two-sided photolithography and etch are used three times to transfer alignment marks of the buried patterns to the surface of the thinned wafer 1. The device fabrication processes on the SOI layer surface are the same as those for conventional SOI devices.

4. Conclusions

An asymmetrical double gate SOI LDMOS with a step doping profile is proposed. At the blocking state, the embedded gate modulates the electric field in the SOI layer and the step doping profile introduces a new surface electric field peak, resulting in a high BV. The broadened current flow path, coupled with the majority carrier accumulation layer on the side wall of the embedded gate and the step doping profile reduce the $R_{on,sp}$. BV is increased by 35.2% and $R_{on,sp}$ is reduced by 35.1% compared with those of a conventional SOI LDMOS.

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