Low-power CMOS fully-folding ADC with a mixed-averaging distributed T/H circuit

Liu Zhen(刘振), Jia Song(贾嵩)†, Wang Yuan(王源), Ji Lijiu(吉利久), and Zhang Xing(张兴)

(Key Laboratory of Microelectronic Devices and Circuits, Institute of Microelectronics, Peking University, Beijing 100871, China)

Abstract: This paper describes an 8-bit 125 MHz low-power CMOS fully-folding analog-to-digital converter (ADC). A novel mixed-averaging distributed T/H circuit is proposed to improve the accuracy. Folding circuits are not only used in the fine converter but also in the coarse one and in the bit synchronization block to reduce the number of comparators for low power. This ADC is implemented in 0.5 μm CMOS technology and occupies a die area of 2 × 1.5 mm^2. The measured differential nonlinearity and integral nonlinearity are 0.6 LSB/–0.8 LSB and 0.9 LSB/–1.2 LSB, respectively. The ADC exhibits 44.3 dB of signal-to-noise plus distortion ratio and 53.5 dB of spurious-free dynamic range for 1 MHz input sine-wave. The power dissipation is 138 mW at a sampling rate of 125 MHz at a 5 V supply.

Key words: analog-to-digital converter; low power; fully-folding; mixed-averaging distributed T/H circuit; bit synchronization

DOI: 10.1088/1674-4926/30/12/125013 **EEACC:** 1265H; 1280; 2570D

1. Introduction

Analog-to-digital converters (ADCs) are widely applied in many fields, especially in high-speed embedded systems, which require over 100 MHz sampling rate and low power. Folding ADCs[1, 2] present advantages over flash or pipelined ADCs because they greatly reduce the number of comparators using folding circuits and decrease power dissipation. Moreover, their speeds are comparable to those of flash ADCs. However, because the input bandwidth is limited by the folding circuits, a T/H circuit with high speed is necessary. A distributed T/H circuit[3] proves a good choice, but the accuracy of the distributed T/H circuit is not very high and needs to be improved[4, 5]. In addition, a folding ADC needs an additional bit synchronization block and comparators are usually used to produce bit synchronization signals[6]. Nevertheless, this method needs 2^{n+1} comparators for n-bit synchronization, which introduces extra comparator expenses.

In this paper, a novel mixed-averaging distributed T/H circuit is proposed which improves the accuracy and provides a better tradeoff between accuracy, size and power dissipation. In addition, a novel bit synchronization architecture is presented to reduce the number of comparators, and this architecture employs folding circuits to produce a bit synchronization signal. Therefore, folding circuits are not only used in the fine converter but also in the coarse one and in the bit synchronization block. A special low-power CMOS ADC is designed and only 22 comparators are used in the whole ADC. The ADC is implemented in 0.5 μm CMOS technology. Measured results show that the power dissipation of the ADC is 138 mW at a sampling rate of 125 MHz at a 5 V supply.

2. ADC architecture

The block diagram of the ADC is shown in Fig. 1. The ADC is composed of three parts: fine and coarse sub-converters, and a special bit synchronization block. Folding is not only used in the fine converter but also in the coarse one and the bit synchronization block. The combination of 3-bit coarse converter and 5-bit fine one is chosen for low power[7]. The interpolating factor is set as 8 to save folders. Two-stage interpolation is used after the folders and followed by the array of latched comparators. A cyclic thermometer code replaces the common thermometer code and reduces the number of comparators in the fine sub-converter by half.

3. Circuit design

3.1. Mixed-averaging distributed T/H circuit

Based on the conventional distributed T/H circuit, a novel mixed-averaging distributed T/H circuit, shown in Fig. 2, is proposed to improve the accuracy. The accuracy of a high-speed ADC with a T/H circuit mainly depends on the offset of the first-stage amplifier and the precision of sampling. Therefore, for the structure of the distributed T/H circuit, the accuracy ΔV includes two parts: the offset of the preamplifiers in distributed T/H circuits $V_{\mathrm{os,PA}}$ and the sampling precision $\Delta V_{\mathrm{sampling}}$.

$$\Delta V = V_{\mathrm{os,PA}} + \Delta V_{\mathrm{sampling}}. \quad (1)$$

The first part $V_{\mathrm{os,PA}}$ is reduced with resistive averaging[8]. Averaging is obtained by coupling the differential outputs of the preamplifiers via averaging resistors R_{av}. The zero-

† Corresponding author. Email: jias@pku.edu.cn
Received 9 April 2009, revised manuscript received 19 August 2009

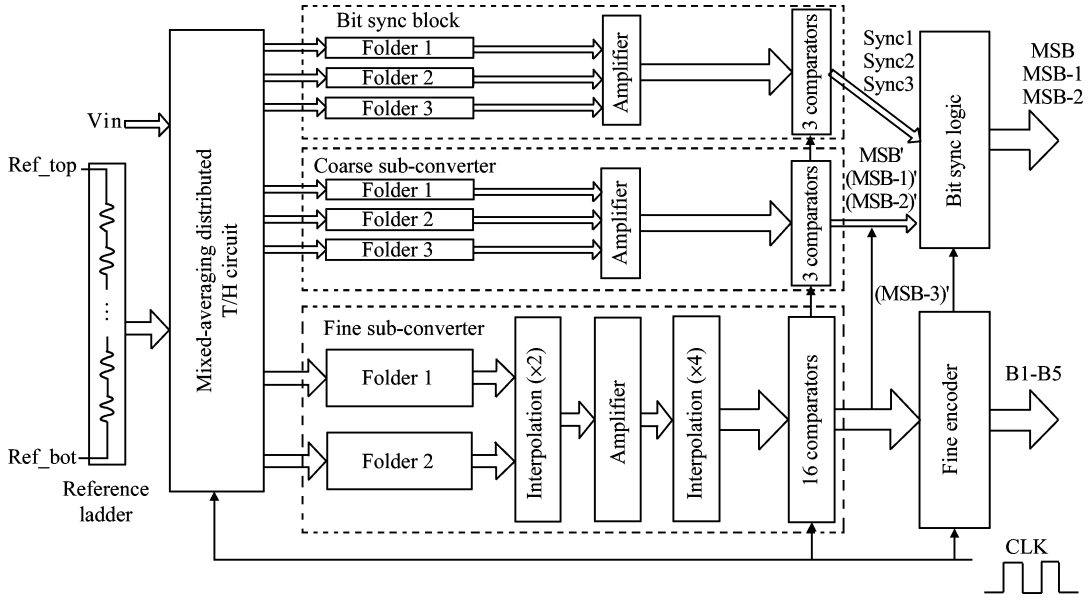


Fig. 1. Block diagram of the proposed ADC.

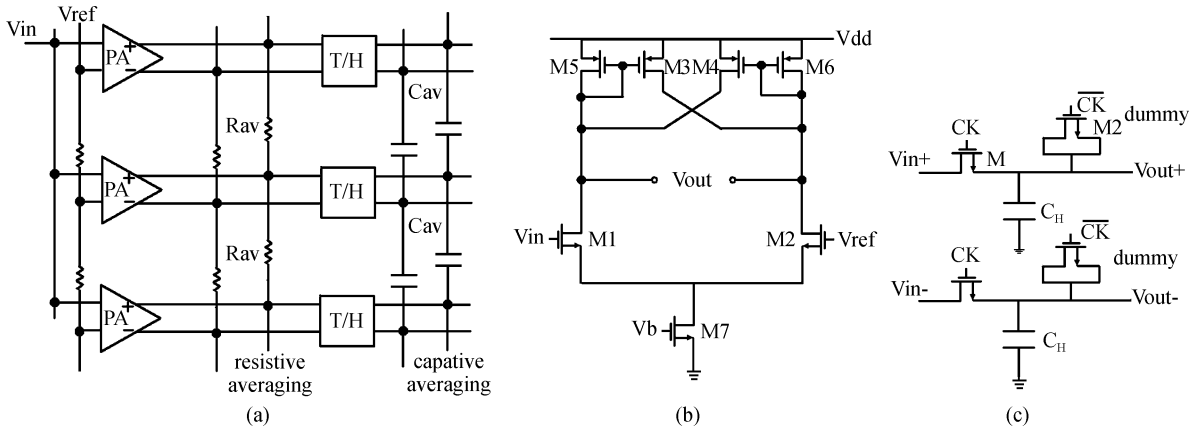


Fig. 2. (a) Mixed-averaging distributed T/H circuit; (b) Preamplifier; (c) T/H circuit.

crossing of each individual preamplifier is influenced by the neighboring preamplifiers operating in the linear input range. Dummy preamplifiers are increased at the edge of preamplifier array to make the zero-crossing accurate. In general, the offset after averaging is reduced by $\sqrt{N_{\text{active}}}$ [9]. Here N_{active} is the number of linear active preamplifiers.

$$\frac{V_{\text{os,PA}}}{V'_{\text{os,PA}}} = \sqrt{N_{\text{active}}}. \tag{2}$$

$V_{\text{os,PA}}$ and $V'_{\text{os,PA}}$ are the offsets before and after averaging. R_{eq} is then introduced to quantify the relationship between R_{av}, the output impedance of the preamplifiers R_{out} and the ratio in Eq. (2) and to guide the design. Equation (2) is also expressed as[10]:

$$\frac{V_{\text{os,PA}}}{V'_{\text{os,PA}}} = \sqrt{1 + 4\left(\frac{R_{\text{out}}}{R_{\text{eq}}}\right) + 2\left(\frac{R_{\text{out}}}{R_{\text{eq}}}\right)^2}, \tag{3}$$

where $R_{\text{eq}} = \frac{R_{\text{av}}}{2} + \frac{\sqrt{R_{\text{av}}^2 + 4R_{\text{av}}R_{\text{out}}}}{2}$. From Eq. (3), better averaging is obtained as the ratio $R_{\text{av}}/R_{\text{out}}$ decreases. However, a smaller ratio can lead to a requirement for more dummies and a lower preamplifier gain. In the design, the ratio is set as about one-fourth. A cross-coupled PMOS load, shown in Fig. 2(b), is adopted in the preamplifiers to implement very high output impedance. In this preamplifier, Mn1 = Mn2, Mp3 = Mp4 and Mp5 = Mp6. The output impedance R_{out} and the gain A_{v} are expressed respectively as:

$$R_{\text{out}} = \frac{1}{g_{\text{m5}} - g_{\text{m3}}}, \tag{4}$$

$$A_{\text{v}} = -g_{\text{m1}}R_{\text{out}} = -\frac{g_{\text{m1}}}{g_{\text{m5}} - g_{\text{m3}}}, \tag{5}$$

where $g_{\text{m3,5}} = \mu_{\text{p}}C_{\text{ox}}\frac{W}{L}(V_{\text{gs3,5}} - V_{\text{T}})$. According to the equations, very high output impedance can be obtained by the design of the ratio W_3/W_5. Therefore, although averaging resistors decrease the gain, their values can be chosen lower, still yielding a reasonable gain, which is set at about five times in the design.

The second part $\Delta V_{\text{sampling}}$ in Eq. (1) arises due to charge injection, clock feed through, clock skew and kT/C noise. Dummy switches can be added for the improvement of sampling precision, shown in Fig. 2(c). Choose $W_1 = 2W_2$ and $L_1 = L_2$. Moreover, capacitive averaging is proposed to improve the precision of sampling. Averaging capacitors C_{av} couple the output nodes of the sampling switches. A similar equation to

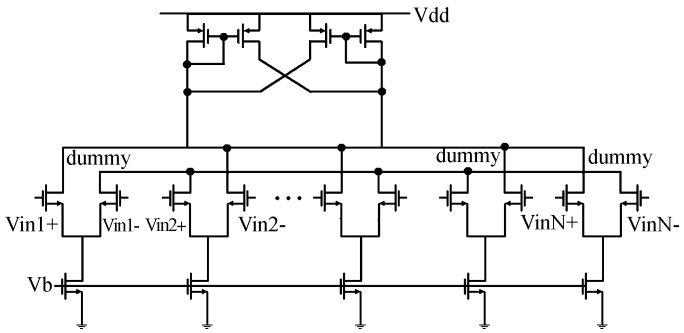


Fig. 3. Folding circuit.

resistive averaging can be obtained for capacitive averaging:

$$\frac{\Delta V_{\text{sampling}}}{\Delta V'_{\text{sampling}}} = \sqrt{1 + 4\left(\frac{C_{\text{av}}}{C_{\text{eq}}}\right) + 2\left(\frac{C_{\text{av}}}{C_{\text{eq}}}\right)^2}, \tag{6}$$

where $C_{\text{eq}} = \frac{C_{\text{H}}}{2} + \frac{\sqrt{C_{\text{H}}^2 + 4C_{\text{H}}C_{\text{av}}}}{2}$. From Eq. (6), better averaging is obtained as the ratio $C_{\text{av}}/C_{\text{H}}$ increases. However, a larger capacitor value can influence the input bandwidth of the T/H circuit. In the design, the ratio is set at about three.

3.2. Folding circuit

The folding circuit shown in Fig. 3 is realized by cross-coupled differential pairs. Cross-coupled PMOS load replaces conventional resistor load in this design. Three dummy differential pairs are added for good folding operation. Two of the dummy differential pairs are for the extension of the folding signals for the low and high side of the input range to allow interpolation in that region. The other is for dc balance. Because of the existence of the preamplifiers with a high gain in T/H circuits, the gain and the offset of the folding circuits do not have much influence on the accuracy of the ADC. Therefore, low tail current can be chosen.

Fed into the comparator, the analog differential output can be converted into digital output: logic "1" or "0". Therefore, the function of folding circuit is enlarged. Folding circuits are used in the coarse converter so that the binary code output can be directly obtained for the coarse converter. Moreover, folding circuits are used in the bit synchronization block to produce a digital bit synchronization signal to save comparators, which will be discussed later.

3.3. Bit synchronization

Bit synchronization signals are usually produced to define a wide range around the transition of the coarse output, where the output of the coarse and fine converters is synchronized. The proposed bit synchronization architecture employs folding circuits to produce digital bit synchronization signal and save comparators. Figure 4 shows its principle.

This is 3-bit synchronization. Sync1, sync2 and sync3 are digital bit synchronization signals produced by folding circuits. MSB′, (MSB-1)′ and (MSB-2)′ are the binary code outputs of the coarse sub-converter before bit synchronization. (MSB-3)′ is from the fine sub-converter. In the shaded regions,

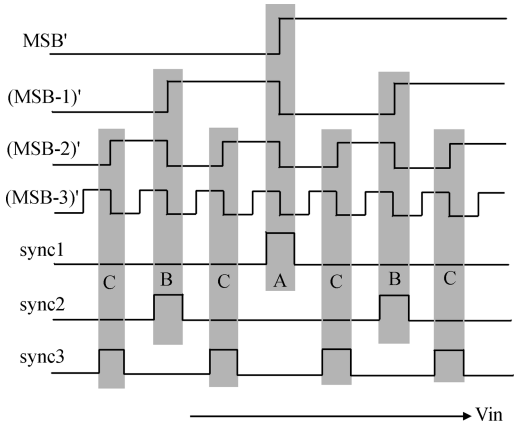


Fig. 4. Bit synchronization.

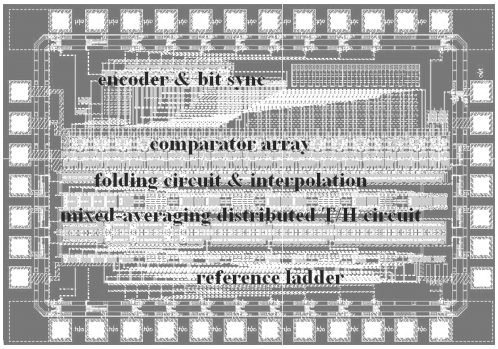


Fig. 5. Layout of the ADC.

the bit synchronization signal function and (MSB-3)′ are used to determine the final coarse output. The MSB, MSB-1 and MSB-2 after bit synchronization can be obtained with the following equations.

$$\text{MSB} = \text{sync1} \times \overline{(\text{MSB-3})'} + \overline{\text{sync1}} \times \text{MSB}', \tag{7}$$

$$\text{MSB-1} = \text{sync1} \times (\text{MSB-3})' + \text{sync2} \times \overline{(\text{MSB-3})'} + \overline{\text{sync1}} \times \overline{\text{sync2}} \times (\text{MSB-1})', \tag{8}$$

$$\text{MSB-2} = \text{sync1} \times (\text{MSB-3})' + \text{sync2} \times (\text{MSB-3}) + \text{sync3} \times \overline{(\text{MSB-3})'} + \overline{\text{sync1}} \times \overline{\text{sync2}} \times \overline{\text{sync3}} \times (\text{MSB-2})'. \tag{9}$$

It is obvious that the new bit synchronization idea needs only $2n$ comparators for n-bit synchronization and coarse conversion instead of the 3×2^n comparators of conventional methods.

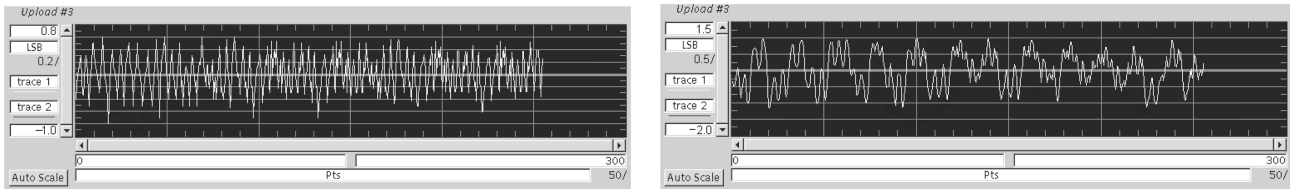
3.4. Other components

The ADC also includes a resistor ladder and an on-chip bandgap reference voltage generator to generate positive and negative reference voltage. A dynamic latched comparator[11] and a dynamic encoder[12] are adopted for low power.

4. Measured results

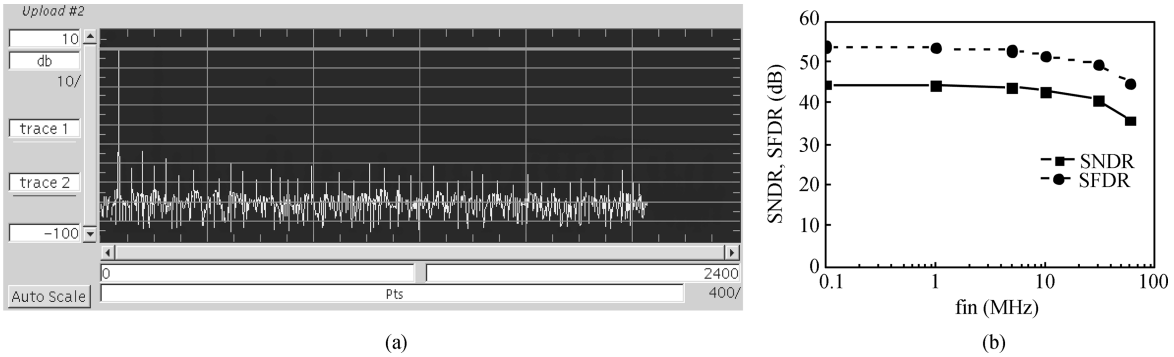
The described ADC was fabricated in 0.5 μm CMOS technology and occupies a die area of 2×1.5 mm^2. Figure 5 shows the layout of the ADC.

The chip was measured by an Agilent 93 k SOC test system. The maximum sampling rate is 125 MHz. The measured



(a) (b)

Fig. 6. (a) DNL; (b) INL.



(a) (b)

Fig. 7. (a) FFT spectrum; (b) Dynamic characteristic of the ADC.

Table 1. Performance summary.

Parameter	Value
Technology	0.5 μm CMOS
Supply voltage	5 V
Sampling rate	125 MHz
SNDR	44.3 dB (fin = 1 MHz) 40.8 dB (fin = 30 MHz)
SFDR	53.5 dB (fin = 1 MHz) 49.6 dB (fin = 30 MHz)
DNL	0.6 LSB/–0.8 LSB
INL	0.9 LSB/–1.2 LSB
Analog input range	1.5–3.5 V
Power dissipation	138 mW @ 125 MHz
Chip area	2×1.5 mm^2

Table 2. Performance comparison.

Parameter	This work	Ref. [13]	Ref. [14]	Ref. [15]	Ref. [16]
Process	0.5 μm CMOS	0.6 μm CMOS	0.5 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Resolution (bits)	8	8	8	8	8
Sampling rate (MHz)	125	150	100	200	250
Supply voltage (V)	5	3.3	5	3.3	1.8
Power (mW)	138	395	165	655	279
SNDR (dB)	44.3	43.7	42.3	44.3	43.2
ENOB (bits)	7.07	6.97	6.73	7.07	6.88
Power/Speed (mW/MHz)	1.104	2.633	1.650	3.275	1.116

DNL/INL with a slow full-scale ramp-wave input is 0.6 LSB/–0.8 LSB and 0.9 LSB/–1.2 LSB, as depicted in Fig. 6. The dynamic characteristic was measured by analyzing the fast Fourier transform of the output code with a sine-wave input. The SNDR is 44.3 dB, equivalent to 7.06 effective number of bits (ENOB) when the frequency of the input signal is about 1 MHz and 4096 sampling points are chosen. In this case, the SFDR is 53.5 dB and the FFT spectrum is plotted in Fig. 7(a). When the frequency of the input signal rises to 30 MHz, the SNDR reduces to 40.8 dB and the SFDR is 49.6 dB. The measured SNDR and SFDR versus the frequency of input sine-wave are shown in Fig. 7(b). According to the measured results, the current from digital parts is 4.1 mA and the current from analog parts is 23.4 mA at a sampling rate of 125

MHz. Therefore, the total power dissipation is calculated as about 138 mW. Table 1 summarizes the performance of the proposed ADC. Table 2 shows the performance comparison of this work and several previously reported 8-bit ADCs. The comparison shows that the proposed ADC performs better in terms of power, accuracy and the ratio of power and speed.

5. Conclusion

This paper describes an 8-bit low-power fully-folding CMOS ADC in 0.5 μm CMOS technology. A novel mixed-averaging distributed T/H circuit is proposed to improve the accuracy. Folding circuits are not only used in the fine converter but also in the coarse one and in the bit synchronization block to reduce the number of comparators for low power. A cyclic thermometer code replaces the common thermometer code and reduces the number of comparators by half. In the whole ADC, only 22 comparators are used. The measured results show that the proposed ADC performs better than some previously reported designs.

References

[1] Grift R, Rutten I, Veen M. An 8-bit video ADC incorporating folding and interpolation techniques. IEEE J Solid-State Circuits, 1987, 22(6): 944

[2] Nauta B, Venes A. A 70-MS/s 110-mW 8-b CMOS folding and interpolating A/D converter. IEEE J Solid-State Circuits, 1995, 30(12): 1302

[3] Venes A, Plassche R J. An 80-MHz, 80-mW, 8-b CMOS folding A/D converter with distributed track-and-hold preprocessing. IEEE J Solid-State Circuits, 1996, 3(12): 1846

[4] Liu Fei, Jia Song, Ji Lijiu, et al. A folding and interpolating A/D converter with master-slave T/H circuit. Chinese Journal of Semiconductors, 2004, 25(4): 462

[5] Chen Cheng, Wang Zhaogang, Ren Junyan, et al. 200 Ms/s 177 mW 8 bit folding and interpolating A/D converter. Chinese Journal of Semiconductors, 2004, 25(11): 1391

[6] Flynn M P, Sheahan B. A 400-Msample/s, 6-b CMOS folding and interpolating ADC. IEEE J Solid-State Circuits, 1998, 33(12): 1932

[7] Lin K L, Boom T, Stevanovic N, et al. A basic design guide for CMOS folding and interpolating A/D converters-overview and case study. The 6th IEEE International Conference on Electronics, Circuits and Systems, 1999, 1: 529

[8] Kattmann K, Barrow J. A technique for reducing differential non-linearity errors in flash A/D converters. IEEE International Solid-State Circuits Conference, 1991: 170

[9] Bult K, Buchwald A. An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2. IEEE J Solid-State Circuits, 1997, 32(12): 1887

[10] Scholtens P. A 2.5 volt 6 bit 600 MS/s flash ADC in 0.25 μm CMOS. Proceedings of the 26th European Solid-State Circuits Conference, 2000: 224

[11] Figueiredo P M, Vital J C. Kickback noise reduction techniques for CMOS latched comparators. IEEE Trans Circuits Syst II, 2006, 53(6): 541

[12] Liu Zhen, Jia Song, Zhang Xing, et al. Efficient encoding scheme for folding ADC. IEEE International Conference on Solid-State and Integrated Circuit Technology, 2008: 1988

[13] Wang Y T, Razavi B. An 8-b 150-MHz CMOS A/D converter. IEEE J Solid-State Circuits, 2000, 35(3): 308

[14] Choe M J, Song B S, Bacrania K. An 8-b 100-MSample/s CMOS pipelined folding ADC. IEEE J Solid-State Circuits, 2001, 36(2): 184

[15] Uyttenhove K, Vandenbussche J, Lauwers E, et al. Design techniques and implementation of an 8-bit 200-MS/s interpolating/averaging CMOS A/D converter. IEEE J Solid-State Circuits, 2003, 38(3): 483

[16] Oh T H, Lee H Y, Park H J, et al. A 1.8 V 8-bit 250 Msample/s Nyquist-rate CMOS pipelined ADC. IEEE International Symposium on Circuits and Systems, 2004, 1: I-9