An area-saving and high power efficiency charge pump built in a TFT-LCD driver IC*

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Abstract: An area-saving and high power efficiency charge pump is proposed, and methods for optimizing the operation frequency and improving the power efficiency are discussed. Through sharing coupling capacitors the proposed charge pump realizes two DC–DC functions in one circuit, which can generate both positive and negative high voltages. Due to sharing of the coupling capacitors, as compared with a previous charge pump designed by us for a TFT-LCD driver IC, the die area and the amounts of necessary external capacitors are reduced by 40% and 33%, respectively. Furthermore, the charge pump's power efficiency is improved by 8% as a result of employing the new topology. The designed circuit has been successfully applied in a one-chip TFT-LCD driver IC implemented in a 0.18 μm low/mid/high mixed-voltage CMOS process.

Key words: charge pump; area-saving; power efficiency; coupling capacitors; TFT-LCD driver IC
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1. Introduction

Built-in charge pump circuits are widely used in all kinds of VLSIs and SoCs to generate the desired voltages for internal circuit blocks. The output voltages of charge pumps are step-up or step-down or inverse voltages of the input power supply, which are obtained by transferring the charges of the input power supply to a capacitive load via the coupling capacitors, involving no amplifier or voltage regulator[1].

The one-chip TFT-LCD driver IC is a typical mixed-signal VLSI fabricated by a low/mid/high mixed-voltage CMOS process, in which a built-in charge pump is required to generate positive and negative high voltages to drive the TFT-LCD panel[2, 3]. A previous built-in charge pump[2, 3] for a TFT-LCD driver IC generated positive and negative high voltages through two separate circuits, which consumes excessive silicon area and requires more external coupling capacitors, so it is not suitable for area-saving layouts and more compact LCD modules (LCMs). Besides, power dissipation is increased as a result.

The charge pump circuit proposed in this paper can generate both positive and negative high voltages by combining the step-up and inversing functions through sharing coupling capacitors. Thus, the die area, the coupling capacitors and the power dissipation are all reduced.

In this paper, after introducing the topology of the previous built-in charge pump for a TFT-LCD driver IC, the proposed charge pump with novel topology is described. Then, the methods for optimizing operation frequency and improving power efficiency are discussed for the proposed circuit. Finally, the chip test results and the display image of the LCM using this chip are given, which illustrate the successful application of the proposed charge pump in a one-chip TFT-LCD driver IC.

2. Topology of the previous built-in charge pump

To drive the TFT-LCD panel, two positive and negative high voltages are needed, typical values of which are 16.50 V (V_{GH}) and –13.75 V (V_{GL}), respectively, but the input voltage (V_{IN}) of the charge pump circuit is as low as 5.5 V. Thus, the charge pump needs to generate three times the input voltage ($V_{GH} = 3V_{IN} = 16.50$ V) and –2.5 times the input voltage ($V_{GL} = -2.5V_{IN} = -13.75$ V).

The previous built-in charge pump circuit in a TFT-LCD driver IC is shown in Fig. 1. The circuits in Figs. 1(a) and 1(b) are used for generating the positive and negative high voltages, respectively. The switches are realized by high-voltage or mid-voltage analog CMOS switches according to the voltages they conducted (M represents mid-voltage analog CMOS switches, while H represents high-voltage ones), and $-V_{IN}$ is the inverse voltage of V_{IN} which is generated by other circuits.

Two phase non-overlap clocks for controlling the switches on and off are shown in Fig. 2.

When Φ_1 is high, switches a, b, c, d and h, i, j, k are on, and the coupling capacitors C_i ($i = 1 - 4$) are charged by input voltage V_{IN}; this phase is called the charging period.

When Φ_2 is high, switches e, f, g and l, m, n are on, V_{IN} drives charges from C_1 and C_2 to C_{OH}, and $-V_{IN}/2$ drives negative charges from C_3 and C_4 to C_{OL}. Thus the output voltage increases. This phase is called the step-up/inverse period.

After a number of charging and step-up/inverse periods, if the charge pumps enter their stable operating state, the theoretical output voltages for Figs. 1(a) and 1(b) are $V_{GH} = 3V_{IN}$

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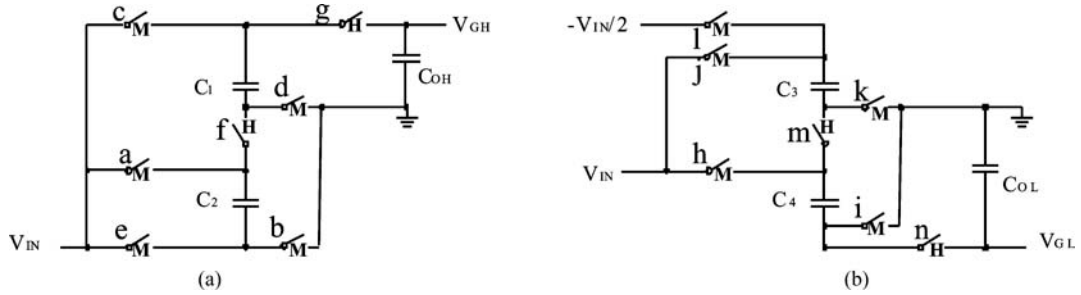

Fig. 1. Topology of previous built-in charge pump: (a) Step-up charge pump; (b) Inverse charge pump.

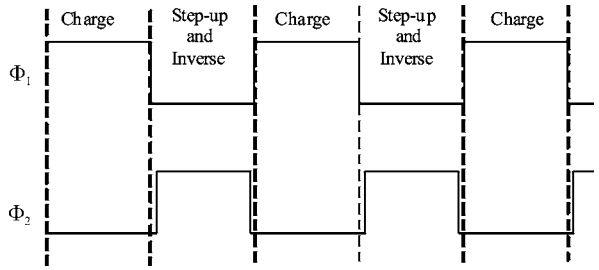

Fig. 2. Timing of two phase non-overlap clocks.

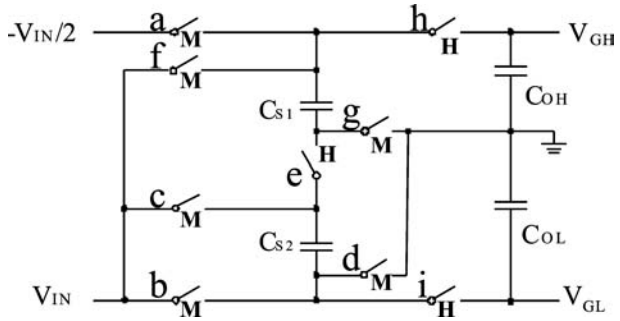

Fig. 3. Topology of the built-in charge pump proposed in this paper.

and $V_{GL} = -2.5V_{IN}$, respectively.

Usually, the charge pump circuit consumes considerable silicon area because of its large analog switches. It is known that, for a one-chip TFT-LCD driver IC, smaller die size means lower chip cost and higher market competitiveness. Besides, the LCM is more and more compact in portable applications, which requires reducing the chip external components on PCB. The built-in charge pump described above generates V_{GH} and V_{GL} independently through the separate circuits. It is found that, in Fig. 1 the whole charge pump employs 14 analog switches and 6 external capacitors, which need large silicon area and more external components. Moreover, the power dissipation is increased due to using more components.

3. Topology of the proposed charge pump

An improved topology of the built-in charge pump is shown in Fig. 3. The two coupling capacitors C_{S1} and C_{S2} are shared in order to generate positive and negative voltages simultaneously.

The timing of three phase non-overlap clocks (Φ_1–Φ_3) that execute the switching of the circuit is shown in Fig. 4. Φ_2 and Φ_3 are generated based on the reference clock Φ_1.

When Φ_1 is high, switches c, d, f and g are on, and the other switches are off, two coupling capacitors C_{S1} and C_{S2} are charged by V_{IN}. This is called the charging period.

When Φ_2 is high, switches b, e and h are on, and the others are off, V_{IN} drives positive charges moving from coupling capacitors C_{S1} and C_{S2} to load capacitor C_{OH}, thus the V_{GH} increases. This is called the step-up period.

When Φ_3 is high, switches a, e and i are on, and the others are off, $-V_{IN}$ drives negative charges moving from C_{S1} and C_{S2} to load capacitor C_{OL}, thus the V_{GL} increases in negative polarity. This is called the inverse period

As shown in Fig. 4, the timing of the step-up and inverse charge pump is as follows: charging period → step-up period → charging period → inverse period → charging period →. This is one cycle of the whole charge pump timing.

After a number of charging, step-up and inverse periods, if the charge pumps enter their stable state, their theoretical output voltages are $V_{GH} = 3V_{IN}$ and $V_{GL} = -2.5V_{IN}$, respectively.

Therefore, through sharing the coupling capacitors C_{S1} and C_{S2}, the proposed charge pump in Fig. 3 can generate positive and negative high voltages simultaneously, combining the two function blocks of Figs. 1(a) and 1(b). The whole circuit employs only 9 analog switches and 4 external capacitors. Compared with the topology shown in Fig. 1, the layout area is reduced by almost 40% and the number of external capacitors is reduced by 33%. Moreover, by reducing the number of the circuit components the power dissipation is decreased.

4. Optimizing the operation frequency

The operation frequency of a charge pump is a very important factor because it is related to many features of the charge pump, such as DC–DC conversion efficiency, output voltage ripple, settling time and so on. In this section, the optimizing operation frequency for the proposed charge-pump is discussed through analysis of the charging and step-up/inverse periods.

Before the analysis, several issues must be addressed: (1) $R_{on,\,mid}$ and $R_{on,\,high}$ refers to the on-resistances of mid-voltage and high-voltage analog CMOS switches, respectively; (2) the parasitic capacitances and resistances are neglected; (3) the non-overlap period of the clocks is too short to be considered; (4) the charge balance time is neglected; (5) T refers to Φ_1's period.

The equivalent circuits of the charge pump in different periods[4] are shown in Fig. 5. The output voltages are V_{GH} =

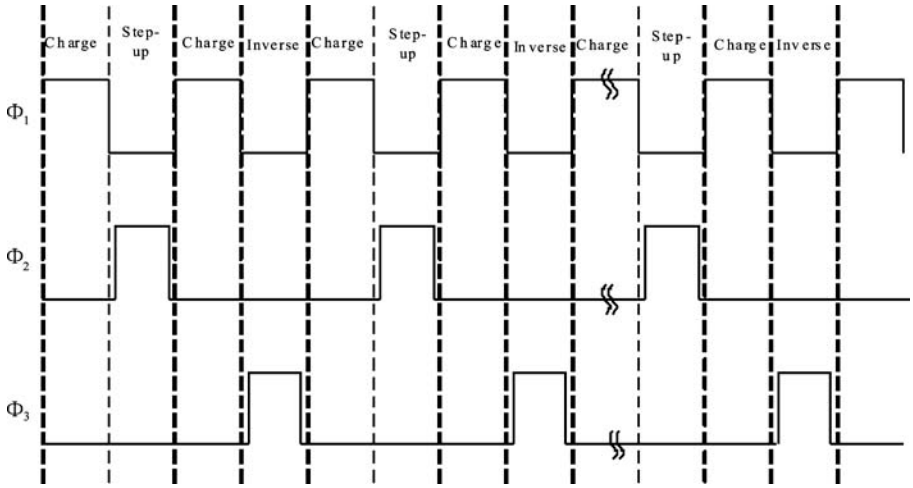

Fig. 4. Timing of three phase non-overlap clocks.

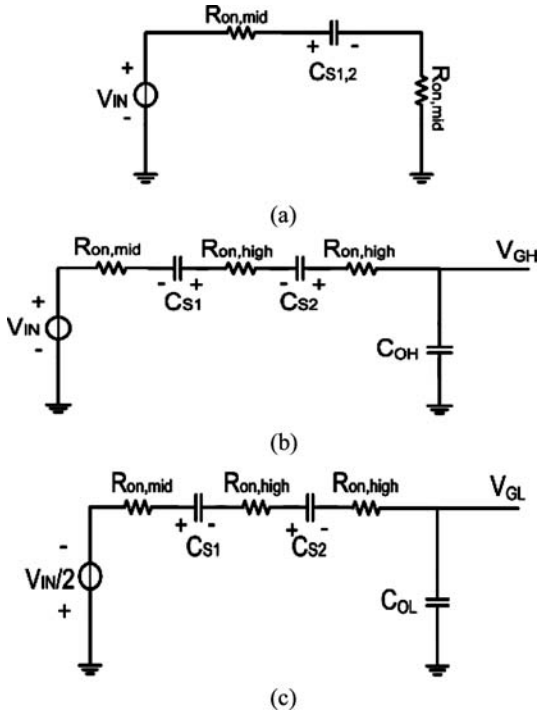

Fig. 5. Equivalent circuits of the charge pump in different periods: (a) Charging period; (b) Step-up period; (c) Inverse period.

$3V_{IN}$ and $V_{GL} = -2.5V_{IN}$.

4.1. Charging period

In Fig. 5 (a), assuming that there is no charge on $C_S(C_{S1} = C_{S2} = C_S)$ at $t = 0$, then the voltage $V_{CS}(t)$ across C_S can be expressed as[5]

$$V_{CS}(t) = V_{IN}(1 - e^{-t/\tau}), \quad t > 0, \tag{1}$$

where $\tau = 2R_{on,mid}C_S$. When $t \geqslant 5\tau$, $V_{CS}(t)$ reaches nearly 0.99 times V_{IN}, namely

$$V_{CS}(5\tau) \geqslant 0.99V_{IN}. \tag{2}$$

In this time we consider C_S to be fully charged; here, $t \geqslant 5\tau$ indicates $(T/2) \geqslant 5\tau$, namely

$$f \leqslant \frac{1}{20R_{on,mid}C_S}. \tag{3}$$

4.2. Step-up/inverse period

Only the step-up period is analyzed in this section; the inverse period can be analyzed in the same way.

Assuming that there is a constant load current I_L connected to the output of the charge pump, we can find the following relation for the kth step-up period by the charge balance principle:

$$\begin{aligned} &2V_{CS}(T/2)C_S + V_{GH}(k-1)C_{OH} - 2TI_L \\ &\quad = V_{GH}(k)C_{OH} + (V_{GH}(k) - V_{IN})C_S, \end{aligned} \tag{4}$$

where $V_{GH}(k-1)$ and $V_{GH}(k)$ are the output voltages in the $(k-1)$th and kth period, respectively.

According to Eq. (4), we can get the output voltage $V_{GH}(k)$:

$$V_{GH}(k) = \frac{[V_{IN} + 2V_{CS}(T/2)]C_S/C_{OH} + V_{GH}(k-1) - 2TI_L/C_{OH}}{1 + C_S/C_{OH}}. \tag{5}$$

Let $V_{GH}(k) = V_{GH}(k-1)$; the charge pump obtains its stable output voltage $V_{stable1}$,

$$V_{stable1} = V_{IN} + 2V_{CS}(T/2) - 2TI_L/C_S. \tag{6}$$

If Equation (3) is satisfied, for $I_L = 0$, $V_{stable1}$ approaches $3V_{IN}$. So, it can be considered that, since the load current derives charges from the capacitors, the output voltage of the charge pump is less than $3V_{IN}$ if the load is added.

Another factor that influences the stable output voltage is the voltage drop on the switches, so we can write the actual output voltage V_{stable} as[6]

$$V_{stable} = V_{IN} + 2V_{CS}(T/2) - 2TI_L/C_S - I_L(R_{on,mid} + 2R_{on,high}). \tag{7}$$

4.2.1. DC–DC conversion efficiency η

Only when Equation (3) is satisfied, the DC–DC conversion efficiency η can be calculated as

$$\eta = \frac{V_{stable}}{3V_{IN}} = 1 - \frac{2I_L/C_S}{3fV_{IN}} - \frac{I_L(R_{on,mid} + 2R_{on,high})}{3V_{IN}}. \tag{8}$$

It must be noted that if Equation (3) is not satisfied, there will be an additional voltage loss in V_{stable} shown in Eq. (7), as well as an additional decrease in η shown in Eq. (8).

4.2.2. Output voltage rise time t_{rise}

Given that $V_{\text{GH}}(0) = 0$, $V_{\text{GH}}(k)$ can be expressed as

$$V_{\text{GH}}(k) = \frac{3V_{\text{IN}}C_{\text{S}} - 2TI_{\text{L}}}{C_{\text{OH}}}\left[1 - \frac{1}{(1 + C_{\text{S}}/C_{\text{OH}})^k}\right]. \quad (9)$$

It is known that the output voltage rise time t_{rise} is defined as the time consumed before the charge pump's output voltage reaches V_{SP} (specified output voltage level that is lower than V_{stable}), so

$$t_{\text{rise}} = k_{\text{rise}} \times 2T, \quad (10)$$

where k_{rise} is a integer and should satisfy

$$V_{\text{GH}}(k_{\text{rise}}) = V_{\text{SP}}.$$

so $t_{\text{rise}} =$

$$(2/f)\left\{\frac{-\ln\left[1 - \dfrac{V_{\text{SP}}}{3V_{\text{IN}}C_{\text{S}}/C_{\text{OH}} - (2/f)I_{\text{L}}/C_{\text{OH}}}\right]}{\ln(1 + C_{\text{S}}/C_{\text{OH}})}\right\}_{\text{INTEGER}}. \quad (11)$$

4.2.3. Output voltage ripple ΔV

The charge pump is designed to execute a step-up operation every two periods (referring to Φ_1's period T). In the charging and inverse periods, the load current I_{L} derives charges from C_{OH} and causes a ripple upon the output voltage V_{GH}. The amplitude of the output voltage ripple ΔV can be calculated as[7]

$$\Delta V = \frac{I_{\text{L}}(3/2)T}{C_{\text{OH}}} = \frac{3I_{\text{L}}}{2fC_{\text{OH}}}. \quad (12)$$

If C_{S} and C_{OH} have a certain value, from Eqs. (8), (11) and (12), we could draw the simple conclusion that a higher operation frequency f leads to a higher DC–DC conversion efficiency, a shorter rising time and a smaller output voltage ripple. Obviously, higher f benefits the charge pump's performance, but according to Eq.(3), if $f > 1/(20R_{\text{on, mid}}C_{\text{S}})$, the coupling capacitor C_{S} cannot be fully charged, which will lead to a worse DC–DC conversion efficiency. So we choose f as

$$f = \frac{1}{20R_{\text{on, mid}}C_{\text{S}}}. \quad (13)$$

In practice, C_{S} is usually set to be 1 μF, and $R_{\text{on, mid}}$ is calculated to be 3.6 Ω according to the analog switch size and the process model. Based on Eq. (13), the appropriate f is chosen to be $f_{\text{opt}} = 15$ kHz. To verify the above calculation results, a simulation for DC-DC conversion efficiency is implemented at the frequency range of 3.3 to 50 kHz, which is shown in Fig. 6. It is clear that the DC-DC conversion efficiency is optimum at

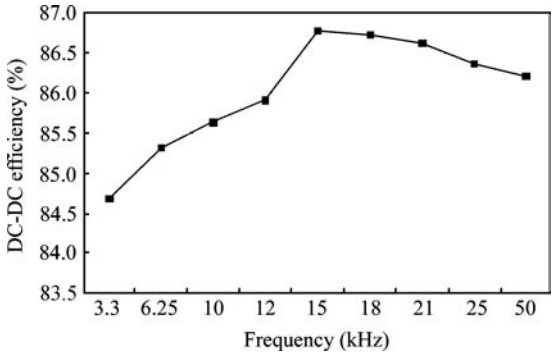

Fig. 6. DC–DC conversion efficiency for different frequencies (V_{GH}).

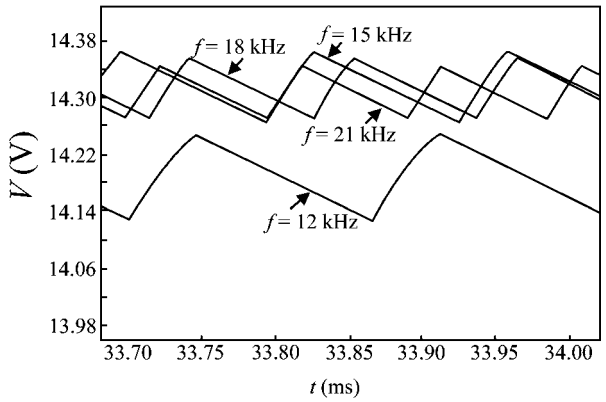

Fig. 7. Output voltage waves of V_{GH} for different operation frequencies.

$f = 15$ kHz. The output voltage waves of V_{GH} at different frequencies are simulated as shown in Fig. 7. It can be seen that for higher frequency the output voltage ripple is smaller. It is found that the DC-DC efficiency decreases slowly when the operation frequency is higher than 15 kHz. Therefore, a frequency higher than 15 kHz is sometimes acceptable for obtaining a more stable output voltage at the cost of a small reduction of DC–DC efficiency. It should be pointed out that all the simulations in this paper are implemented under the 0.18 μm low/mid/high voltage CMOS process, and with a total current load of 2 mA for V_{GH} and 1 mA for V_{GL}, unless otherwise specified.

5. Improvement of power efficiency

In this section, the method for improving power efficiency is discussed. The corresponding simulation and calculation are implemented at the optimized operation frequency of $f = 15$ kHz.

Power dissipation P_{d} of the charge pump is caused by two factors[1]. Firstly, the analog switches exhibit on-resistance when conducting current, which causes power dissipation P_{r}. Secondly, because the transistors used in analog switches are usually with large sizes, so as to conduct load current, the large parasitic capacitances of transistors are periodically charged and discharged, then the power dissipation P_{c} caused by parasitic capacitances occurs. So the total power dissipation P_{d} can be expressed as

$$P_{\text{d}} = P_{\text{r}} + P_{\text{c}}. \quad (14)$$

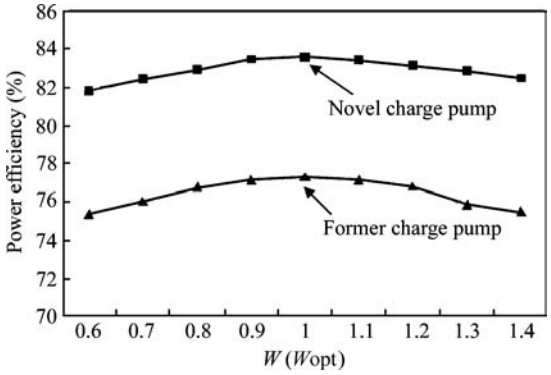

Fig. 8. Power efficiencies for different sized switches.

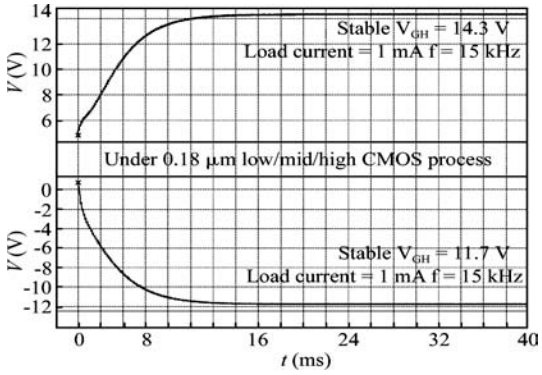

Fig. 9. Simulation results for the start-up of output voltages.

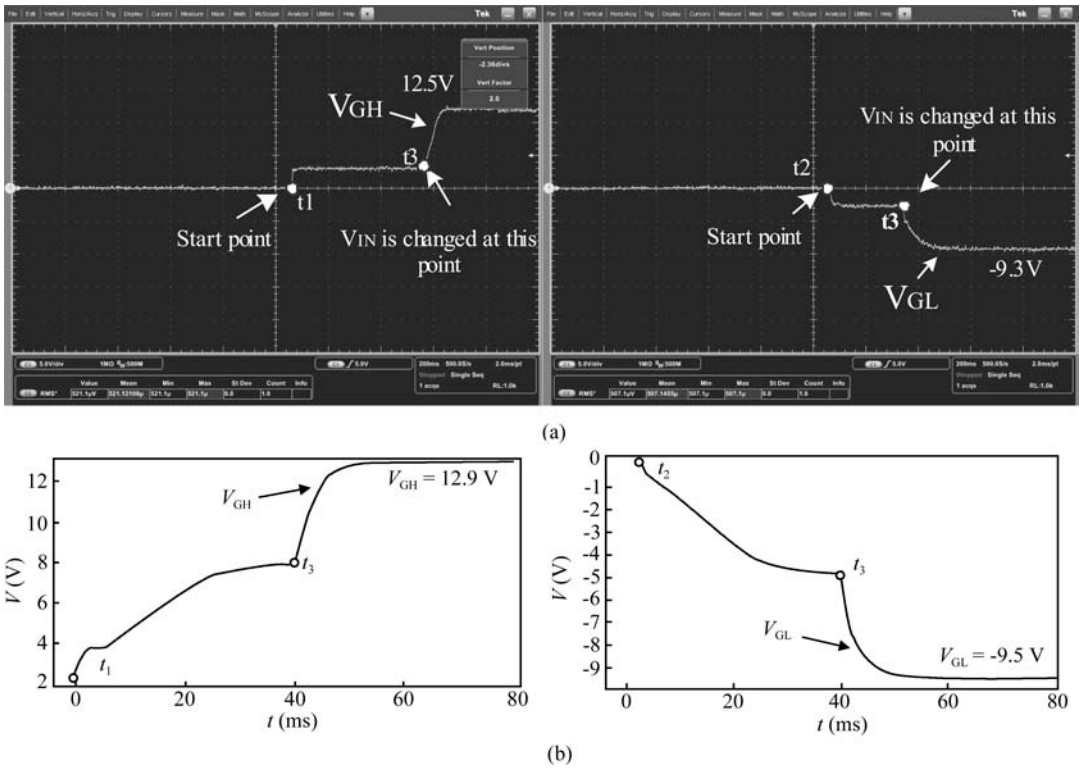

Fig. 10. (a) Measured and (b) simulated results for V_{GH} and V_{GL}.

If the total input power is P_{tot}, power efficiency E_P can be written as

$$E_P = 1 - P_d/P_{tot}. \tag{15}$$

The optimization of power efficiency is implemented on the size W of the analog switch transistors. A larger W leads to a smaller on-resistance and therefore P_r decreases, namely $\partial P_r/\partial W < 0$. However, larger W means larger parasitic capacitances, and thus P_c increases, namely $\partial P_c/\partial W > 0$. So, an appropriate W ($W = W_{OPT}$) exists to give

$$\left.\frac{\partial P_d}{\partial W}\right|_{W=W_{OPT}} = \left.\frac{\partial P_r}{\partial W}\right|_{W=W_{OPT}} + \left.\frac{\partial P_c}{\partial W}\right|_{W=W_{OPT}} = 0. \tag{16}$$

If Equation (16) is satisfied, P_d will reach its smallest value, and the power efficiency E_P of the charge-pump is optimized.

The power efficiencies of the proposed and previous charge pump circuits are shown in Fig. 8 for different sizes of W. It is obvious that at $W = W_{OPT}$ the power efficiencies are largest for both circuits; moreover the proposed charge pump circuit has a better power efficiency than the former one. The largest power efficiency of the proposed circuit is 83.59% while that of the former circuit is 77.31%; the power efficiency is improved by 8%.

6. Simulation and test results

The proposed charge-pump circuit is designed and simulated under a 0.18 μm low/mid/high CMOS process. The simulation results for the start-up of output voltages V_{GH} and V_{GL} are shown in Fig. 9, where $V_{IN} = 5.5$ V, load current $I_L = 1$ mA, operation frequency $f = 15$ kHz. It can be seen that it takes no more than 20 ms for the circuit to reach its stable output voltages, and the DC–DC conversion efficiencies are 86.7% and 85.1% for V_{GH} and V_{GL}, respectively.

The designed charge-pump circuit is built in a one-chip TFT-LCD driver IC developed by us; the chip measurement results for V_{GH} and V_{GL} are shown in Fig. 10(a). In order to compare with the chip measurement results, the designed charge-

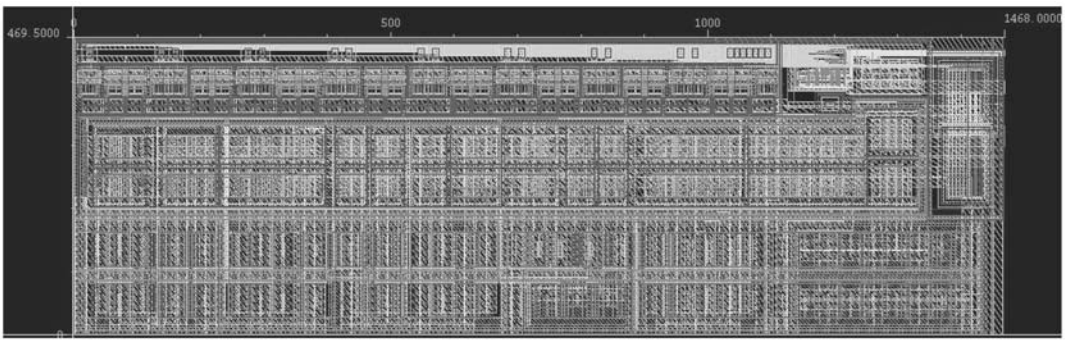

Fig. 11. Layout of the proposed charge-pump circuit.

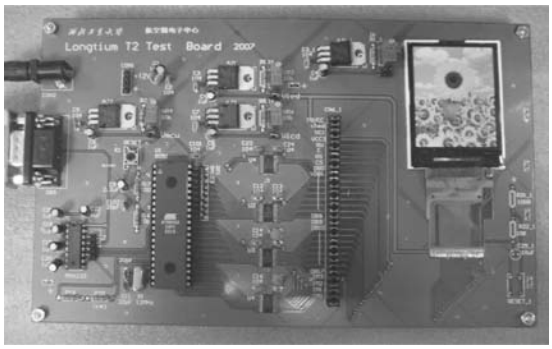

Fig. 12. Photo of the LCD module using the proposed charge pump circuit.

pump circuit is also simulated following the chip start-up sequence; the simulated results are shown in Fig. 10(b), where V_{IN} = 4.5 V, load current I_L = 1 mA, operation frequency f = 15 kHz. For the built-in charge-pump circuit, since V_{IN} is generated by a voltage-doubler, it is not equal to 5.5 V, but is nearly 4.5 V, so V_{IN} = 4.5 V is used in the above simulation.

For the proposed charge-pump built in a one-chip TFT-LCD driver IC, due to its input voltage V_{IN} being generated by other charge-pump, when the power is on V_{IN} is not at a stable value. In order to lighten the load of V_{IN} when the power is on, the external power supply V_{DD} (2.5–3 V) is applied to the proposed charge-pump instead of V_{IN}, until V_{IN} is stable.

In Fig. 10(a), t_1 and t_2 are the power-on time points for V_{GH} and V_{GL}, from t_1 (t_2) to t_3, the proposed charge-pump is driven by the external power supply V_{DD}, and at point t_3 the input voltage of the proposed charge-pump is switched to V_{IN}.

For the measured voltages V_{GH} and V_{GL} shown in Fig. 10(a), the stable values are less than the simulated values. These voltage differences are mainly ascribed to the differences in load current I_L for both situations, because the real load current in the chip test cannot be estimated accurately.

The layout of the proposed charge-pump circuit is shown in Fig. 11. It consumes a die area of 1468 × 470 μm^2, which is only 60% of the former charge pump circuit.

The proposed charge pump circuit has been successfully applied in a one-chip TFT-LCD driver IC implemented in a 0.18 μm low/mid/high mixed-voltage CMOS process. Figure 12 is a photo of the LCD module using this one-chip TFT-LCD driver IC.

7. Conclusion

An area/cost-saving and high-power efficiency charge pump is proposed. Through sharing coupling capacitors, the charge pump combines step-up and inversing functions in one circuit. Due to this new topology, the layout area, the number of external capacitors and the power dissipation are all reduced compared with the traditional circuit. Methods for optimizing operation frequency and improving power efficiency are given.

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