Design and fabrication of a planar patch-clamp substrate using a silicon-on-insulator wafer

Zhang Zhenlong(张振龙), Liu Xiangyang(刘向阳), and Mao Yanli(毛艳丽)†

(Institute of Optics and Photoelectronic Technology, School of Physics and Electronics, Henan University, Kaifeng 475004, China)

Abstract: The planar patch-clamp technique has been applied to high throughput screening in drug discovery. The key feature of this technique is the fabrication of a planar patch-clamp substrate using appropriate materials. In this study, a planar patch-clamp substrate was designed and fabricated using a silicon-on-insulator (SOI) wafer. The access resistance and capacitance of SOI-based planar patch-clamp substrates are smaller than those of bulk silicon-based planar substrates, which will reduce the distributed RC noise.

Key words: planar patch-clamp substrate; silicon-on-insulator; access resistance; capacitance
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1. Introduction

Ion channels are transmembrane pores which allow the passage of ions into and out of a cell down the electrochemical gradient, which play key roles in many cellular processes[1, 2]. There are many distinct dysfunctions known as channelopathies caused by ion channel mutations[3]. Therefore the investigation of ion channels is of great significance for understanding how they work and for drug discovery of channelopathies.

The pipette patch-clamp technique has proven to be a powerful technique for the investigation of fundamental ion channel biophysics and for drug discovery[4, 5]. This technique allows one to monitor the gating of ion channels under defined conditions and enables the coupling of functional and molecular studies on ion channels at the single cell level[6]. However, this technique has some weaknesses, such as the requirement of precise micromanipulation and a skilful experimenter, and the fact that the electrode is an individual glass pipette, which are not suitable for application to high-throughput screening[7, 8]. Recently a planar patch-clamp method has attracted increasing attention, because it has some advantages compared with the pipette patch-clamp method, such as the miniaturization and parallelization of the planar substrates and the ability to combine with other physical probes[9, 10].

Many materials have been used for planar patch-clamp substrate fabrication, such as glass[11], Si[12–14], quartz[15] and PDMS[16]. It has been considered for Si that the background noise current is large due to the high density of free charge carriers in the substrate. However, we have recently demonstrated that the noise current can be significantly reduced by using a silicon-on-insulator (SOI) substrate[17]. There are several other advantages to using an SOI substrate: (1) the structure of the micropore through the substrate can be precisely controlled by using the large etching rate difference between Si and SiO_2 in both plasma and wet etching, and (2) it is possible to produce significantly miniaturized devices by integrating the biosensor and Si electronic circuits of the preamplifier into the same SOI substrate.

In this study, we design and fabricate a planar patch-clamp substrate using an SOI wafer. The access resistance and capacitance of the SOI-based planar patch-clamp substrate are smaller than those made with a bulk silicon wafer due to the special structure of the SOI wafer. Therefore the noise current in the experiments must be smaller because the small access resistance and capacitance induce small current noise[18].

2. Experimental

An N-type SOI substrate (50–75 Ω·cm resistivity with about 600 μm total thickness) with 2.5 μm top Si layer and 3 μm buried SiO_2 layer was cut to a square of size 7 × 7 mm^2 after the formation of the micropore. The backside thick Si layer was etched by 8% tetramethylammonium hydroxide (TMAH, Wako), and the buried SiO_2 layer was etched by 10% solution of HF (Steller Chemifa, Japan).

The intracellular solution in the cell experiments contains (in mM): 140 KCl, 5 EGTA, 10 HEPES, pH 7.4 (with KOH). The extracellular solution contains (in mM): 140 NaCl, 5 KCl, 2 $MgCl_2$, 2 $CaCl_2$, 10 Glucose, 10 HEPES, pH 7.4 (with NaOH). All the chemicals were purchased from Sigma-Aldrich, of analytical grade, and used without further purification. Water with a typical resistivity of 18.2 MΩ·cm was produced with Milli-Q purification (Millipore Ltd.).

The access resistance and capacitance of the substrate were measured with an Axopatch 200B Amplifier (Axon Instruments) and a Digidata 1322A interface (Axon Instruments) connected to a computer. The results were acquired using the pClamp 9.0 program (Axon) at 500 Hz.

† Corresponding author. Email: myl3000@163.com
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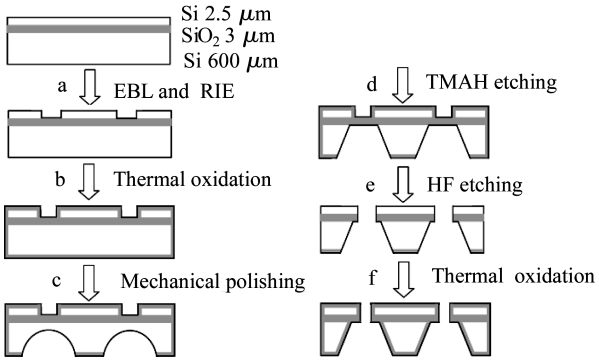

Fig. 1. Procedures of SOI-based planar patch-clamp substrate fabrication using EBL and RIE.

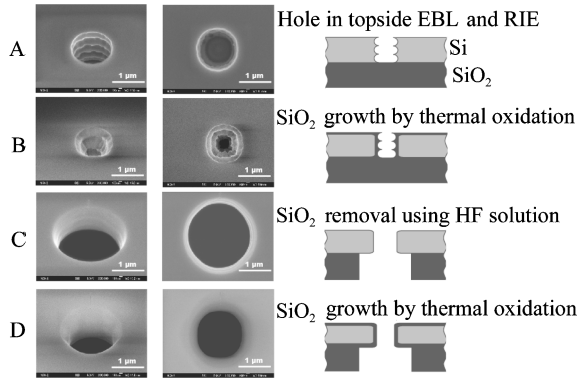

Fig. 2. SEM images of a single pore and the schematic of the pore wall after the processes a, b, e and f shown in Fig. 1, respectively. SEM images in the left and middle panels are the oblique view and top view of the same pore. The light-gray and dark-gray layers in the illustrations represent Si and SiO_2, respectively.

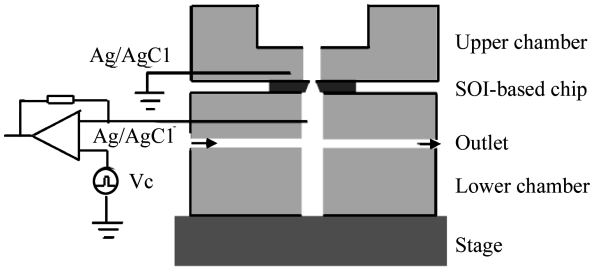

Fig. 3. Setup for the measurement of access resistance and capacitance of the substrate.

3. Results and discussion

3.1. Design and fabrication of the planar patch-clamp substrate

Figure 1 shows the through-pore fabrication procedures in an SOI wafer using electron beam lithography (EBL) and reactive ion etching (RIE). Firstly circular patterns were made in the substrate with the EBL and RIE techniques (Fig. 1(a)). Then a SiO_2 layer of 1 μm thickness was grown at 900 °C with thermal oxidation in which O_2 bubbled water vapor at 95 °C was used as the reactive gas (Fig. 1(b)). This thermally formed SiO_2 layer is for protecting the top surface of the substrate in the subsequent tetramethylammonium hydroxide (TMAH) etching process. Then large holes were made by 1 mm diameter diamond drill polishing the backside of the substrate (Fig. 1(c)), followed by 8% (v/v) TMAH etching at 90 °C to the buried SiO_2 layer (Fig. 1(d)). Finally the buried SiO_2 layer at the bottom of the pattern was removed with 10% (v/v) HF solution from the topside of the substrate (Fig. 1(e)), followed by 1 μm thick SiO_2 layer formation at 900 °C with thermal oxidation in the presence of O_2 bubbled water vapor at 95 °C (Fig. 1(f)). This thermal SiO_2 layer is for decreasing the capacitance of the substrate and reducing the pore diameter. Figure 2 shows the SEM images of a single pore and the schematic of the pore wall after the processes a, b, e and f shown in Fig. 1, respectively. From the SEM of the substrate, the final diameter of the pore is about 1 μm. In the present study, substrates with diameters of 1–2 μm were fabricated, which were demonstrated to be suitable for high seal resistance formation and ion-channel current measurement[11, 15, 16].

3.2. Electrical properties of the SOI-based planar patch-clamp substrate

Ion channel current recording needs sufficient signal intensity compared with the background noise. In the pipette patch-clamp experiment, the background noise is generated from many sources, such as the amplifier, cell membrane, glass-membrane seal, pipette, pipette holder and interactions between all of them[5]. In the planar patch-clamp experiment, the microstructured substrate replaces the pipette holder and glass pipette in the pipette patch-clamp experiment. From the viewpoint of reducing the background noise, it is required that the access resistance and the capacitance of the fabricated substrate be small, because small access resistance and capacitance produce small distributed RC noise[18].

The access resistance of the planar substrate is dominated by the conductance of the electrolyte in the pore because the area of the pore is very small compared with the rest of the conducting path[13]. Therefore the access resistance can be evaluated by only taking into account the resistance of the solution in the pore, which is given by

$$R_{\mathrm{a}} = \frac{\rho l_{\mathrm{p}}}{A} \tag{1}$$

with access resistance R_{a}, resistivity of the solution ρ, cross-sectional area of the pore A, and length of the pore l_{p}.

The access resistance and capacitance of the substrate were measured with the setup shown in Fig. 3. The SOI-based substrate was sandwiched between the upper chamber and the lower chamber. The Ag/AgCl electrodes were inserted in the upper and lower chambers. In our experiments, the diameter of the pore is between 1 and 2 μm, and the access resistance was measured to be 0.5–2.3 MΩ with bath solution in the upper chamber and pipette solution in the lower chamber. Figure 4 shows the variation of the access resistance with pore diameter.

The capacitance of the substrate can be evaluated by

$$C = \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \frac{1}{C_4} + \frac{1}{C_5}\right)^{-1}, \tag{2}$$

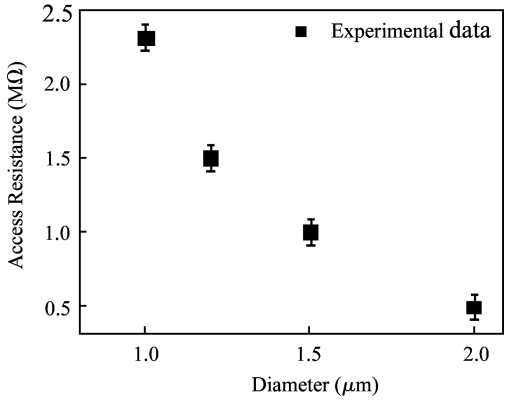

Fig. 4. Variation of access resistance with pore diameter.

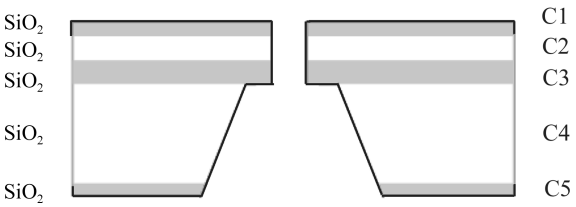

Fig. 5. Schematic cross section of the SOI-based substrate.

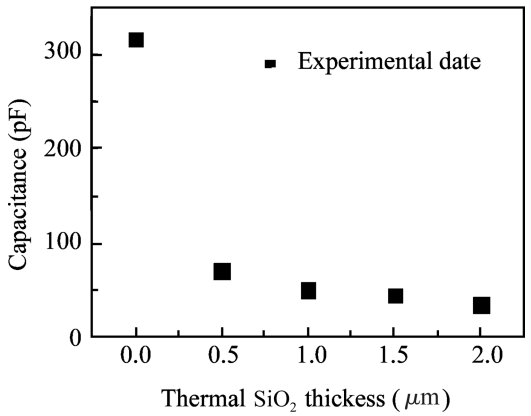

Fig. 6. Variation of substrate capacitance with thermal SiO_2 layer thickness.

$$C_{\rm i} = \varepsilon_0 \varepsilon_{\rm r} \frac{S_{\rm i}}{d_{\rm i}}, \tag{3}$$

where C stands for the total capacitance of the substrate, $C_{\rm i}$ for the capacitance of the SiO_2 or silicon layer (Fig. 5), ε_0 for the dielectric constant of free space, $\varepsilon_{\rm r}$ for the relative dielectric constant of dielectric material, $S_{\rm i}$ for the fluid contact area, and $d_{\rm i}$ for the thickness of the material. The capacitance of the substrate can be decreased by increasing the thickness of the SiO_2 layer due to the smaller relative dielectric constant. Figure 6 shows the variation of the substrate capacitance with the thermal SiO_2 layer thickness. The capacitance with the value of 35 pF was obtained with the formation of the 2 μm SiO_2 layer.

3.3. Discussion

It has been considered that the silicon wafer induces a large capacitance due to the high density of free charge carriers in silicon[10]. This large capacitance is the main disadvantage to making a planar patch-clamp substrate because the current noise increases with capacitance[18]. Table 1 shows a comparison of the SOI-based and bulk silicon-based substrates. The capacitance of the SOI-based substrate fabricated with 35 pF in this study was obtained by the formation of a 2 μm thick thermal SiO_2 layer. This value is less than those reported in the literature for bulk silicon-based substrates such as 54 pF[12] and 50 pF[19]. It is expected that the capacitance of the SOI substrate could be decreased by reducing the fluidic contact area using a microfluidic system, and/or increasing the thickness of the buried SiO_2 layer. For example, the thickness of the buried SiO_2 could be increased to 10 μm from 2.5 μm used in this study. It is more difficult to obtain such a thick SiO_2 layer for a bulk silicon wafer. Moreover, in order to reduce the capacitance, thermal oxidation or plasma-enhanced chemical vapor deposition (PECVD) was adopted to form the SiO_2 layer on the substrate after the pore was formed[12–14], which changed the shape of the pore[13] or the roughness of the substrate surface[12]. In the case of the SOI substrate, the thickness of the buried SiO_2 layer and the thermal layer could be decided before making the pore with FIB, thus the original surface condition and the pore shape could remain.

Table 1. Comparison of the SOI-based and bulk silicon-based substrates.

Parameter	SOI-based substrate (ϕ 1–2 μm)	Bulk silicon-based substrate (ϕ 1–2 μm)
Access resistance (MΩ)	0.5–2.3	3–10[13, 14]
Capacitance (pF)	Minimum: 35	Minimum: 50[19]

Another important parameter of the substrate is the access resistance, because smaller access resistance produces smaller current noise[18]. The thickness of the layer containing the pore could be precisely controlled to be about 5.5 μm in this study because TMAH etching stops at the buried SiO_2 layer of the SOI wafer, therefore the access resistances of the substrates are small and distribute in a narrow range (shown in Table 1). For bulk silicon wafer, the thickness of the layer containing the pore was carefully controlled to be 20–40 μm; thus the access resistances of the substrates were large and distributed in a wide range[13, 14].

4. Conclusion

In this work, a planar patch-clamp substrate was designed and fabricated using an SOI wafer, and the access resistance and capacitance were measured. The values of the access resistance and capacitance are smaller compared with the reported values of a bulk silicon-based substrate due to the special structure of SOI. It is asserted that this reduces the current noise in the measurement of ion channel current.

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