A low cost integrated transceiver for mobile UHF passive RFID reader applications*

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Abstract: A low cost integrated transceiver for mobile UHF passive RFID reader applications is implemented in a 0.18-μm CMOS process. The transceiver contains an OOK modulator and a power amplifier in the transmitter chain, an IQ direct-down converter, variable-gain amplifiers, channel-select filters and a 10-bit ADC in the receiver chain. The measured output P_{1dB} power of the transmitter is 17.6 dBm and the measured receiver sensitivity is –70 dBm. The on-chip integer N synthesizer achieves a frequency resolution of 200 kHz with a phase noise of –104 dBc/Hz at 100 kHz frequency offset and –120.83 dBc/Hz at 1 MHz frequency offset. The transmitter, the receiver and the frequency synthesizer consume 201.34, 25.3 and 54 mW, respectively. The chip has a die area of 4×2.5 mm^2 including pads.

Key words: UHF RFID; reader; single chip; transceiver
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1. Introduction

Radio frequency identification (RFID) is a wireless communication technology in which a reader captures data encoded in tags using radio waves. Due to numerous advantages, RFID has received great attention all over the world in automatic identification procedures such as manufacturing, logistics, and retail[1]. Different frequencies can be used in RFID systems. Nowadays, near-field inductive coupled RFID systems which operate in low frequency (LF) and high frequency (HF) are fully studied. Due to the requirements of higher data rate and longer read range, a technology using passive RFID tags operating in the UHF band is gaining worldwide attention[2]. Currently many different UHF RFID products are available in the market to meet different demands. The key barrier to UHF RFID development is its cost (both for the tag and the reader), so significant academic and corporate resources are being directed toward the development of low cost chips for RFID applications. Compared with tag chips, the development of low cost front-end, baseband or complete solutions for UHF RFID reader transceivers is more challenging.

Many RFID systems are equipped with stationary readers, and only cover a fixed local area. In many cases, it is expected that the reader could be mobile and hand-held. This paper presents a low-cost passive UHF RFID reader solution for near-field mobile applications.

2. System design considerations and transceiver architecture

A typical UHF RFID system consists of a reader and several passive tags. The communication between the reader and the tags is half duplex (Fig. 1), and the forward data transfer (from the reader to the tags) utilizes the ASK modulation scheme while the return data transfer (from the tags to the reader) utilizes the back-scattered modulation scheme[3].

Since the data from the tags to the reader is transferred by reflecting the reader's continuous-wave (CW) signal, it is very convenient for the reader to use direct-conversion architecture due to high integration level and low power consumption. The passive tag that restores energy from the CW signal should be as simple as possible. The non-coherent demodulation of the tag requires that the forward data transfer from the reader to the tags utilizes the ASK modulation scheme. PA should be integrated for convenient use in mobile devices. Considering the cost of the chip and the battery lifetime of mobile devices, OOK modulators and high-efficient non-linear PAs can be used in mobile RFID readers for some applications which do not have strict spectral mask requirements.

The presented transceiver architecture is shown in Fig. 2. It consists of a frequency synthesizer, an I/Q direct-conversion mixer, a VGA, an OOK modulator and a power amplifier. Only one of the ADC used in TDD (time division duplex) mode is included in this IC to reduce the power consumption. Only one I/Q demodulated result is transferred to the baseband through

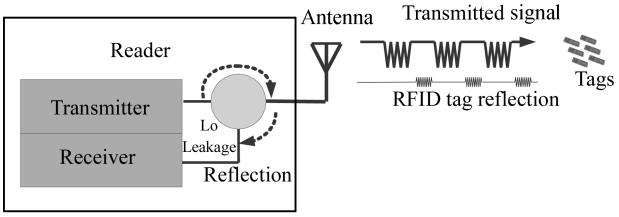

Fig. 1. RFID system operations.

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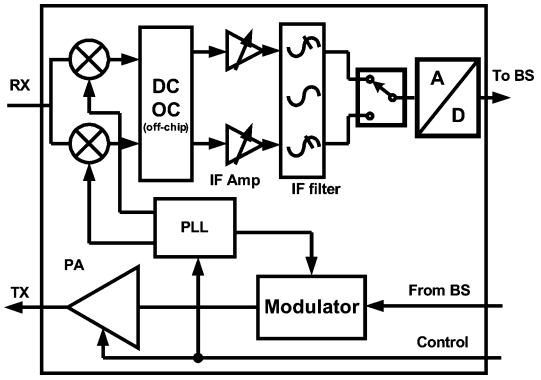

Fig. 2. Presented transceiver architecture.

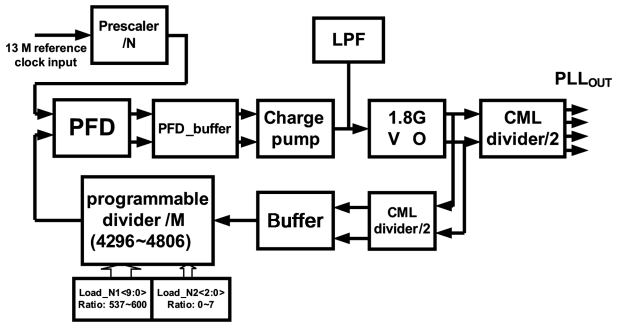

Fig. 3. Frequency synthesizer architecture.

the ADC in each interaction between reader and tag. The controller can determine which path would be selected by analyzing the result. The DC offset cancellation is realized by an off-chip capacitor. The transceiver does not use LNA in the receiver. This leads to low sensitivity but it is good to avoid the LNA saturation problem in RFID systems.

3. Circuit design

3.1. Frequency synthesizer

The diagram of the frequency synthesizer is shown in Fig. 3. The output frequency can be calculated by $f_{\text{out}} = \frac{M}{N} f_{\text{ref}}$, where M is the division ratio of the programmable divider and N is the division ratio of the prescaler. The frequency synthesizer integrates a voltage-controlled oscillator (VCO), a phase frequency detector (PFD), a charge pump, a high-frequency dual-modulus divider, and a digital programmable divider. All loop filter components are also integrated on-chip to reduce the external components. A 1.8 GHz LO signal is generated by the integrated VCO and then the 900 MHz differential I/Q LO signal is obtained by a divide-by-two circuit.

A LC VCO (Fig. 4) is implemented for its low noise. Complementary cross-coupled pairs, Mn1 Mn2 and Mp1 Mp2, generate negative resistance to compensate the LC loss. L1 L2 are the on-chip spiral inductors. In order to reduce the $1/f$ noise, Mpi2 is a long-channel PMOS transistor[4]. Compared with the traditional NMOS cross-coupling pair, a PMOS cross-coupling pair is added to improve the symmetry of the differential output and improve the phase noise performance[5]. A 3-bit switch-capacitor array is used for tuning the oscillation frequency to ensure the PLL can cover enough frequency bands.

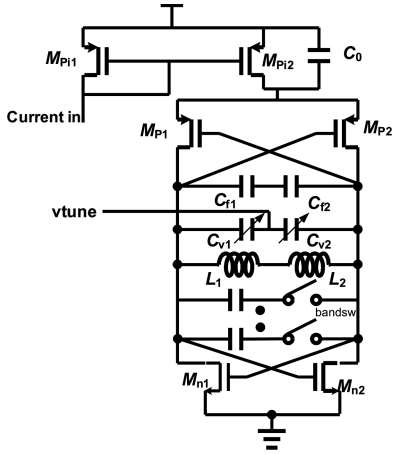

Fig. 4. VCO schematic.

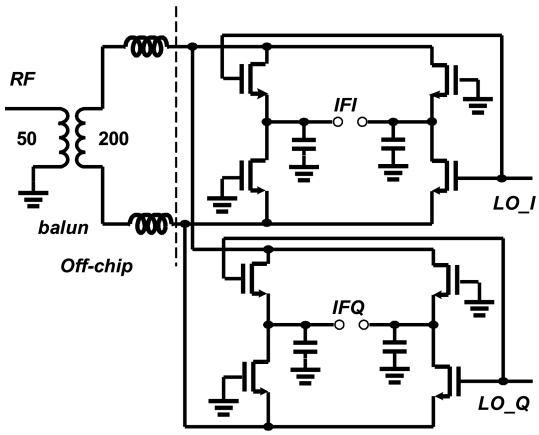

Fig. 5. Down-conversion mixer schematic.

3.2. Down-conversion mixer and VGA

As the first stage of the receiver, the linearity of the mixer should be high enough to deal with the large LO leakage in the passive RFID reader. The down-conversion mixer should have a $P_{1\text{dB}}$ of higher than 0 dBm. A passive differential mixer is used due to its high linearity (Fig. 5). An off-chip balun is employed to realize the single-ended to differential transform. The balun employed provides 6 dB voltage gain because its unbalanced impedance is 50 Ω while its balanced impedance is 200 Ω. The voltage gain of the matching network off-chip not only compensates the $2/\pi$ voltage attenuation caused by the switch of the passive mixer, but also provides the receiver with some voltage gain to improve the noise performance. This is very important to improve the noise performance of the receiver. The simulation result shows that the noise figure of the mixer is only 7.7 dB.

A 20–60 dB gain, 2 MHz bandwidth VGA is designed for the IF amplifier. A 20 dB fixed gain stage and two 0–20 dB variable gain stages are cascaded to achieve the 60 dB gain range, and the fix gain stage is put in front of the variable gain stages to reduce the noise. A source degeneration amplifier was used in the fixed gain stage and an improved Gilbert cell was used for the variable gain stages[6]. Current mirrors take the place of resistor loads and a CMFB circuit is applied to control the common level of the output signals in every stage. So the VGA is insensitive to process and temperature variations.

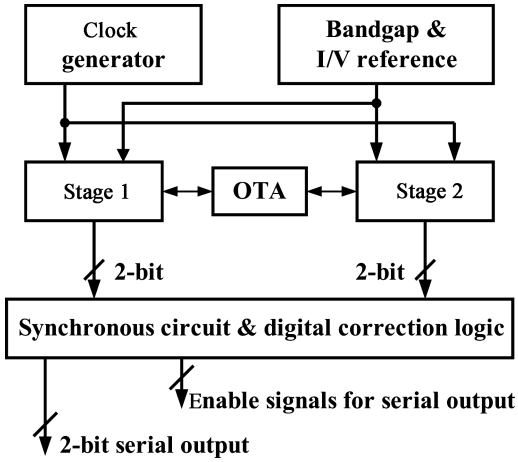

Fig. 6. Architecture of the proposed cyclic ADC.

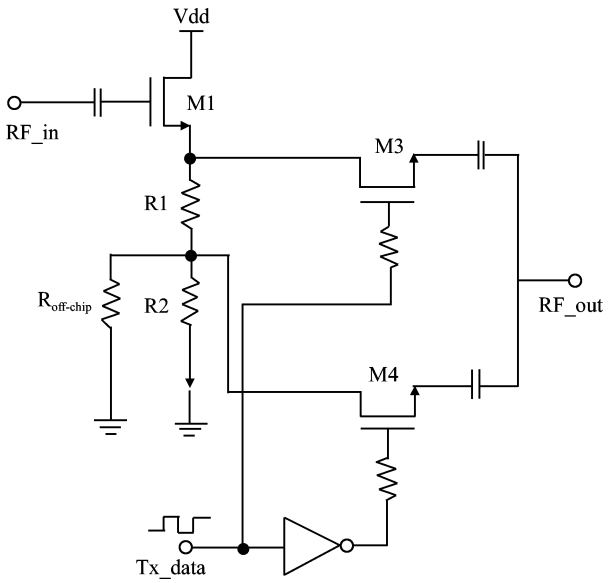

Fig. 7. Schematic of the RF signal modulator.

3.3. ADC

The backscattered communication data rate from tag to reader is usually under 100 kHz which is enough for mobile applications. After considering both the power consumption and the sampling rate, we utilize a 1-MHz cyclic ADC in this transceiver. The proposed 10-bit 1-MHz cyclic ADC architecture is shown in Fig. 6. It consists of an on-chip bandgap, current/voltage references, a clock generator, two cyclic stages and some extra supporting circuit blocks. In particular, the two stages share one operational transconductance amplifier (OTA) for the purpose of low power in order to satisfy mobile applications.

3.4. ASK modulator and power amplifier

The transmitter front-end is comprised of an OOK modulator and a two-stage class-E power amplifier. The direct-conversion architecture minimizes the off-chip components requirement and provides a low-cost, high-efficiency solution. The modulator (Fig. 7) has two functions. First, it serves as a driver to provide the RF carrier path from PLL output to PA. Second, it controls the RF signal to PA to generate different modulation depth amplitude modulation waves. In order

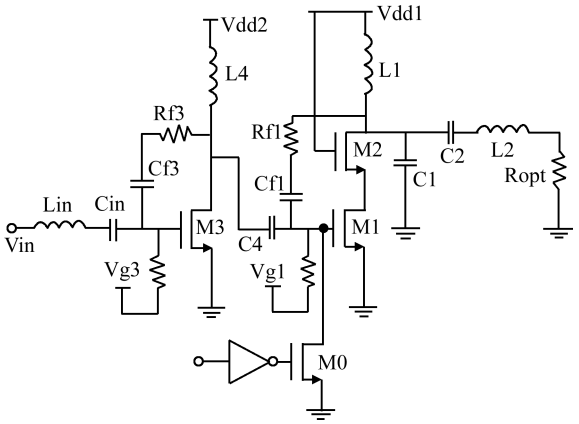

Fig. 8. Schematic of the class-E PA.

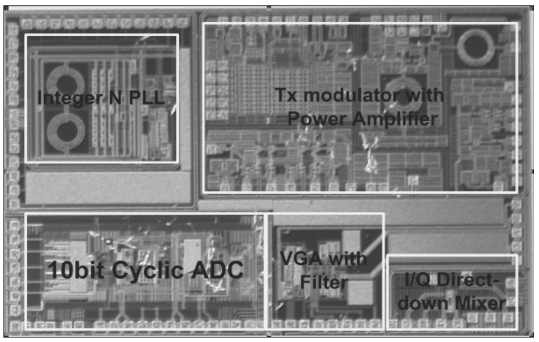

Fig. 9. Die photo of the proposed transceiver.

to obtain different RF output signals, two series resistors are connected to the source node of a source follower. Meanwhile, two switch transistors are followed in the RF signal path, respectively. The gates of the switch transistors are controlled by the transmitted OOK data, fulfilling the different modulations of the RF signal by different ratios of R_1 and R_2. Both R_1 and R_2 are implemented on-chip to generate a default modulation depth. Also an off-chip resistor can be connected parallel to R_2 to adjust the modulation depth to deal with the different requirements of the tags.

A non-linear PA was chosen due to its high power efficiency. Among all the switched-mode power amplifiers, class-E is the most attractive candidate in terms of circuit simplicity and high frequency performance[7]. Figure 8 shows the schematic of the presented two-stage class-E PA. The first stage works in class-AB mode and the second stage works in class-E mode, each with a power gain of about 11 dB. Except for the drain inductor L1, all the other components are integrated on-chip. The second stage can be shut down by a control signal through M0.

4. Measurement results

The RFID reader IC was fabricated using a standard 0.18-μm CMOS process. The chip microphotograph is shown in Fig. 9 with a die area of 4×2.5 mm^2 including pads. Different parts of the IC are connected off-chip and the match network was carefully designed to get good performance. The front-end IC is bounded to a PCB board and connected to the digital base band which is implemented in Xilinx SPARTAN XC3S400 FPGA for measurement purposes. To get the sensi-

Table 1. Summary of the transceiver I_c performance.

Parameter		Conditions	Measured result
Transmitter	Output power (P1Db)	Power amp	17.6 dBm
	Power consumption	1.8 V for modulator and driver stage 2.5 V for output stage	200 mW
	Input P_{-1dB}		5 dBm
	Sensitivity	40 kHz data rate	−70 dBm
Receiver	ADC peak SNDR	1 MS ample/s	55.9 dB
	ADC peak SFDR	1 MS ample/s	62 dB
	Power consumption	1.8 V for VGA, 2.7 for ADC@1MS ample/s	25.3 mW
PLL	Phase noise	f_{ref} = 13 MHz	−104 dBc/Hz@100 kHz −120.83 dBc/Hz@1 MHz
	Power consumption	1.8 V	54 mW

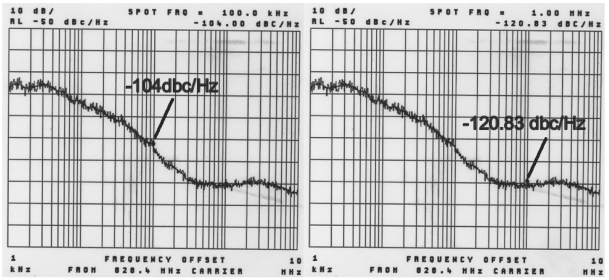

Fig. 10. Measured carrier phase-noise: (a) 100 kHz offset; (b) 1 MHz offset.

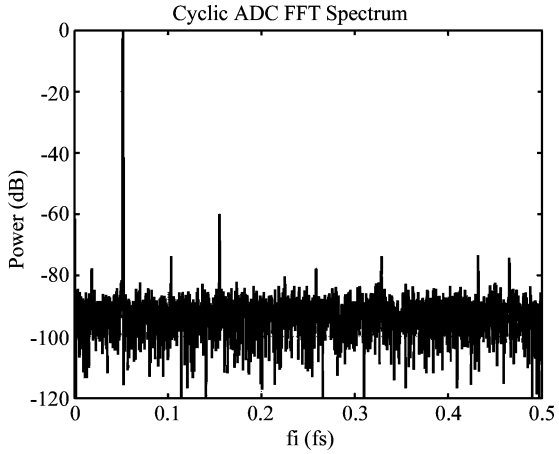

Fig. 11. Measured FFT spectrum.

tivity, we set the output of the PLL at a fixed frequency and connect the RF input of the IC with a signal generator which has a 40 kHz difference in frequency from that of the PLL. When the output power of the signal generator is –70 dBm, the demodulated result can still be observed at the output of the IC. So the sensitivity of the IC can achieve –70 dBm @ 40 kbps. The reader performance is summarized in Table 1. Figure 10 shows that the measured carrier phase-noise could achieve –104 dBc/Hz at 100 kHz frequency offset and –120.83 dBc/Hz at 1 MHz frequency offset. Figure 11 shows the measured FFT spectrum. With a –0.153 dBFS 2.4 MHz sine wave input at 1-MHz sampling rate, the measured peak spurious free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are 62.0 dB and 55.9 dB, respectively. Figure 12 gives out the measured output power and PAE of the power amplifier. The output 1dB power of the integrated PA

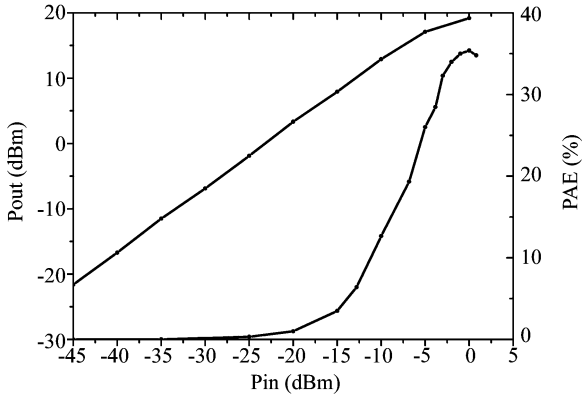

Fig. 12. Measured output power and power-added efficiency (PAE) versus input power (P_{in}) of the PA.

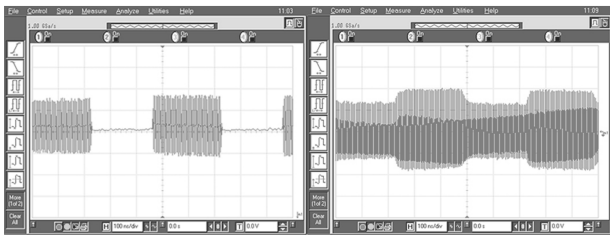

Fig. 13. Transient waveform for 100% and 18% modulation depth.

is about 17.6 dBm and the maximum PAE could achieve 35%. Figure 13 demonstrates the transient transmitted waveform with different modulation depth.

The UHF RFID reader IC presented in this paper is compared with other recently published works and summarized in Table 2. Reference [8] integrates a PA with enough power output, but the power consumption of the whole chip is too high. It is not suitable for mobile use. References [9] to [11] consume acceptable power, but they do not integrate the PA on-chip. Another PA must be added to form a reader with full functionality. This results in more space occupied on the mainboard just like a PCB board and it is not a perfect solution for mobile applications. The reader chip in this paper integrated a PA with enough output power to satisfy the requirements of mobile applications, and the other performance of the chip is enough to meet the specifications of mobile use. We will integrate an MCU with firmware in the next edition of the reader chip to minimize the difficulty of high level design.

Table 2. Performance summary of single-chip RFID readers.

Reference	Ref. [8]	Ref. [9]	Ref. [10]	Ref. [11]	This work
Process	0.18-μm SiGe BiCMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Integration level	RF + Analog + Digital Baseband	RF + Analog + Digital Baseband	RF + Analog + Data Converter	RF + analog + Digital Baseband	RF + Analog + AD
LO phase noise	−116 dBc/Hz@200 kHz −144 dBc/Hz@3.6 MHz	−87 dBc/Hz@100 kHz −120 dBc/Hz@1 MHz	−101 dBc/Hz@100 kHz −120 dBc/Hz@1 MHz	−110 dBc/Hz@200 kHz −127 dBc/Hz@1 MHz	−101 dBc/Hz@100 kHz −120.83 dBc/Hz@1 MHz
Input P_{1dB} (low gain mode)	11 dBm	8 dBm	−8 dBm	3.5 dBm	5 dBm
Sensitivity	20 dBm	N/A	−85 dBm	−90 dBm	−70 dBm
Output power	20 dBm	4 dBm	10 dBm	10.4 dBm	19 dBm
Die size	21 mm^2	23.9 mm^2	36 mm^2	18.3 mm^2	10 mm^2
Total power	1.5 W	160 mW	540 mW	< 276.4 mW	< 300 mW

5. Conclusion

A single chip UHF passive RFID reader is fabricated in a 0.18 μm CMOS process with a die area of 4 × 2.5 mm^2 including pads. The IC contains an OOK modulator and a power amplifier in the transmitter chain, an IQ direct-down converter, variable-gain amplifiers, channel-select filters and a 10-bit ADC in the receiver chain. A frequency resolution of 200 kHz is achieved with the on-chip integer N synthesizer, and it achieves a phase noise of –104 dBc/Hz at 100 kHz frequency offset and –120.83 dBc/Hz at 1 MHz frequency offset. The transmitter, the receiver and the frequency synthesizer consume 201.34, 25.3 and 54 mW respectively. The measured output max power of the transmitter is 19 dBm and the measured receiver sensitivity is –70 dBm.

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