# A 10-bit low power SAR A/D converter based on 90 nm CMOS*

Tong Xingyuan(佟星元)[1,†], Yang Yintang(杨银堂)[1], Zhu Zhangming(朱樟明)[1], Xiao Yan(肖艳)[2], and Chen Jianming(陈剑鸣)[2]

*(1 Institute of Microelectronics, Xidian University, Xi'an 710071, China)*

*(2 IP-2 of D. S. Division, Semiconductor Manufacturing International Corporation, Shanghai 201203, China)*

**Abstract:** Traditional and some recently reported low power, high speed and high resolution approaches for SAR A/D converters are discussed. Based on SMIC 65 nm CMOS technology, two typical low power methods reported in previous works are validated by circuit design and simulation. Design challenges and considerations for high speed SAR A/D converters are presented. Moreover, an *R–C* combination based method is also addressed and a 10-bit SAR A/D converter with this approach is implemented in SMIC 90 nm CMOS process. The DNL and INL are measured to be less than 0.31 LSB and 0.59 LSB respectively. With an input frequency of 420 kHz at 1 MS/s sampling rate, the SFDR and ENOB are measured to be 67.6 dB and 9.46 bits respectively, and the power dissipation is measured to be just 3.17 mW.

**Key words:** analog-to-digital converter; *R–C* combination; CMOS integrated circuits; nonlinearity; low power
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## 1. Introduction

A/D converters are pivotal building blocks in SoCs (system-on-chip) and have been widely used in HDTV, GSM and UWB communication systems. SAR A/D converters are especially popular for wireless communications, touch screen controllers and wireless sensor networks due to their simple architecture, small area and eaziness to be integrated with other IC blocks[1−3]. There are many types of state-of-the-art SAR A/D converters[1,4−10]. In Refs. [4, 5], 10-bit SAR A/D converters are realized based on a combination of resistor ladder and capacitor array. And several low power approaches have been proposed[6,7]. Before, due to their inherent not very high sampling rate, SAR A/D converters were just used in low to medium speed systems[8,9]. But recently, as in Refs. [1, 10], high speed SAR A/D converters have been realized with the time-interleaved approach.

With regard to more stringent requirements coming with the improved technology of SoC design, many novel approaches of high speed, high resolution and low power conversion for SAR A/D converter have been proposed in previous works. Thereby, in this paper, the previous designs are reviewed and studied. Discussions will not only be on the operation principles of these approaches but some challenges and considerations during the circuit design. Based on SMIC 65 nm CMOS technology, two typical low power methods reported in previous works are validated by circuit design and simulation. This is the first time that low power theories have been researched and compared based on 65 nm CMOS technology. With silicon feature dimensions downscaling into the nanometer scale, this research is of great importance to the development of embedded IP cores. Lastly, an *R–C* combination based approach is introduced and it is compared with traditional approaches. A 10-bit SAR A/D converter with this approach is implemented in SMIC 90 nm CMOS process. The measurement shows that it is very applicable to embedded SoCs.

## 2. Description of SAR A/D converter

An SAR A/D converter is illustrated in Fig. 1. It consists of an S/H circuit, a comparator, an SAR control unit and a D/A converter. Its operation is based on a "binary search" algorithm. The analog input is sampled and compared with the output of the D/A converter, which is under the control of the logic circuit. The reference voltage at particular stage depends on the value of the calculated bit. The reference voltage is calculated with the formula: $b_{n-1}V_{\rm ref}/2^1 + b_{n-2}V_{\rm ref}/2^2 + b_{n-3}V_{\rm ref}/2^3 + \cdots + b_0V_{\rm ref}/2^n$, where $n$ is the resolution of the converter. The digital outputs can then be sequentially generated by these comparisons.

SAR A/D converters can usually be implemented with either voltage scaling or charge redistribution approaches.

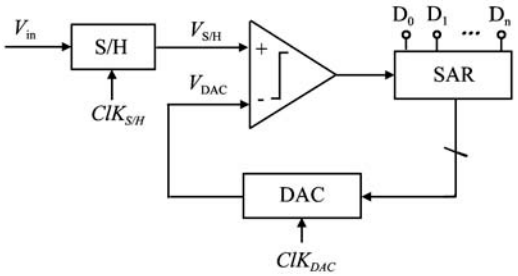


Fig. 1. Architecture of SAR A/D converter.

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† Corresponding author. Email: mayxt@126.com

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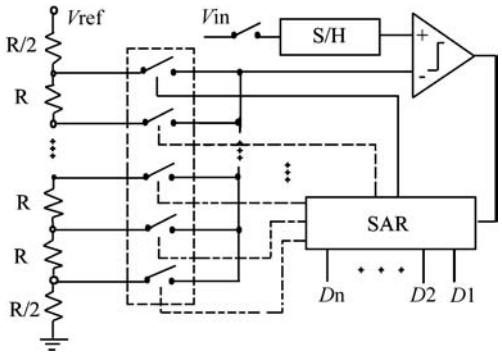


Fig. 2. Voltage scaling approach.

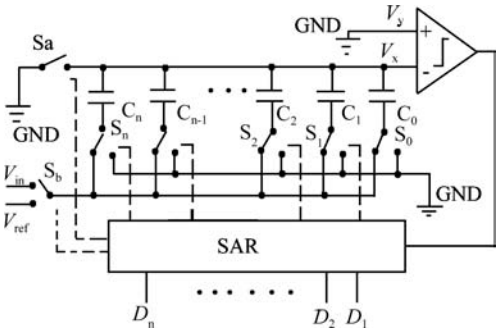


Fig. 3. Charge redistribution approach.

Figure 2 shows the architecture of a voltage scaling SAR A/D converter. A resistor string is used to divide the voltage reference into multiple voltages for comparison with the sampled input. For this type of converter with more than 8-bit resolution, high performance can hardly be achieved due to the correspondingly bad matching performance of the resistors.

The charge redistribution approach is illustrated in Fig. 3. Its internal D/A converter is realized with a capacitor array. Since capacitors have an inherent S/H function and are easier to match than resistors, this method is more popular than the voltage scaling approach.

## 3. Low power approaches for SAR A/D converters

In wireless sensor networks and wireless communication systems, designing low power A/D converters is one of the major challenges[1, 2] Compared with the voltage scaling approach, charge redistribution D/A converters are more suitable for low power applications because capacitors have no static consumption. In this part, two recently reported low power capacitor arrays for charge redistribution SAR A/D converters are discussed, and validated based on 65 nm CMOS technology.

### 3.1. Capacitor splitting approach[6]

Figure 4(a) is a 2-bit sample with traditional charge redistribution approach. From Fig. 3, we know that $V_x$ equals $-V_{\text{in}}$ during the hold step. When the converter enters the charge redistribution step, $C_2$ in Fig. 4(a) is switched to $V_{\text{ref}}$ to generate $D_2$. If $V_{\text{in}} > V_{\text{ref}}/2$, $D_2$ = "1", and then the capacitor $C_1$ will also be connected to $V_{\text{ref}}$ to decide $D_1$ (an "up" transition shown in Fig. 4(a)). During this transition, energy should be drawn from $V_{\text{ref}}$ to change the state of the capacitor array. Based on the capacitor energy formula:

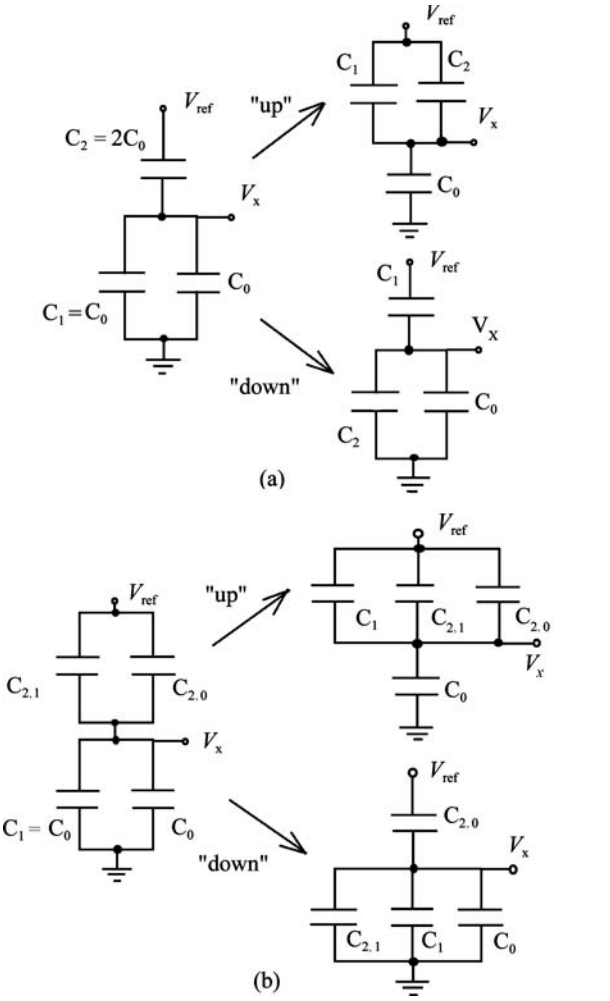


Fig. 4. Operation of (a) traditional charge redistribution approach and (b) capacitor splitting approach.

$$E_{\text{Change}} = \int_{t_1}^{t_2} i_{\text{ref}} V_{\text{ref}} \mathrm{d}t = V_{\text{ref}} \int_{t_1}^{t_2} i_{\text{ref}} \mathrm{d}t$$
$$= V_{\text{ref}} Q_{t_1 \to t_2} = V_{\text{ref}} (Q_{t_2} - Q_{t_1}), \quad (1)$$

the energy drawn from $V_{\text{ref}}$ during the "up" transition can be computed as follows:

$$E_{\text{up}} = V_{\text{ref}} (Q_{C_1, t_1 \to t_2} + Q_{C_2, t_1 \to t_2})$$
$$= V_{\text{ref}} \left[ \frac{3}{4} + \left( -\frac{1}{2} \right) \right] V_{\text{ref}} C_0 = \frac{1}{4} C_0 V_{\text{ref}}^2. \quad (2)$$

Here, $Q_{C_1, t_1 \to t_2}$ and $Q_{C_2, t_1 \to t_2}$ represent the charge changes of $C_1$ and $C_2$ during the "up" transition.

If $V_{\text{in}} < V_{\text{ref}}/2$, $D_2$ = "0", and then, to generate $D_1$, $C_2$ is connected to ground while $C_1$ is switched to $V_{\text{ref}}$ (a "down" transition shown in Fig. 4(a)). In this process, only $C_1$ needs to be charged by $V_{\text{ref}}$. From Eq. (1), the energy drawn from $V_{\text{ref}}$ in this process can be derived as below:

$$E_{\text{down}} = V_{\text{ref}} \left[ \frac{3}{4} - \left( -\frac{1}{2} \right) \right] C_0 V_{\text{ref}} = \frac{5}{4} C_0 V_{\text{ref}}^2. \quad (3)$$

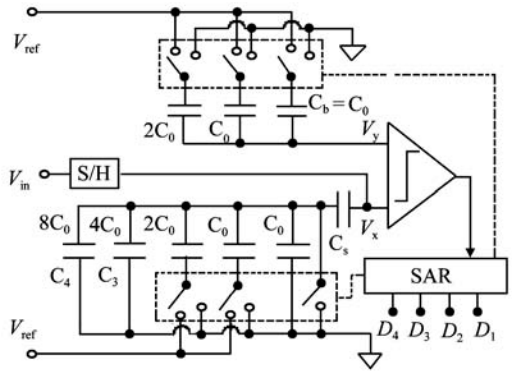


Fig. 5. Two-step approach.

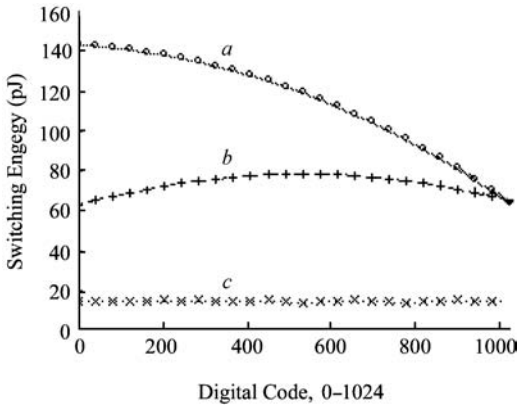


Fig. 6. Switching energy of capacitor arrays in 10b A/D converters with (*a*) traditional charge redistribution approach, (*b*) capacitor splitting approach, and (*c*) two-step approach versus digital code.

It is five times the energy dissipated in the "up" transition. This occurs because all of the charge initially on $C_2$ is discharged to ground, but all the charge that ends up on $C_1$ must be delivered from $V_{\rm ref}$. To reduce energy dissipation in the "down" transition, a capacitor splitting approach is presented in Ref. [6].

Figure 4(b) is a 2-bit sample with the capacitor splitting approach. The MSB capacitor $C_2$ is split into $C_{2,1}$ and $C_{2,0}$ in parallel, where $C_{2,1} = C_1$, $C_{2,0} = C_0$. During the "down" transition, what needs to be done is just to switch $C_{2,1}$ to ground directly, thereby avoiding charging any capacitor to $V_{\rm ref}$. The energy required is just to drive the state change of $C_{2,0}$. It can be computed with Eq. (1) as below:

$$E_{\rm down,Split} = V_{\rm ref}\left(\frac{3}{4} - \frac{1}{2}\right)C_0 V_{\rm ref} = \frac{1}{4}C_0 V_{\rm ref}^2. \quad (4)$$

Compared with Eq. (3), the capacitor splitting approach consumes less energy in the "down" transition. For an A/D converter with this approach, the $k$-th bit capacitor $C_k$ is realized by $C_0 + C_1 + \cdots + C_{k-1}$. This methodology guarantees that only one capacitor needs to be switched. For each bit cycle, the energy consumed in the "down" transition is identical to that consumed in the "up" transition.

### 3.2. Two-step approach[7]

In the traditional charge redistribution approach, a large amount of energy is consumed in the decisions of upper bits which correspond to large size capacitors. The two-step approach proposed in Ref. [7] uses two capacitor arrays to decide the upper bits and lower bits separately. In the decision of the upper bits, smaller capacitors can be used in the coarse quantization, so energy dissipation can be dramatically reduced.

Figure 5 shows a 4-bit sample with the two-step approach. In the sample step, $V_{\rm in}$ is sampled by $C_{\rm s}$, $V_x = V_{\rm in}$. When the converter enters the coarse quantization step, $V_x$ is unchanged and $V_y$ is controlled to approximate $V_x$ for the determination of bit-4 and bit-3. Since the coarse quantization capacitor array is just to decide the first two bits, just $2^2C_0$ is needed. During the fine quantization step, $V_y$ is kept unchanged and $V_x$ is controlled to move towards $V_y$ for the decision of bit-2 and bit-1. In Fig. 5, after the coarse quantization, $C_{\rm b}$ is connected to $V_{\rm ref}$ so $V_y$ can be boosted by $V_{\rm ref}/4$, and then, at the beginning of the fine quantization step, $V_x < V_y$. A 4-bit capacitor array is used to meet the voltage resolution for fine quantization. Since the upper bits have been generated, the bottom plates of $C_3$ and $C_4$ are connected to ground during the fine quantization step, causing no extra energy consumption.

### 3.3. Discussion and considerations

With no extra sequence and area, the capacitor splitting approach dissipates less energy in the "down" transition than the traditional approach. But the improvement is just made for the "down" transition, so the energy saving advantage would be minimal at large output codes. Also, the layout design of this approach is complex. Especially for higher resolutions, linearity errors can be caused by coupling from so many interconnection lines. The parasitic capacitances will influence the overall performance of the converter. Shielding is a solution for minimizing the influence of the parasitic capacitances, but careful layout design is still necessary to minimize the mismatch due to the technological process, because any mismatch between two capacitors will cause nonlinearity[11, 12].

Due to the minimization of the capacitors corresponding to the upper bits, the two-step approach can dramatically reduce the energy dissipation. But the LSBs must be obtained by the complementary code of the fine quantization results, and to meet the resolution of the fine quantization, more capacitors are required.

Based on SMIC 65 nm CMOS technology, three 10-bit SAR A/D converters are designed with the traditional charge redistribution approach, the capacitor splitting approach and the two-step approach. In the two-step structure, a "5 MSBs + 5 LSBs" approach is utilized, and the capacitor splitting approach is combined with this structure to further reduce the energy dissipation. Here, the value of unit capacitor $C_0$ is 50fF. Attention must be paid to the trade-off, where larger capacitors consume more power dissipation and smaller ones make it difficult to realize good matching performance. Figure 6 shows the simulated switching energy of capacitor arrays in the designed converters. Compared with the traditional approach, the capacitor splitting approach can save more energy at smaller

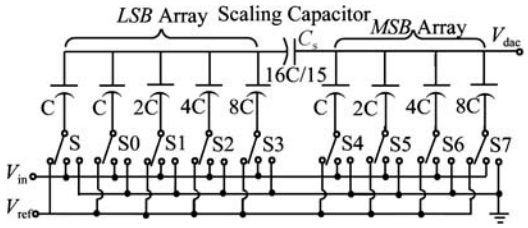


Fig. 7. Scaling capacitor based approach.

output codes. The energy-saving advantage of the two-step approach is obvious in the full range.

## 4. High speed approaches for SAR A/D converters

With silicon feature dimensions downscaling into the nanometer scale, high speed A/D converters have become more important than ever in SoC design[13]. As we know, SAR A/D converters are generally used in low sampling rate applications. However, approaches have been proposed for SAR A/D converters to realize high sampling rates.

### 4.1. Scaling capacitor based approach[14]

The concept of the scaling capacitor based approach used in Ref. [14] is to decrease the size of the MSBs' capacitors. Figure 7 shows an 8-bit sample with this approach. It combines two 4-bit charge redistribution sub-D/A converters. The scaling of the LSB sub-converter is accomplished through the scaling capacitor $C_s$. Since the series combination of $C_s$ and the LSB array must terminate the MSB array or equal $C$, we find that the value of the scaling capacitor, $C_s$, should be $16C/15$. The equivalent voltage of the MSB array, $V_1$, and the LSB array, $V_2$, can be written as follows:

$$V_1 = V_{\text{ref}}\,(D_7 \times 8C + D_6 \times 4C + D_5 \times 2C + D_4 \times C)/15C,$$

and

$$V_2 = V_{\text{ref}} \times (D_3 \times 8C + D_2 \times 4C + D_1 \times 2C + D_0 \times C)/16C.$$

From the approximation principle for SAR A/D converters, at the end of the conversion step, we have:

$$V_{\text{in}} \times 16C = V_2 \times C + V_1 \times 15C.$$

After rearrangement, we obtain:

$$V_{\text{in}} = V_{\text{ref}} \sum_{i=0}^{7} D_i \times 2^{-(N-i)}. \tag{5}$$

With this approach, the sizes of the MSBs' capacitors are dramatically decreased. Thus, with careful optimization of the switches connected to the capacitor array, a small time constant of D/A conversion can be realized. Certainly, a high speed comparator and logic circuit are also important in high speed SAR A/D converters. In Ref. [14], a 10MS/s SAR A/D converter has been realized with this approach.

### 4.2. Time-interleaved approach[15]

The time-interleaved approach was initially proposed in Ref. [15]. As shown in Fig. 8, a time-interleaved A/D converter consists of $m$ parallel A/D converters, which are called "channel converters" and have the same sampling rate. Yet they operate at interleaved sampling times, as though they were effectively a single A/D converter operating at $m$ times higher sampling rate. Recently, with this approach, SAR A/D converters with a high throughput rate have been realized without sacrificing their inherent low power merit [1, 10].

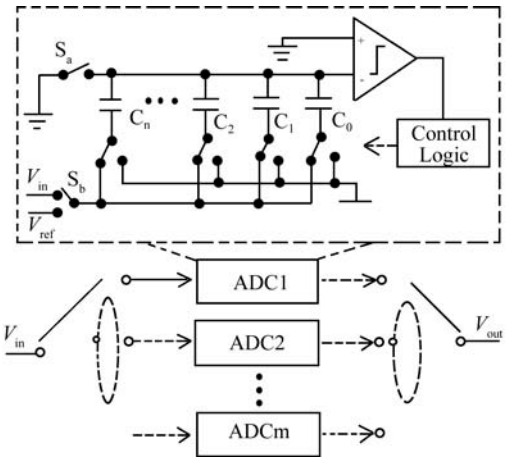


Fig. 8. Time-interleaved approach.

### 4.3. Design challenges and considerations

SAR A/D converters are generally used for medium to high resolution, low sampling rate operations. An $n$-bit SAR A/D converter requires at least $n + 1$ clock periods to produce the output. Its speed is mainly limited by the settling time of its internal D/A converter and the comparator. The comparator must resolve small input differences within the specified time. For the D/A converter, it must settle to within the resolution of the overall converter. As we mentioned in part 2, the charge redistribution approach is more popular. However, the challenge of realizing a high speed SAR A/D converter with this approach is the trade-off between choosing small size capacitors and realizing good linearity.

For the scaling capacitor based approach, it really can realize higher speeds due to the decreased capacitor size. However, this approach is very sensitive to errors in the scaling capacitor because the correct generation of LSBs is based on accuracy of the scaling capacitor $C_s$. In fact, with standard CMOS technologies, the substrate parasitic capacitances make it hard to realize good matching performance and an accurate $C_s$.

Time-interleaved SAR A/D converters can realize sampling rates as high as flash converters[10]. But their performance is limited by the offset mismatch, gain mismatch and sample time mismatch among time-interleaved channels. Thus, careful layout, foreground calibration, digital filters or trimming are usually used to minimize these mismatches. Additionally, from comparison with a flash A/D converter in Ref. [16], we must note that time-interleaved SAR A/D converters are preferential to flash converters only when the resolution is larger than a certain threshold.

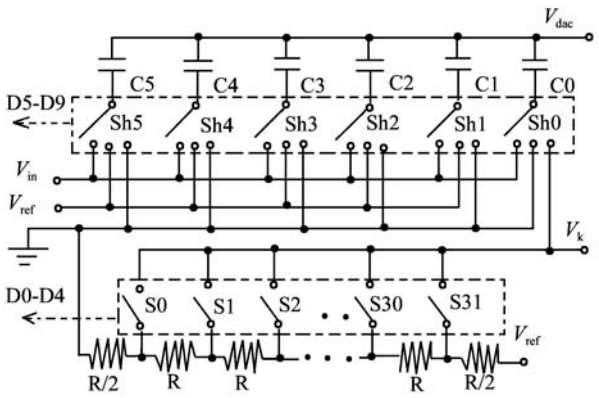


Fig. 9. *C–R* combination based approach.

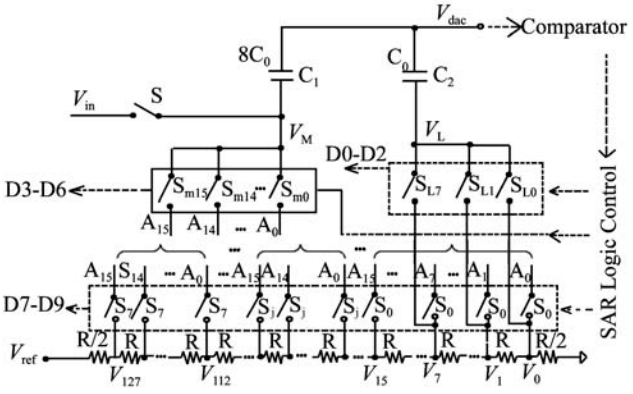


Fig. 10. An *R–C* combination based approach.

## 5. *C–R* combination based approach[4, 5]

SAR A/D converters with no less than 10-bit resolution are necessary for the touch-screen controllers used in GPS and mobile phones[3]. But for traditional voltage scaling and charge redistribution SAR A/D converters, with the resolution increasing, the total number of resistors or capacitors in their D/A converters will also increase exponentially. Therefore, many passive components make it difficult for them to be integrated with other IC blocks in SoC design[17].

Figure 9 is a *C–R* combination based approach used in Refs. [4, 5]. A "5 MSBs + 5 LSBs" approach is utilized, where the 5 MSBs are realized by a capacitor array, and the 5 LSBs are realized by a resister ladder. In Fig. 9, $C_5 = 2C_4 = 4C_3 = 8C_2 = 16C_1$, $C_1 = C_0$. In the sampling step, $V_{in}$ is sampled by capacitors $C_0$–$C_5$ with switches Sh0–Sh5 connected to $V_{in}$. During the conversion step, capacitor $C_0$ is connected to ground, and capacitors $C_1$–$C_5$ are switched to $V_{ref}$ or ground under the control of the logic circuit. $D_9$–$D_5$ can then be generated. After $D_9$–$D_5$ are generated, the resistor ladder is used to generate $D_4$–$D_0$ with the switches $S_0$–$S_{31}$ controlled by logic circuits. Then, with the approximation principle of SAR A/D converters, at the end of the conversion step, we have:

$$V_{in} \times 2^5 C_0 = V_{ref}\left(D_{10-1} \times 2^{5-1} C_0 + D_{10-2} \times 2^{5-2} C_0 + \cdots + D_{10-5} \times C_0\right) + V_k \times C_0.$$

With the substitution of $V_k = V_{ref}(D_{5-1} \times 2^{-1} + D_{5-2} \times 2^{-2} + \cdots + D_1 \times 2^{-(5-1)} + D_0 \times 2^{-5})$, we can approximate $V_{in}$ as below:

$$V_{in} = V_{ref}\left(\sum_{i=1}^{5} D_{10-i} \times 2^{-i} + \sum_{i=5+1}^{5+5} D_{10-i} \times 2^{-i}\right) = V_{ref} \sum_{i=1}^{10} D_{10-i} \times 2^{-i}. \quad (6)$$

With this approach, the total passive components used for the internal D/A converter are dramatically reduced, which is important for high resolution applications. Also, due to the inherent sample and hold function of the capacitor array, no additional S/H circuit is needed.

## 6. *R–C* combination based approach

### 6.1. Topology and operation

Figure 10 shows an *R–C* combination based approach. 10-bit D/A conversion is realized with the combination of a 7-bit resistor ladder and an 8:1 capacitor pair. $V_M$ represents the output of the 7-bit voltage scaling D/A converter while $V_L$ is the output value of its last three bits, and $C_1 = 8C_0$, $C_2 = C_0$. Here, $C_0$ represents the unit capacitor. In the sampling phase, with the switch S turned on, the analog input $V_{in}$ is sampled by capacitor $C_1$ while $V_L$ is connected to $V_5$ which has a voltage value of $9V_{ref}/256$. In the converting phase, $V_M$ is connected to $C_1$ and $V_L$ is connected to $C_2$. Then, with the approximation principle of SAR A/D converters, at the end of the converting phase, we have:

$$V_{in} \times 8C_0 + V_5 \times C_0 = V_M \times 8C_0 + V_L \times 1C_0.$$

After rearrangement, we obtain:

$$V_{in} = V_M + \frac{1}{8}(V_L - V_5).$$

With the substitution of $V_M = \frac{V_{ref}}{128}\left(\sum_{i=3}^{9} D_i \times 2^{i-3} + \frac{1}{2}\right)$ and $V_L = \frac{V_{ref}}{128}\left(\sum_{i=0}^{2} D_i \times 2^i + \frac{1}{2}\right)$ into it, we can approximate $V_{in}$ as below:

$$V_{in} = \frac{V_{ref}}{1024} \sum_{i=0}^{9} D_i \times 2^i. \quad (7)$$

### 6.2. Discussion and comparison

Obviously, in this approach, the total number of passive components is less than that in traditional approaches. Thus, it is easier to utilize to realize high resolution SAR A/D converters. As discussed in Section 6.1, due to the inherent sample and hold function of the capacitor, no additional S/H circuit is needed. This is very similar to the approach discussed in Section 5. For the capacitor matching performance, only $C_1$ and $C_2$ need to be matched well in this architecture, while more than two capacitors need good matching performance in the

Table 1. Summary of traditional and hybrid approaches.

| | 10-bit voltage division | 10-bit charge redistribution | 3MSBs + 7LSBs *C–R* | 7MSBs + 3LSBs *R–C* |
|---|---|---|---|---|
| Unit resistor | $2^{10}R_0$ | — | $2^7R_0$ | $2^7R_0$ |
| Unit capacitor | — | $2^{10}C_0$ | $2^3C_0$ | $(2^3 + 1)C_0$ |
| Resistor need to be matched | $2^{10}R_0$ | — | $2^7R_0$ | $2^7R_0$ |
| Capacitor need to be matched | — | $2^{10}C_0$ | $C_0$, $C_0$, $2C_0$, and $4C_0$ | $C_0$, and $8C_0$ |

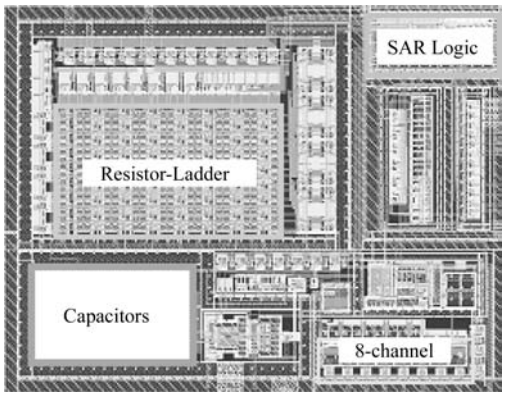


Fig. 11. Micrograph of the proposed converter.

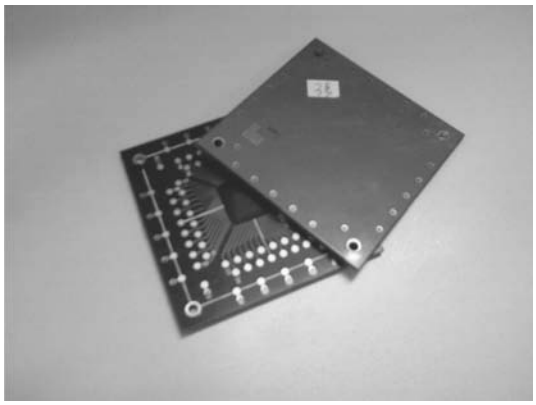

Fig. 12. Chips for measurement.

*C–R* combination based approach. Thus, with this *R–C* combination based approach, it is easier to realize good matching performance than in the *C–R* combination based approach.

Table 1 gives a summary of the traditional approaches and the two hybrid approaches. Here, $C_0$ and $R_0$ represent the unit capacitor and the unit resistor respectively.

### 6.3. Circuit implementation and measurement

With this *R–C* combination based approach, a 10-bit SAR A/D converter has been implemented in the SMIC 90 nm CMOS 1P6M process. The design results show that it is very suitable for embedded systems. A layout photograph is shown in Fig. 11, where it occupies an area of $253 \times 217$ $\mu$m$^2$. In the layout design, each unit resistor is sided by dummies for good matching performance, and the capacitors are routed with a common-central symmetry method to reduce the nonlinearity error.

The chips for measurement are shown in Fig. 12. The DNL and INL of this converter are measured with the histogram testing method[18]. After the mass sampled data are processed with the "Matlab" program, DNL and INL plots are generated from "Microsoft Office Excel", as shown in Fig. 13. The measured DNL and INL are 0.31 LSB and 0.59 LSB, respectively.

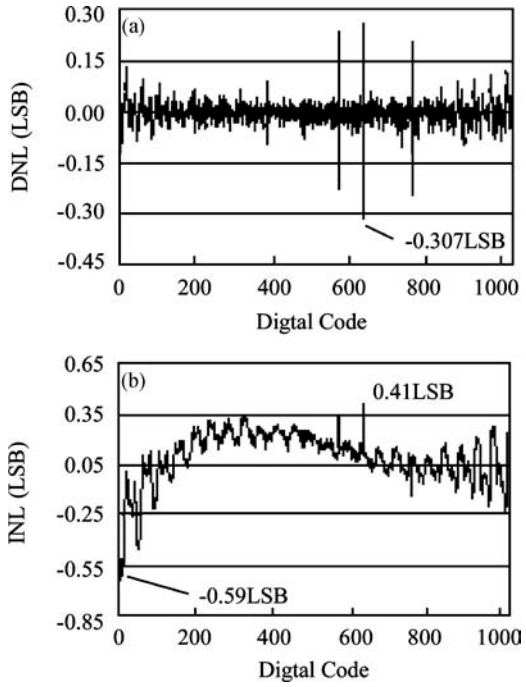


Fig. 13. Measured DC characteristics: (a) DNL; (b) INL.

The AC characteristics are measured at 1 MS/s sampling rate. Figure 14(a) is a 2000 point DFT spectrum measured with a 420 kHz single-ended sine wave input signal. The ENOB is 9.46 bits and the SFDR is measured to be 67.6 dB. Figure 14(b) indicates the measured SINAD and SFDR at different input frequencies. With low frequency inputs, this ADC features even better performance.

The overall performance of the proposed A/D converter is summarized in Table 2. To enable a comparison with other works, the FOM (figure of merit)

$$\text{FOM} = \frac{P_{\text{diss}}}{2^{\text{ENOB}} \times f_{\text{sample}}}$$

is used, where $P_{\text{diss}}$ is the power dissipation of the converter, and ENOB is measured at the sampling rate $f_{\text{sample}}$. For the proposed converter, the typical power dissipation is 3.17 mW including the output drivers and the ENOB is 9.46 measured with a 420 kHz single-ended sine wave sampled at 1 MS/s. Table 3 gives a comparison with some previous work[2, 4, 8]. From the comparison, it can be seen that the proposed converter features high performance. This converter also features a better FOM than ADS7843 from Texas Instruments which has a

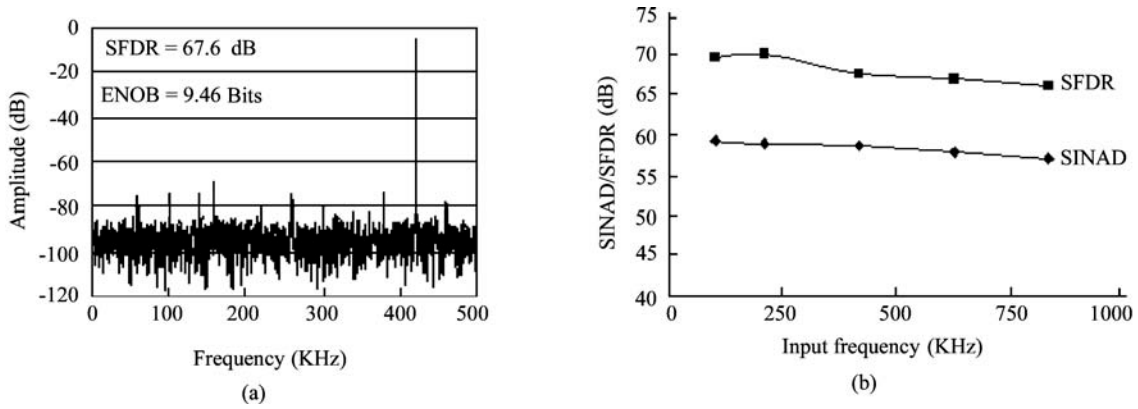


Fig. 14. Measured AC characteristics: (a) 2000 point DFT spectrum @ 420 kHz input; (b) SINAD and SFDR versus $f_{in}$.

Table 2. Performance summary of the A/D converter.

| Paramenter | Value |
|---|---|
| Technology | 90 nm CMOS 1P6M |
| Supply voltage | 1.2, 2.5 V |
| Input range | 1.25 ± 1.235 V |
| Sampling rate | 1 MS/s |
| ENOB ($f_{in}$ = 420 kHz) | 9.46 bits |
| SINAD ($f_{in}$ = 420 kHz) | 58.71 dB |
| SFDR ($f_{in}$ = 420 kHz) | 67.60 dB |
| THD ($f_{in}$ = 420 kHz) | 61.71 dB |
| DNL | 0.31 LSB |
| INL | 0.59 LSB |
| Power dissipation | 3.17 mW |
| Active area | 253 × 217 $\mu$m$^2$ |

Table 3. Comparison with some previous work.

| Reference | Resolution (bit) | DNL (LSB) | INL (LSB) | Area (mm$^2$) | FOM (pJ/conversion step) |
|---|---|---|---|---|---|
| Ref. [2] | 10 | 0.4 | 0.5 | 5.0 | 480 |
| Ref. [4] | 10 | 0.5 | 0.5 | 0.4 | 5.9 |
| Ref. [8] | 8 | 0.18 | 0.87 | 0.14 | 9.0 |
| This work | 10 | 0.31 | 0.59 | 0.054 | 4.5 |

maximum FOM of about 14.6 pJ per conversion step.

## 7. Conclusion

Several recently reported low power, high speed and high resolution approaches for SAR A/D converters are discussed. Two typical low power approaches proposed in previous works are validated based on SMIC 65 nm CMOS technology. Some challenges and considerations for high speed SAR A/D converters are presented. Finally, an *R–C* combination based approach for SAR A/D converters is discussed. A 10-bit low power converter with this approach is implemented in the SMIC 90 nm CMOS 1P6M process. Measurement shows that it achieves high performance. With silicon feature dimensions downscaling into the nanometer scale, low power A/D conversion within a small area has become a key requirement for applications such as portable systems and touch screen SoCs, and this proposed converter is very suitable for these applications.

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