Noise performance in AlGaN/GaN HEMTs under high drain bias*

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Abstract: The advent of fully integrated GaN PA-LNA circuits makes it meaningful to investigate the noise performance under high drain bias. However, noise performance of AlGaN/GaN HEMTs under high bias has not received worldwide attention in theoretical studies due to its complicated mechanisms. The noise value is moderately higher and its rate of increase is fast with increasing high voltage. In this paper, several possible mechanisms are proposed to be responsible for it. Impact ionization under high electric field incurs great fluctuation of carrier density, which increases the drain diffusion noise. Besides, higher gate leakage current related shot noise and a more severe self-heating effect are also contributors to the noise increase at high bias. Analysis from macroscopic and microscopic perspectives can help us to design new device structures to improve noise performance of AlGaN/GaN HEMTs under high bias.

Key words: GaN HEMT; noise performance; high drain bias; high electric field; impact ionization
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1. Introduction

During the past few years, there has been fervent GaN HEMT activity to develop high power performance resulting in excellent power density[1,2]. More recently, there has been considerable interest in developing robust low noise GaN HEMTs[3,4]. The feasibility of combining high power, low noise, high efficiency, high dynamic range, high survivability, and robustness properties of GaN HEMTs opens up new possibilities in the design and fabrication of fully integrated GaN LNA-PA MMICs on one wafer, thus having a significant impact on next generation military phase array radar systems, which require high performance, small size and weight per T/R module[5,6]. The company of Sirenza Microdevices reports a high dynamic range GaN MMIC LNA-PA which achieves a low noise value and a P_{1dB} of 2 W. It achieves NF of 0.7–0.9 dB at high power bias (15 V) and 0.5 dB at lower bias[6].

Traditional transceiver design requires separate power and low noise amplifiers, which needs at least two different DC bias conditions or a DC–DC converter[7]. All these components will increase the cost of the application, while GaN based technology can use only one amplifier to fulfill all these requirements. Without a doubt, in order to obtain high power, a fully integrated LNA-PA circuit should be biased under relatively high drain voltages. Even though the noise value of GaN technology under high bias may be slightly inferior, the overall transceiver performance including the noise performance will be greatly improved over the others[8]. For example, the robustness of the GaN LNAs facilitates the omission of additional RF limiting/protection circuitry in the receiver path which severely degrades noise performance and dynamic range of the system[9]. However, the integrated LNA-PA circuits applied with high bias really show a moderately higher noise value, and the rate of rise of NFmin is faster as the high voltage increases. In order to improve noise performance and suppress the increasing rate of the noise value under high bias, it is necessary for us to attentively analyze the special mechanism of noise in GaN HEMTs, explore possible reasons responsible for noise increasing at high voltages and take corresponding measures.

2. Device and process description

Figure 1 shows the layer structure of the transistor which is an $Al_{0.2}Ga_{0.8}N$–AlN–GaN multilayer grown on a semi-insulating 4H-SiC substrate. The two inch epitaxial wafer grown by MOCVD was provided by the Institute of Semiconductors of the Chinese Academy of Sciences. An average electron mobility of 1250 $cm^2/(V{\cdot}s)$ and a sheet carrier density of 1.4×10^{13} cm^{-2} were obtained by room-temperature Hall measurement. The AlGaN/GaN HEMT fabrication commenced with the definition of the active device area. This isolation was implemented by an ion implantation mesa. Next, ohmic contacts were formed by first depositing the ohmic metals Ti/Al/Ti/Au followed by rapid thermal annealing (RTA) at 870 °C for 50 s. All these steps resulted in a low specific contact resistance of $l0^{-6}$ $\Omega{\cdot}cm^2$. Then, the T-Schottky gate was formed by Ni/Au evaporation and the subsequent lift-off process. The gate length and width were 0.25 μm and 140 (35×4) μm, respectively. Finally, Au air bridges were deposited by electroplating in order to connect different source areas. In

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i-GaN	3 nm
i-AlGaN	25 nm
AlN	1 nm
GaN	3 μm
4H-SiC	

Fig. 1. Layer structure for a transistor grown by MOCVD.

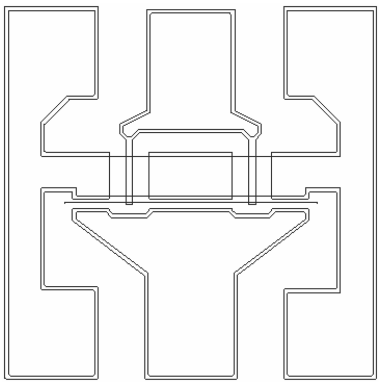

Fig. 2. Layout of GaN HEMT designed for low noise.

order to reduce gate and source resistances to obtain good noise performance of the GaN HEMTs, a kind of four-finger transistor was especially designed, the layout of which is shown in Fig. 2.

3. Noise measurement and result analysis

Before the noise measurement and result analysis, some related noise mechanisms will be illustrated briefly. When biased under moderate V_{ds}, in general, three main kinds of noise mechanisms have been identified to be responsible for the high frequency noise of GaN HEMTs, which can be represented as an equivalent noise voltage source, and gate and drain noise current sources in the noise model. Parasitic resistances will generate thermal noise, which is considered at thermal equilibrium. Gate leakage current associated shot noise originates from the randomness of the electron injection into the channel over the gate Schottky barrier. Drain diffusion noise is caused by variation in the velocity of the carriers scattering in the channel. It is a kind of non-equilibrium distributed noise in the channel, which is strongly bias-dependent.

Multi-bias high frequency noise parameter on-wafer property measurement was undertaken by an Agilent PNA-X based noise parameter measurement combined with Maury automated tuners and an Agilent 346C noise source. The noise parameter measurement system, shown schematically in Fig. 3, can realize fast and accurate calibration and measurement. The noise values of the devices were measured on-wafer at a single frequency of 8 GHz and a single gate–source voltage V_{gs} of –2 V for various drain bias conditions, with V_{ds} from 4 to 26 V, which is displayed in Fig. 4(a). It is noticeable that there is no significant increase in NFmin when V_{ds} is applied below 16 V, from 0.9 dB under 4 V to 1.19 dB under 16 V. However, there is a sharp increase with V_{ds} when it is applied

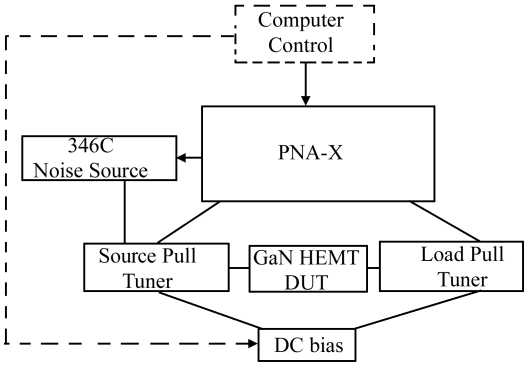

Fig. 3. PNA-X based noise parameter measurement setup.

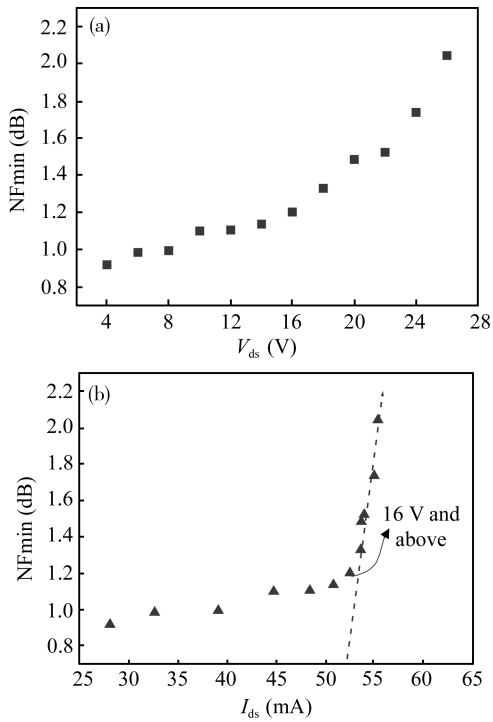

Fig. 4. (a) Typical plot of NFmin versus drain–source voltage at 8 GHz with V_{gs} of –2 V; (b) Change of NFmin with corresponding drain–source current at 8 GHz with V_{gs} of –2 V.

larger than 16 V, from 1.19 to 2.0 dB under 26 V. There are different mechanisms in noise increase when GaN HEMTs are applied at large drain voltages. These underlying physical mechanisms of noise are helpful for us to identify ways in which new device structures or geometry can be adopted to improve noise performance and suppress the increasing rate of NFmin under high bias. Next, several possible mechanisms are proposed.

Figure 4(b) shows the relationship between NFmin and corresponding I_{ds} with frequency fixed at 8 GHz and V_{gs} at –2 V. It also shows that I_{ds} nearly flattens out at a value of 54 mA when V_{ds} is applied above 16 V. It is observed that NFmin is essentially constant with increasing V_{ds} under lower V_{ds}, whereas it increases dramatically under high bias in the I_{ds} saturation region. Under moderate high V_{ds}, the dominant contribution to the slight increase in noise is due to fluctuation of the carrier velocity in the channel. However, under high V_{ds}, the carrier velocity is approaching saturation, in

which precondition fluctuation in carrier density is most likely to account for the dramatic rise in NFmin. What causes the great fluctuation of carrier density under high electric field? The ensemble Monte Carlo simulation of impact ionization by Kolnik *et al.*[10] sheds some light for us to relate the unique performance of GaN noise under high electric field to the impact ionization process. In this EMC model, ionized impurity scattering and phonon scattering, piezoelectric, deformation potential and intervalley scattering, are included. Impact ionization is generally considered to be one of the most important processes in the high-electric-field range and is usually treated as an additional scattering mechanism. At moderate voltages, carrier velocities eventually cease to increase with increasing electric field due to scattering by high-energy phonons, which is the so-called velocity saturation. A higher electric field will cause carrier acceleration to initiate the impact ionization process. When impact ionization occurs, electron–hole pairs are generated, the number of which is proportional to the product of the ionization coefficient and the current density. The impact ionization coefficient shows a strong dependence on the electric field, and increases sharply in the high electric field range. As reported in Ref. [11], weak impact ionization occurs around V_{ds} = 18 V in GaN HEMTs, and with higher V_{ds}, impact ionization becomes so frequent as to induce avalanche multiplication of carriers. The huge fluctuation of carrier density under high electric field will doubtless lead to noise increase at high drain bias.

As well as the impact ionization high-field effect, the severe short channel effect under high drain bias is also responsible for the noise increase. The reduction of L_g below 300 nm causes short channel effects like threshold-voltage shift, which originates in the poor confinement of the electrons in the 2DEG, reducing the modulation efficiency of the gate. On-wafer measurements of pinch-off characteristics were performed using an Agilent 4155A semiconductor parameter analyzer, and Table 1 shows the dependence on drain voltages, from which we can conclude that the pinch-off characteristics degrade rapidly for high drain voltages. Although our noise parameter measurement was carried out at fixed V_{gs} (–2 V), shift of the threshold voltage towards the negative direction of the half axis under high drain bias implies higher gate leakage current at the same gate voltage, and this was substantiated through measurements, as shown in Fig. 5. Gate noise current source related shot noise is proportional to the Schottky gate leakage current, and as a consequence, the augmenting I_g can also lead to NFmin increase.

In addition, the thermal effect under high voltages is also a contributor to the noise increase. Obviously, high drain bias results in a more and more severe self-heating effect in GaN HEMTs. Thus, the circuit-modeled parasitic resistances will generate more thermal noise, which causes the noise performance to deteriorate further under high drain voltages.

All these analyses encourage us to find new device structures or geometry to improve noise performance and suppress the increasing rate of NFmin under high voltages. For example, we should try to adopt GaN HEMTs with field-plate structures when designing GaN LNA MMICs. The Atlas device simulation tells us GaN HEMTs with source/gate field-plates can reduce the maximum electric field in the gate-to-drain gap, which can diminish the impact ionization effect under high voltages, thus suppressing the rapid increase in the noise value. It has been firmly proven that using field-plates in GaN HEMTs can effectively reduce the noise value[12, 13]. Other device structures, which help to suppress the short channel effect, diminish the self-heating effect or reduce gate leakage current, can all be employed to improve noise performance under high bias.

Table 1. Threshold voltage under different drain voltages with V_{gs} of –2 V.

V_{ds} (V)	V_{th} (V)
6	–2.7
10	–2.9
15	–3.3
20	–4
25	< –5

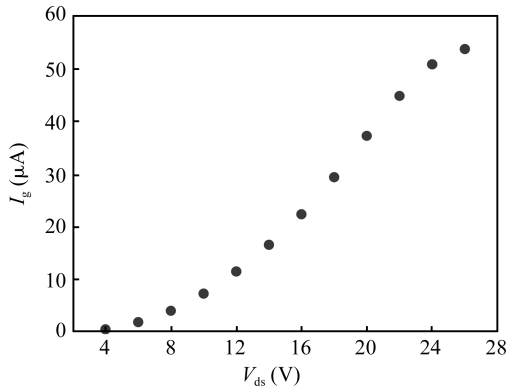

Fig. 5. Change of gate leakage current with drain–source voltage with V_{gs} of –2 V.

4. Conclusions

AlGaN/GaN HEMTs are displaying more and more advantages in both high power and low noise performance. The feasibility of fully integrated GaN transceivers shows great potential for next generation radar and base-station systems. However, a rapidly increasing noise value with high drain bias is one of the trickiest issues in the process of circuit integration. In our research, a reasonable explanation is demonstrated. Impact ionization, higher gate leakage current and a severe self-heating effect are responsible for the increasing noise value of GaN HEMTs under high bias. Correspondingly, new device structures like adoption of field-plates can reduce the noise value.

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