Low modulation index RF signal detection for a passive UHF RFID transponder

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Abstract: In a typical RFID system the reader transmits modulated RF power to provide both data and energy for the passive transponder. Low modulation index RF energy is preferable for an adequate tag power supply and increase in communication range but gives rise to difficulties for near-field conventional demodulation. Therefore, a novel ASK demodulator for minimum 20% modulation index RF signal detection over a range of 23 dB is presented. Thanks to the proposed innovative divisional linear conversion from the power into voltage signal, the detection sensitivity is ensured over a wide power range with low power consumption of 8.6 μW. The chip is implemented in UMC 0.18 μm mix-mode CMOS technology, and the chip area is 0.06 mm^2.

Key words: RFID; low modulation index; transponder

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1. Introduction

RFID technology has been implemented in many areas. Unlike the traditional barcode system, an item with an affixed RFID tag can be recognized by reading the data stored in the tag through a wireless link, rather than light. Thus the system's endurance and convenience are greatly improved. There has been great interest in UHF RFID tag research. Much effort has been made to reduce costs[1], enlarge the reading range[2] and integrate the tag with other functions (e.g., a temperature sensor)[3].

The tags mainly fall into two types: active and passive. Passive tags extract RF power induced on an antenna for their operation, instead of a battery. Therefore their cost and volume are reduced but the requirements for the power harvest system are increased. Communication data are also modulated on RF power. Usually for the forward link (reader to tag) the absence of RF energy denotes a bit "0" and for the rewards link (tag to reader) a bit "1" is represented by the tag connecting the antenna to the ground in order to backscatter most of the receiving power back to the reader. If the modulation index is 100%, there is no power available for the tag. To increase the communication range, the modulation index is adjusted lower than 100% to provide more energy for the tag at far-field. For the ISO 18000-6B protocol, the modulation depth is 30.5% or 100% and for type C it is 80%–100%[4]. However, low modulation index RF power increases difficulties in conventional demodulation based on envelope detection. Nonlinear envelope voltage signal extraction from the RF power makes the voltage-mode demodulation in the near field difficult to realize. The current-mode demodulation does not have this problem for linear conversion of RF power to the current signal[5], but linearly increasing the current consumption will cause a tag supply voltage collapse in the near field with large modulation depth input RF power, and so a large storage capacitor is necessary.

In this paper, a novel demodulator is presented for both high and low modulation index RF signals over a wide power range. An innovative divisional linear voltage demodulation method is implemented for low power consumption of 8.6 μW. Cross regional signal demodulations are achieved with an embedded ultra-small digital circuit. This paper also explains the tag architecture and the novel demodulation principle, and describes the demodulator circuit in detail.

2. Tag architecture and divisional linear voltage modulation

Figure 1 compares the traditional and the proposed tags. Usually the tag consists of the rectifier, the regulator, the demodulator, the oscillator, the reset and digital circuits. The traditional demodulator includes the rectifier, the voltage limiter, the peak detector and hysteresis comparator. The modulated RF power induced on the antenna is converted into a low frequency modulated voltage signal by the rectifier realized by stacked doublers known as a Dickson charge pump. As a result of variations in the received RF power level due to RF signal modulation and different reader-to-tag distances, there are huge fluctuations in the rectifier output voltage, and therefore a voltage limiter needs to be connected with the rectifier to avoid voltage overload and ensure the voltage signal is within the comparator input range. The inevitable adoption of the voltage limiter leads to a nonlinear conversion of power modulation into the modulated voltage signal. As shown in Fig. 2(a) when the tag is far from the reader the transformed modulated voltage signal is large enough for the demodulator to detect. But when the tag gets closer to the reader the signal becomes weaker and the S/N ratio drops sharply.

A current-mode demodulator[5] is developed to ensure a large modulated signal over the whole communication range

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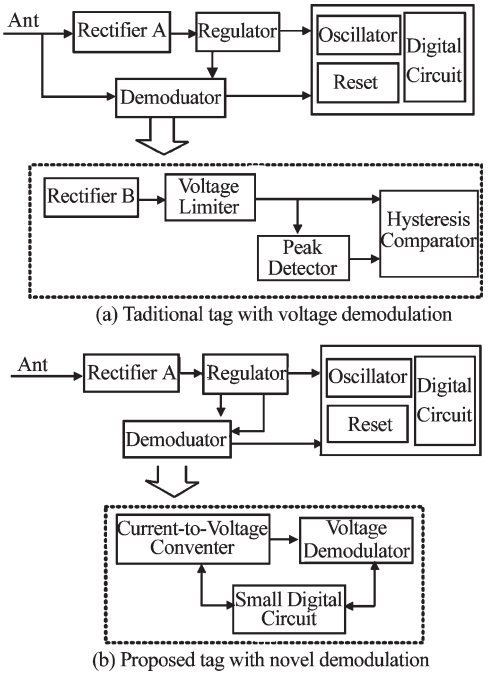

Fig. 1. Comparison between the traditional and proposed tags.

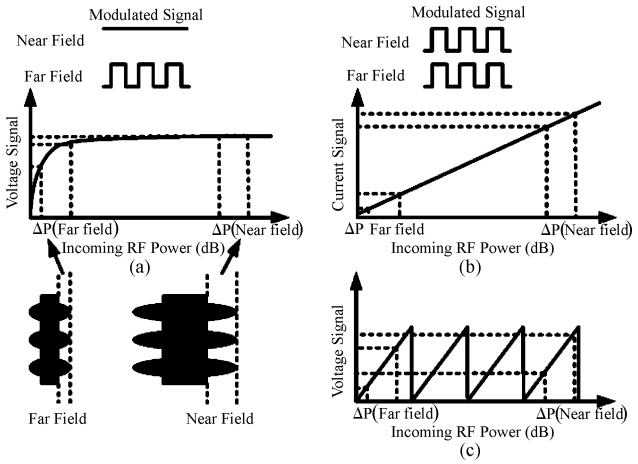

Fig. 2. Comparisons between three demodulation methods.

shown in Fig. 2(b). A current signal proportional to the incoming power is generated directly from the antenna. Nevertheless, as the tag approaches the reader, the current signal rises linearly with the receiving power, including the current consumption of the circuit processing the signal. The added power dissipation can be complemented by low modulation index RF energy. But for the power with a large modulation index, only a large capacitor can avoid supply voltage collapse for progressively increasing current consumption.

The proposed demodulator is shown in Fig. 1(b), which includes the current-to-voltage converter, the voltage demodulator and a small digital circuit. The embedded input current extraction circuit in the converter is a voltage clamp, also for coarse power regulation. The current in the clamp directly represents the power level and it is converted into the voltage signal as shown in Fig. 2(c). When the voltage reaches 1.3 V, it restarts from 400 mV. So the signal remains within the circuit operation range. The voltage demodulator compares the scaled peak hold voltage with the voltage signal to achieve the digital

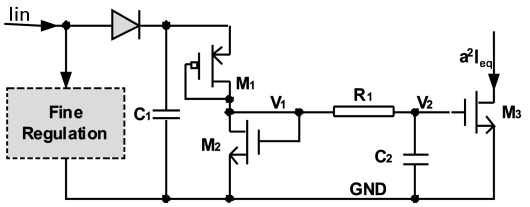

Fig. 3. Current extraction circuit.

signal. A small digital circuit is integrated in the demodulator for cross regional signal demodulation. The following section will describe the demodulator circuits.

3. Demodulator circuits

3.1. Current-to-voltage converter

A current extraction circuit is integrated in the current-to-voltage converter as shown in Fig. 3. The diode and MOS transistors M1–M2, form a voltage limiter connected with the charge pump output to ensure the output voltage remains almost constant, and thus I_{in} is linear to the RF energy. However, as the input RF power increases, a large RF noise current will appear in I_{in} and affect the demodulation. As a result, an RC filter formed by R_1 and C_2 is inserted between V_1 and V_2 to filter the noise. I_{eq} is an equivalent filtered current of I_{in} determined by V_2. The limiter is also the coarse regulation for the regulator. A smooth voltage supply is generated by further fine regulation.

A block diagram of the current-to-voltage converter is illustrated in Fig. 4. $\alpha^2 I_{eq}$, $\alpha^3 I_{eq}$, $\alpha^4 I_{eq}$, $\alpha^5 I_{eq}$ and $\alpha^6 I_{eq}$ are generated by V_2 biased different W/L NMOS transistors as shown in Fig. 3. I_{in} is estimated by comparing $\alpha^2 I_{eq}$, $\alpha^3 I_{eq}$, $\alpha^4 I_{eq}$, $\alpha^5 I_{eq}$ and $\alpha^6 I_{eq}$ with I_{ref} respectively through five simple current comparators to determine in which region I_{in} is located. The comparison results are sent to the digital circuit to control the switches formed by NMOS transistors M8–M11 and PMOS transistors M12–M16. If there are no sudden changes in In_{1-5}, Out_{1-5} follow In_{1-5}. Only one current path is allowed to be opened for saw-tooth current signal generation and thus there is a saw-tooth voltage signal across R_2 and R_3. The maximum current in M17 is lower than 800 nA. A hysteresis function is realized by adding a voltage demodulator output signal controlled current.

For power consideration, I_{ref} is set at approximately 120 nA and α is equal to 1/5. Every output voltage of the current comparator is compared with V_{ref} by a voltage comparator to sharpen the output signal. If I_{eq} is in a range of $\alpha^{-k} I_{ref}$ to $\alpha^{-(k+1)} I_{ref}$, comparison between I_{eq} and a current smaller than $\alpha^{-k} I_{ref}$ is unnecessary. Therefore, for reduction of power consumption, all the current and voltage comparators are controlled by the subsequent stage voltage comparator output except for the last stage. When the enabled signal is low the voltage comparator outputs low to disable the current and voltage comparators in the previous stage to ensure correct conversion.

3.2. Small digital circuit

The voltage comparator outputs In_1–In_5 are send to the

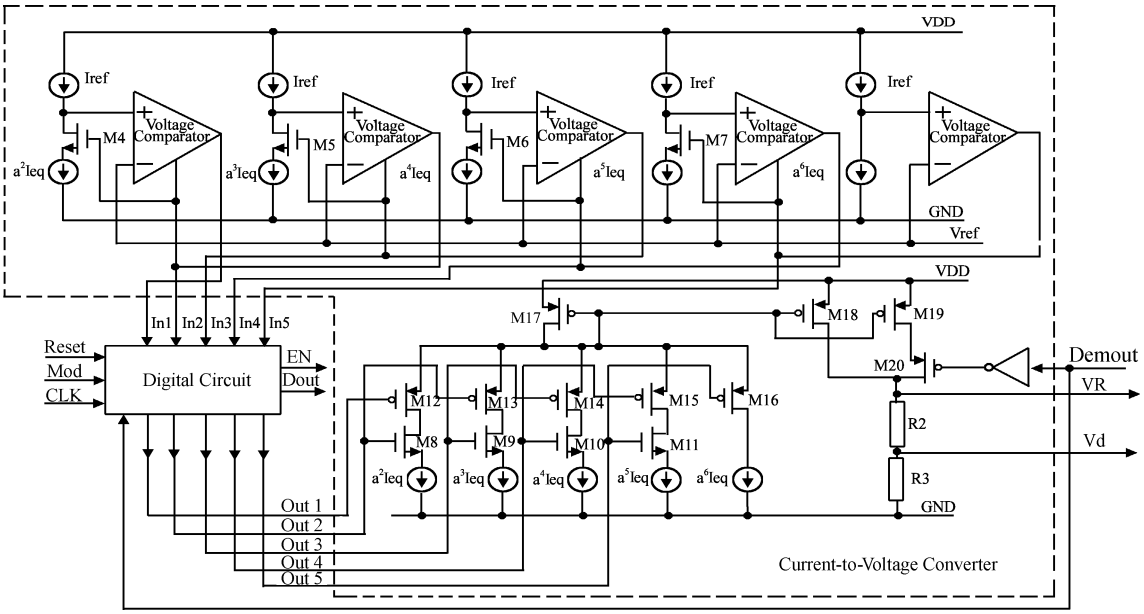

Fig. 4. Current-to-voltage converter.

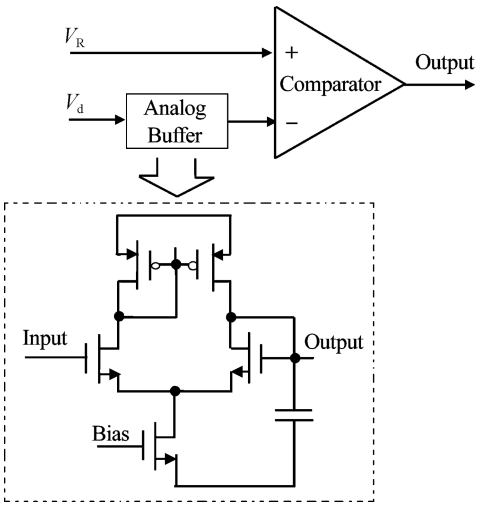

Fig. 5. Voltage demodulator.

digital circuit. If all of them remain unchanged after the clock up edge, Out_1–Out_5 are equal to to In_1–In_5 respectively. Otherwise a sudden change of In_1–In_5 represents the received data directly. In other words, I_{eq} changes across one of $\alpha^{-2}I_{ref}$, $\alpha^{-3}I_{ref}$, $\alpha^{-4}I_{ref}$, $\alpha^{-5}I_{ref}$ and $\alpha^{-6}I_{ref}$. Therefore, the demodulation can be accomplished by the current comparator directly. The digital circuit senses the direct demodulation and then powers off all the subsequent circuits to reduce power dissipation.

3.3. Voltage demodulator

Without direct demodulation the voltage demodulator is enabled by the digital circuit. Figure 5 shows the demodulator circuit. V_d is held by an analog buffer during the low power level. The analog buffer is a simple differential amplifier with a current mirror load and a capacitor. Its output is connected to the negative input thus achieving unit gain. Its output is compared with modulated V_R to achieve the signal transmitted by the reader.

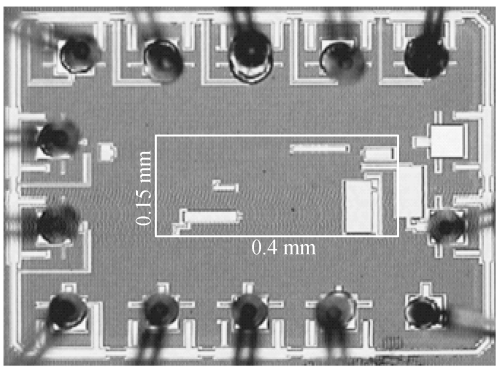

Fig. 6. Chip micro-photograph (die size 0.4×0.15 mm^2).

4. Measurement results

The chip is implemented in UMC 0.18 μm mix-mode CMOS technology and a photograph of it is shown in Fig. 6. Figure 7 shows a block diagram of the measurement setup. The supply voltage is 1.5 V and the input clock is 2 MHz which is typical for the ISO18000-6C tag. For cross division RF signal demodulation a higher clock frequency means higher precision. Connected with an external Dickson charge pump consisting of six Schottky diodes as the rectifier, Figure 8(a) shows V_R versus input 933 MHz RF power. Clearly a saw-tooth conversion is realized. However, as the input energy increases, the input impedance of the chip becomes smaller, as does the power-to-V_R gain. Figure 9 shows V_R and the demodulator output with –12 dBm and 11 dBm 20% modulation index input RF power. The receiving pulse width is 5 μs. Clearly, with the same modulation index, the converted voltage variation reduces as the input power increases, leading to a minimum 20% modulation index 933 MHz RF signal detection range of 23 dB. A simple and convenient method to obtain a larger demodulation range is to slowly increase the current ratio α in the near-field region and add more regions to eliminate the effect of chip impedance reduction. Another method is to insert

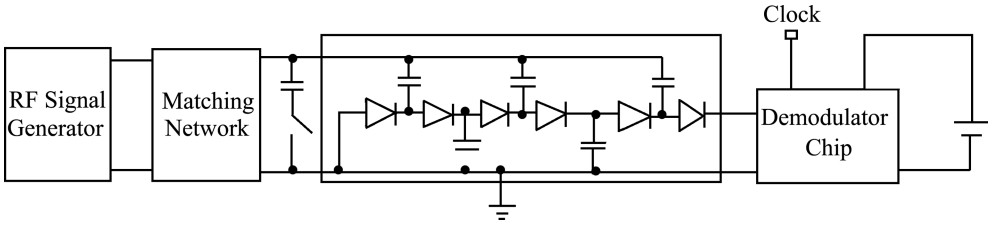

Fig. 7. Block diagram of the measurement setup.

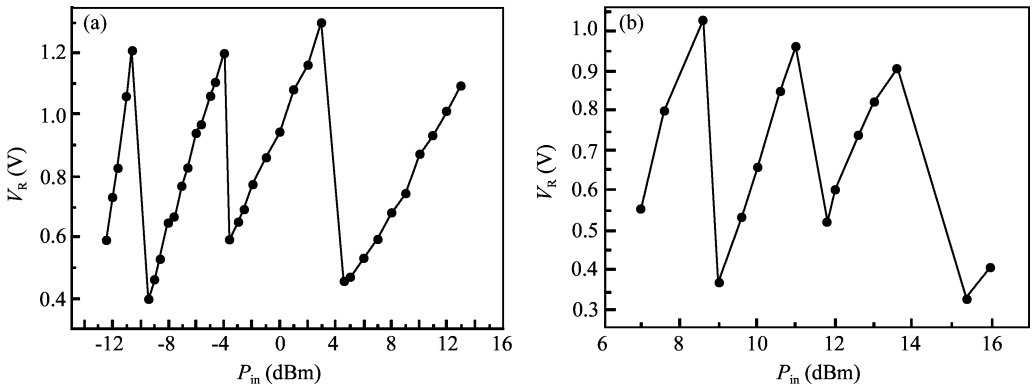

Fig. 8. V_R versus P_{in}: (a) Measurement without the capacitance; (b) Measurement with the capacitance.

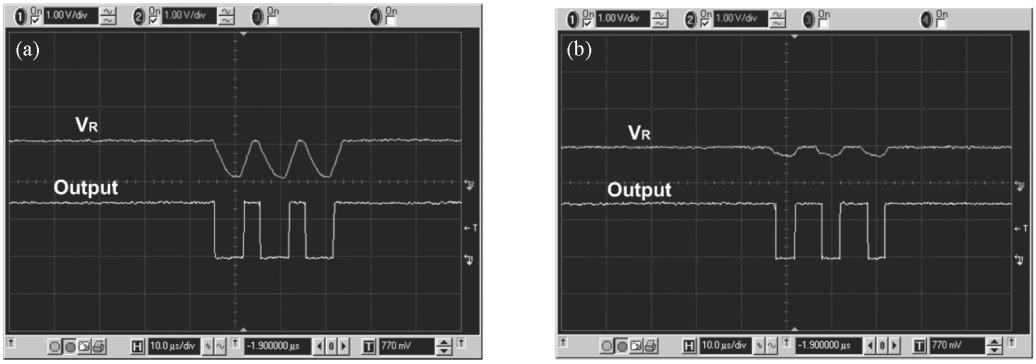

Fig. 9. V_R and the demodulator output waveforms: (a) 20%, –12 dBm RF power; (b) 20%, 11 dBm RF power.

Table 1. Performance summary for the demodulator.

Parameter	Value
IC size	0.06 mm^2
Supply voltage	1.5 V
Power consumption	8.6 μW
Modulation index (Min 20%)	23 dB

a parallel capacitance at the rectifier input to introduce mismatch for adjusting the power-to-V_R conversion region in the near-field as shown in Fig. 8(b). Table 1 summarizes the performance characteristics of the demodulator.

5. Conclusions

An ASK demodulator with an innovative divisional detection method for low modulation index signal over a wide power range is presented in this paper. The circuit is implemented in UMC 0.18 μm mix-mode CMOS technology. The measurement results show that a minimum 20% modulation index detection over a power range of 23 dB is achieved. The chip area is 0.06 mm^2 and the whole chip power consumption is 8.6 μW.

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