Effects of Si implantation on the total dose hardness of fully-depleted SIMOX wafers

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Abstract: Total dose hardened fully-depleted SOI materials are fabricated on separation by implanted oxygen (SIMOX) materials by silicon ion implantation and annealing. The I_D–V_G characteristics of pseudo-MOS transistors pre- and post-irradiation are tested with ^{60}Co gamma rays. The chemical bonds and the structure of Si in the buried oxide are also studied by X-ray photoelectron spectroscopy and cross-sectional high-resolution transmission electron microscopy, respectively. The results show that Si nanocrystals in the buried oxide produced by ion implantation are efficient deep electron traps, which can significantly compensate positive charge buildup during irradiation. Si implantation can enhance the total-dose radiation tolerance of the fully-depleted SOI materials.

Key words: SOI; fully-depleted; SIMOX; total dose radiation; Si nanocrystal
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1. Introduction

Thanks to the full dielectric isolation of individual transistors, silicon-on-insulator (SOI) integrated circuits (ICs) are completely immune to classic p–n–p–n latch-up. Moreover, the sensitive charge collection volume and p–n junction area of SOI devices limited by the buried oxide are considerably small as compared to bulk devices, giving them advantages over conventional bulk silicon ICs for single event upset (SEU) and high dose rate transient upset effects[1,2]. However, SOI devices are more susceptible to total dose effects because of the buried oxide layer which introduces an additional source of radiation-induced charge trapping. In particular, for fully-depleted SOI devices, whose top-gate transistor is electrically coupled to the back-gate transistor, radiation-induced charge buildup in the buried oxide of a fully depleted transistor will cause a decrease in the threshold voltage of the top-gate transistor[3]. Therefore, it is very important to improve the total dose hardness of fully-depleted SOI devices for space applications.

For fully depleted SOI devices, process techniques that reduce the amount of charge trapping in the buried oxide must be used. Previous work has proposed several process techniques for SIMOX wafers, such as ion implantation into the buried oxide[4], buried oxides formed using supplemental and multiple implants and anneal[5–7], lowering the oxygen implant dose and nitrogen implantation[8]. But many of these techniques are based on modifying the fabricating process of SOI wafers, which is unavailable from commercial SOI vendors. In this work, hardened fully depleted SOI samples are prepared by implanting silicon into the buried oxide followed by annealing with ultrathin commercial SIMOX wafers. A pseudo-MOSFET technique[9] is used to characterize the total dose response of the hardened and unhardened samples. The defects in the buried oxide introduced by excess Si are also studied by X-ray photoelectron spectroscopy (XPS) and cross-sectional high-resolution transmission electron microscopy (HRTEM).

2. Experiment

Commercial ultra-thin SIMOX wafers from the Shanghai Simgui Technology Company were used for the experiments, and the starting material was 4-inch p-type (100) Cz-Si wafers. The top Si film thickness was ~50 nm, and the buried oxide thickness was ~370 nm. The wafers were hardened by implanting Si into the buried oxide at a dose of 1×10^{15} cm^{-2}, and the implanted energy was 120 keV; then the hardened wafer was annealed at 950 °C for 2 h to repair the implanting damage of the top Si film. Si islands with square shapes (5×5 mm^2) on the buried oxide were defined by dry etching for measurement and irradiation. For a pseudo-MOSFET, two probes forming source and drain terminals were aligned with an inter-probe distance of 1 mm.

A ^{60}Co gamma ray source was used to perform biased irradiations at a dose rate of 25 krad(Si)/min. During irradiation, a positive voltage was applied to the Si substrate to create a biased electric field of 5×10^5 V/cm through BOX. I–V measurements were taken immediately after each dose using a HP4156C semiconductor parameter analyzer. The XPS experiment was performed by using a VG ESCALAB MK II spectrometer with MgKα X-ray radiation to study the chemical states of the Si-rich buried oxide by Si ion implantation. The microstructures of the hardened SIMOX material were

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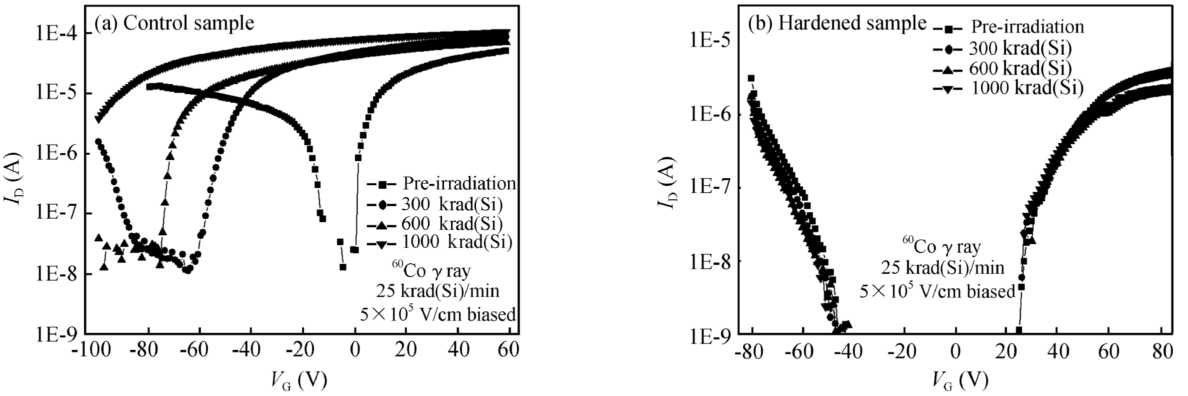

Fig. 1. I_D–V_G characteristics of the pseudo-MOS transistor for (a) control sample and (b) hardened sample after irradiation to 1000 krad(Si) with ^{60}Co γ-ray, V_{DS} = 0.1 V for this measurement.

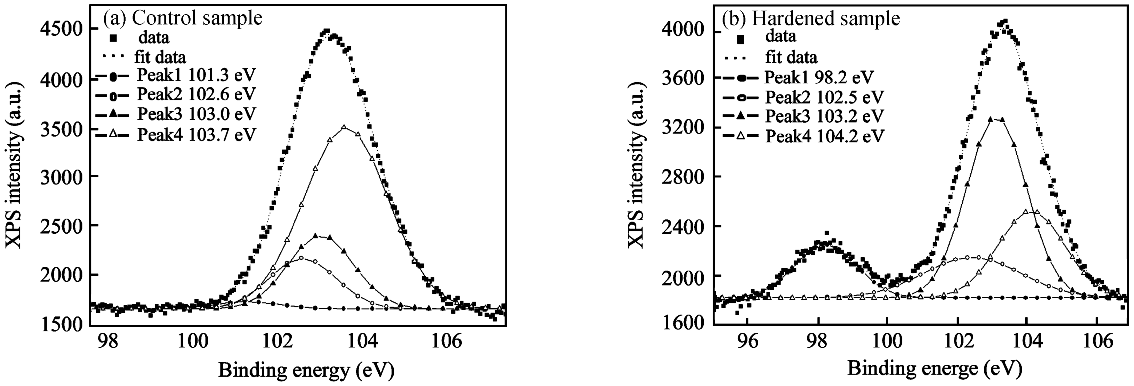

Fig. 2. Si2p core-level spectra for (a) the control sample and (b) the hardened sample.

also studied by JEM-2010 HRTEM.

3. Results and discussion

The drain current versus gate voltage characteristics of the pseudo-MOS transistors are shown in Fig. 1 in a semi-logarithmic plot for V_{DS} = 0.1 V as the back gate voltages scan from negative to positive. For the control sample (without Si implantation) before irradiation, Figure 1(a) shows that the accumulation regime of a pseudo-MOS transistor behaves like a pMOSFET (negative bias), whereas in the inversion regime (positive bias) it behaves like an nMOSFET. Only nMOSFET curves are focused to simplify the evaluation of the radiation induced back channel threshold voltage shift.

As shown in Fig. 1(a), the *I*–*V* curves of the pseudo-MOS transistor show large negative shifts during irradiation for the control sample. The total threshold voltage shift for an nMOSFET is the sum of the threshold voltage shifts due to radiation induced oxide trap and interface trap charges. For SIMOX wafers, interface trap buildup can be neglected compared to oxide trapped charges for the radiation levels of this experiment[10]. Gamma rays can generate high densities of electron-hole pairs in the buried oxide, and electrons escaping initial recombination will rapidly drift toward the substrate at the bias of electric field. However, many of the holes will be trapped in the bulk of the oxide[10], forming a net positive oxide trapped charge that causes negative threshold voltage shifts of the back-gate transistors. For control sample, there is a large positive charge buildup in the buried oxide with irradiation; even at a dose of 300 krad(Si), the drain current of the nMOSFET is saturated at 0 V gate voltage that will seriously affect the top gate transistor. But for the hardened sample, small shifts of the nMOSFET characteristic are observed with irradiation, as illustrated in Fig. 1(b). Compared with the control sample, the hardened sample by Si implantation and annealing greatly reduces positive radiation induced charge buildup in the buried oxide.

XPS experiments were performed to study the chemical states of the Si-rich buried oxide by Si ion implantation. Figures 2(a) and 2(b) show the XPS Si2p core level peaks for the control sample and hardened sample, respectively. Our procedure was based on the use of five Gaussian-shaped peaks of Si^{n+} (n = 0, 1, 2, 3, and 4) to simulate the five silicon oxidation states in the buried oxide. The peak near 98.2 eV binding energy is due to photoelectrons from the Si2p core-level transition in element Si (Si^0) and the peak near 104.1 eV is attributed to SiO_2 (Si^{4+})[11, 12]. For the control sample shown in Fig. 2(a), Si^{4+} is the dominant component and no Si^0 exists in the buried oxide. There is an obvious peak at 98.2 eV which corresponds to Si^0 shown in Fig. 2(b), indicating that element Si and SiO_2 co-exist in the buried oxide of the hardened sample. These structure defects produced by Si implantation in the buried oxide are probably the primary reason for the reduced positive charge buildup during irradiation.

Figure 3 is the cross-sectional HRTEM image of the hardened SIMOX material. From Fig. 3(a), it seems that the

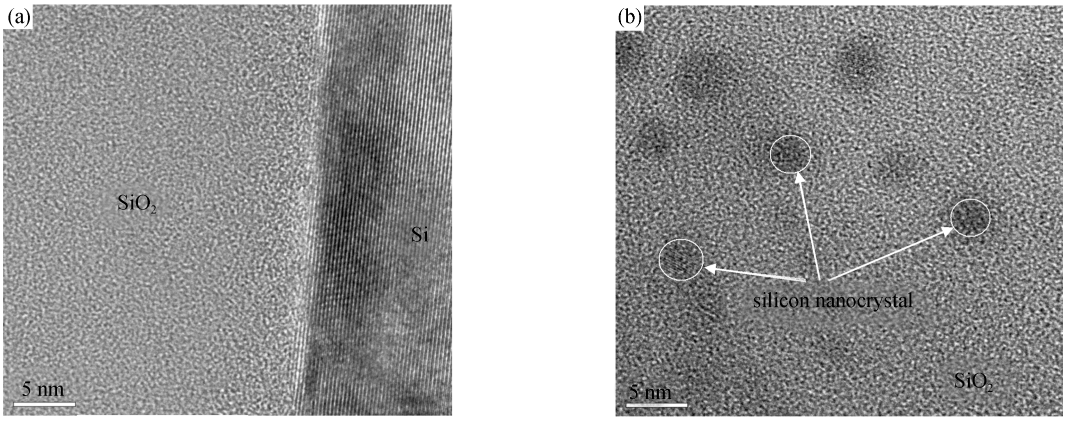

Fig. 3. Cross-sectional high-resolution TEM image of the hardened sample. (a) Top Si film and Si/BOX interface; (b) Si nanocrystals in the BOX layer.

interface of top silicon film and buried oxide is still steep and uniform after silicon implantation plus high temperature annealing, and the silicon film also has a good single crystal structure, indicating that the ion implantation damage can be greatly reduced by the annealing process. In addition, the integrity of amorphous SiO$_2$ near the top Si/SiO$_2$ interface shows that silicon implantation has little influence on it, possibly due to the large distance between the interface and the location of the implanted Si peak. But some dark points are observed in the amorphous buried oxide at a depth of around the implanted Si peak (Fig. 3(b)). These point defects in the SiO$_2$ matrix have crystal lattice structure, with an average size of 3–4 nm. Obviously these Si nanocrystals correspond to Si^0 in Fig. 2(b). No nanocrystals were observed at the depth of the Si implanted range in the buried oxide. So the effect of the hardening process is that Si nanocrystals are formed near the location of the Si implantation peak. Previous work[13] has calculated the energy states of various structural defects introduced by Si implantation, showing that they have ground and excited energy states that lie within the energy gap of amorphous SiO$_2$. Garrido *et al.*[14] studied the optoelectronic properties of Si nanocrystals embedded in SiO$_2$, and attributed the photoluminescence to the quantum confinement effect of carriers in nanocrystalline-sized Si structures. Therefore, Si implanted followed by annealing produced Si nanocrystal defects in the buried oxide that can act as electron traps. Once the hardened sample is irradiated by gamma rays, electrons can also be trapped by Si nanocrystals and recombined with the radiation generated holes. Thus the net positive charge buildup in the buried oxide will be reduced by electron compensation. Small shifts of nMOSFET threshold voltage are observed in Fig. 1(b), indicating that the Si nanocrystal defects in the buried oxide are efficient deep electron traps with large capture cross-section.

4. Conclusions

Total dose hardened fully-depleted SOI materials were fabricated on SIMOX materials by silicon ion implantation into the buried oxide layer followed by annealing. The total dose radiation effects of the hardened and control material were studied by ^{60}Co gamma ray irradiation. The results show that the threshold voltage shifts of the pseudo-MOS transistor are greatly reduced for the hardened material. An XPS experiment and HRTEM study indicate that Si nanocrystals produced by excess Si are probably responsible for this improved radiation hardness. They are efficient deep traps in the buried oxide, and can compensate the trapped positive charge when filled during irradiation. Small threshold voltage shifts of the pseudo-MOS transistor are due to the reduced positive charge buildup in the buried oxide.

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