A time-domain digitally controlled oscillator composed of a free running ring oscillator and flying-adder

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Abstract: A time-domain digitally controlled oscillator (DCO) is proposed. The DCO is composed of a free-running ring oscillator (FRO) and a two lap-selectors integrated flying-adder (FA). With a coiled cell array which allows uniform loading capacitances of the delay cells, the FRO produces 32 outputs with consistent tap spacing for the FA as reference clocks. The FA uses the outputs from the FRO to generate the output of the DCO according to the control number, resulting in a linear dependence of the output period, instead of the frequency on the digital controlling word input. Thus the proposed DCO ensures a good conversion linearity in a time-domain, and is suitable for time-domain all-digital phase locked loop applications. The DCO was implemented in a standard 0.13 μm digital logic CMOS process. The measurement results show that the DCO has a linear and monotonic tuning curve with gain variation of less than 10%, and a very low root mean square period jitter of 9.3 ps in the output clocks. The DCO works well at supply voltages ranging from 0.6 to 1.2 V, and consumes 4 mW of power with 500 MHz frequency output at 1.2 V supply voltage.

Key words: all-digital phase-locked loops; clock generator; digitally controlled oscillator; flying-adder; free-running ring oscillator

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1. Introduction

All-digital phase-locked loops (ADPLLs) are widely used as clock generators in a variety of systems, such as high-performance microprocessors[1], bluetooth radios[2] and mobile phones[3]. One of the critical components in the ADPLL is a digitally controlled oscillator (DCO). Currently there have been several approaches reported so far to realizing the digital control of the oscillators, such as: digitizing the oscillator current[1], selecting the numbers of the delay cells[4], digitizing the MOS varactors[5], and selecting continuously the multiphase outputs of ring-delay lines[6]. Most of those approaches, however, require a large chip area to achieve good conversion linearity with the DCO[1,4,5]. This is because the conversion linearity is usually determined by the symmetry between the components of the DCO, and the degree of symmetry is directly proportional to the component area. A large chip area can be avoided by using the multiphase outputs of the ring-delay-line[6], resulting in a large output jitter and MUX glitch in the pulse selector. The jitter can be reduced through a free-running ring oscillator with a coiled layout topology, and the glitch can be eliminated by adding a flying-adder (FA) logic[7]. A DCO composed of the FA logic and a multiphase analogue phase-locked loop has been recently proposed to produce an improved linearity and monotonic tuning curve[8]. However the output frequency range of the DCO is limited considerably due to the addition of the FA logic.

On the other hand, a time domain DCO is more preferable for ADPLL applications compared to a phase domain one. In the phase-domain ADPLL, the signal is first converted to be time-domain and then back to phase-domain. This conversion process needs additional chip area and power, and deteriorates the gain linearity of the ADPLL. At the same time, there are also some benefits for the ADPLL to operate in the time domain just as in the phase domain[9]. For example it can produce a precise frequency clock as output.

In this paper, we propose a DCO consisting of a free-running ring oscillator (FRO) and a flying-adder (FA). The FRO is designed to generate the reference clock signals for the FA logic. The FA logic uses the multiphase to produce the new frequency output. Two lap selectors are adopted into the FA to widen the output frequency range. Experimental results show the proposed DCO consumes less power and chip area, allows lower supply voltages and requires no additional passive components compared to previous ones, and thus is very suitable for time-domain ADPLL applications.

2. DCO architecture

Figure 1 shows a block diagram of the proposed DCO architecture, which is composed of an FRO and an FA. Two lap selectors are integrated in the FA. The FRO is able to output the reference clocks with consistent tap space thanks to a non-sequent layout array. The FA uses the outputs from the

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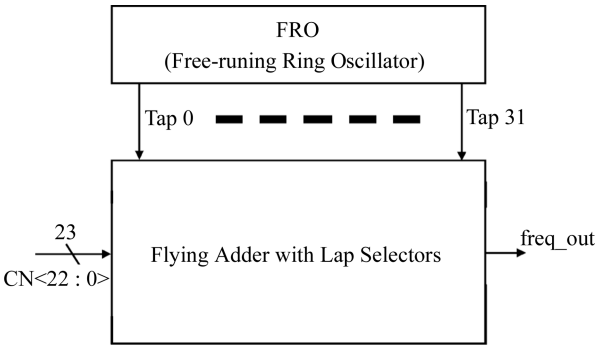

Fig. 1. Schematic architecture of the proposed digitally controlled oscillator.

FRO to generate the outputs of the DCO according to the digital controlling word inputs. This results in a dependence on the output period, instead of the frequency linearly on the digital controlling word input. Thus the proposed DCO promises a good conversion linearity in a time-domain, and is suitable for applications in the time-domain all-digital phase locked loops.

2.1. Free-running ring oscillator

The FRO designed in this work is composed of 16 differential delay cells as shown in Fig. 2, with (a) a delay cell array and (b) circuit of a delay cell, where M1 is for power down. One of the critical issues addressed in the layout implementation of FROs is that the outputs have to be brought to the FA's inputs in equal lengths, or delays. Any mismatch will show up as deterministic jitter on the frequency synthesizer's output. In a traditional FRO layout configuration shown in Fig. 2(c), where only four differential delay cells are drawn for illustration purposes, the delay cells distribute in a sequent chain. This configuration makes the task of bringing the FRO outputs to the FA easy, but the wire connection lengths between the connected cells are not equal, e.g, the connection from cell 4 to cell 1 is longer than the other connections. This unequal connection causes significant delay mismatch between the cells. The mismatch gets worse with increasing cell number. On the other hand, in the configuration used in this work shown in Fig. 2(a), the cells are in a coiled arrangement [8]. The coiled cell array ensures equal-length connections between the connected cells, allowing consistent tap spaces.

Moreover, the FRO has a better phase noise trait than the voltage controlled oscillator (VCO) used in conventional DCOs since it does not have a controlling input. In this design, each tap clock in the FRO is delayed by approximately 45 ps from its progenitor, resulting in an oscillator frequency of about 690 MHz in a typical corner, with the tap spacing being the highest resolution of the DCO.

2.2. Flying-adder

The structure of the proposed FA is shown in Fig. 3. The architecture is comprised of two almost identical blocks PATH_A and PATH_B, as well as a 2 to 1 MUX and a D flip-flop (DFF). The basic principle of the two-path FA is as follows[7]. PATH_A and PATH_B select the corresponding outputs from the FRO to trigger the DFF. The MUX decides which of PATH_A and PATH_B does the triggering. PATH_A is composed of a 32 to 1 MUX, a 19-bit adder, a 19-bit register, 5-bit register, an AND, and a lap selector (LS). PATH_B is composed of a 32 to 1 MUX, a 5-bit adder, two 5-bit registers, an AND, and an LS. The inputs to the MUXs are the 32 outputs of the FRO. We will refer to these outputs as 32 ticks. The right period is generated by using the right tick at the right time to trigger the DFF. In order to select any of the 32 ticks, 5 bits are needed for the MUXs' address decoding. Additional fractional bits are needed if we want to generate all the periods in a certain range with a certain accuracy.

These two paths are interlocked through the two AND gates and the MUX gate. When PATH_A is enabled (CLK1 is 1), the rising edge from the MUX output can be sensed by the DFF. Meanwhile, PATH_B is disabled at this time. In contrast, when PATH_B is enabled, PATH_A is disabled. The locking status of the two paths will be toggled from ON to OFF or from OFF to ON because the DFF toggles from 1 to 0 or from

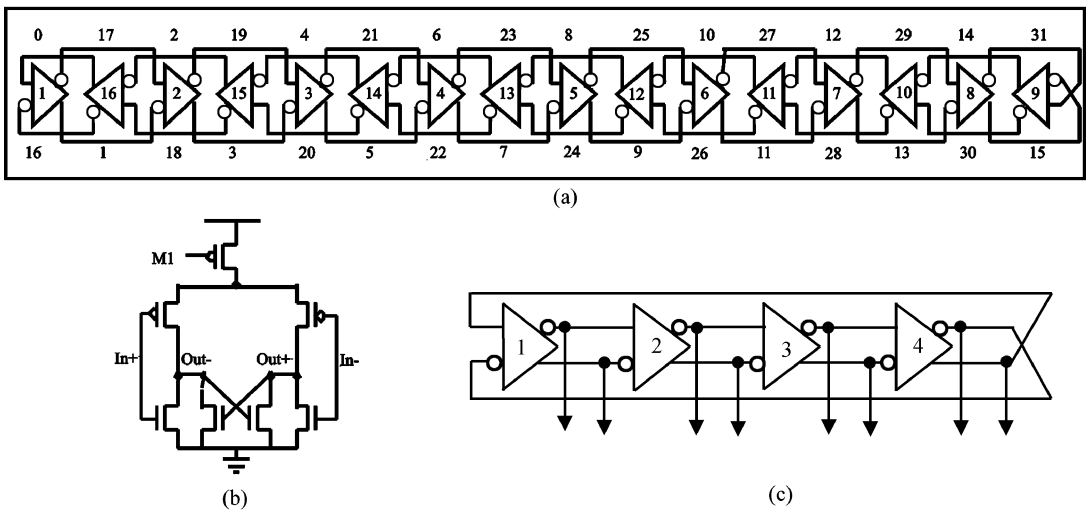

Fig. 2. Layout configurations of the free-running ring oscillator (FRO): (a) Delay cell array; (b) Circuit of a delay cell; (c) Conventional chain cell array.

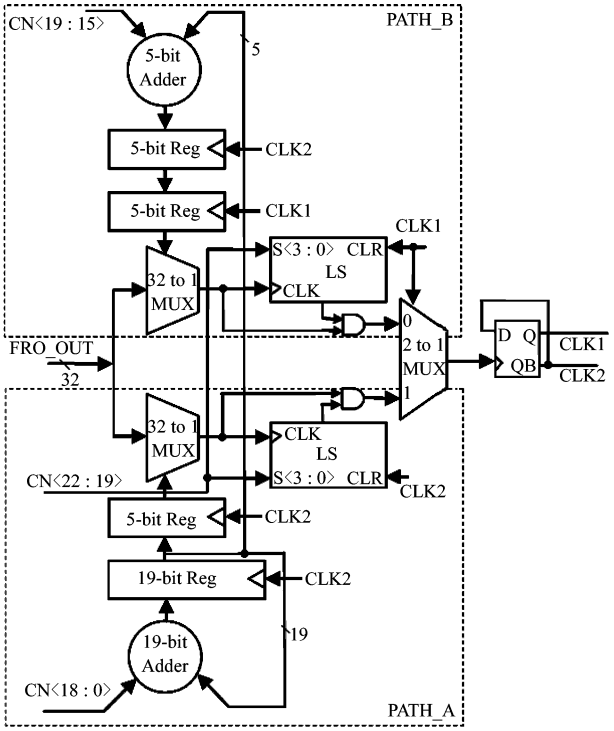

Fig. 3. Structure of the proposed FA logic.

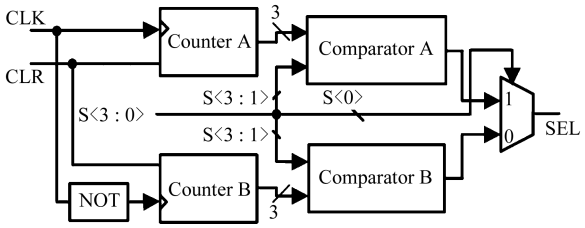

Fig. 4. Structure of the proposed lap selector.

0 to 1. These two paths will continually work together to generate the output waveform. The falling edge of CLK1 will be generated by PATH_A; the rising edge will be generated by PATH_B.

In order to overcome the frequency range limitation caused by the addition of the FA[7], two LSs are integrated in the FA to enlarge the DCO conversion range by selecting the lap of the output clock of the 32 to 1 MUX.

Figure 4 shows the structure of one lap selector. The lap selector tallies the cycles (laps) of the CLK and enables SEL signal when the number of the CLK cycles matches the input S⟨3:1⟩ data. Two counters are used to correctly tally the CLK laps, and the signal CLR is asynchronous. The counter A tallies the laps at the CLK rising edge and the counter B tallies the laps at the CLK falling edge. The 2→1 MUX on the right side of the circuit is used to select one of the two available comparator outputs. The value of the signal S⟨0⟩ is related to the falling edge of CLR when S⟨0⟩ = '1', and CLR toggles between point A and B. When S⟨0⟩ = '0', CLR toggles between point B and C. The relationship between CLR and S⟨0⟩ in the lap selector is shown in Fig. 5.

The timing diagram of the flying-adder is shown in Fig. 6. In order to describe concisely the operation of the flying-adder, we assume the FRO in Fig. 5 has four phase outputs. The

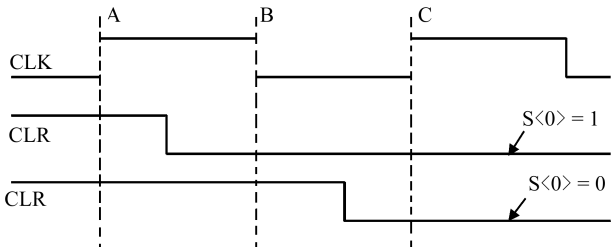

Fig. 5. Relationship between CLR and S⟨0⟩.

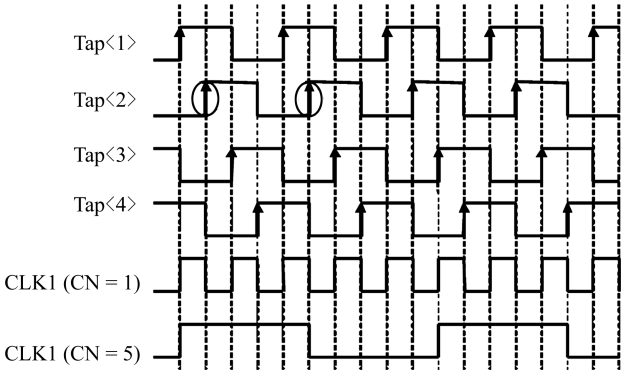

Fig. 6. Timing diagram of the FA.

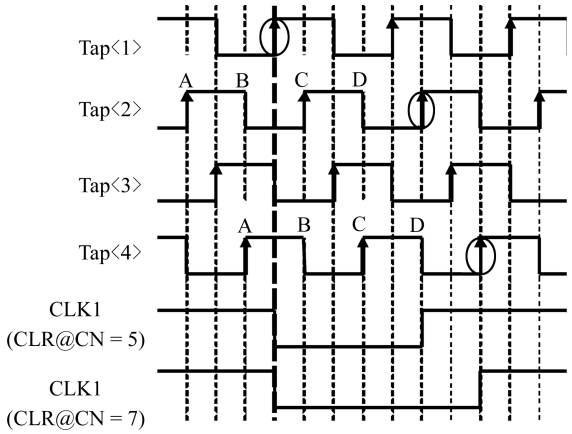

Fig. 7. Generation of the CLK1 for different CN values.

period of the output clock T is determined by the product of the DCO input control number CN and the unit delay of the delay cell, i.e., the delay of the two adjacent phases Δ. Thus, we have

$$T = \mathrm{CN} \times 2\Delta.$$

With a coiled cell array which allows uniform loading capacitances of the delay cells, the FRO produces consistent tap spacing outputs for the FA as reference clocks. The FA can make the period of the output clock be directly proportional to the controlled words. Thus, the DCO has good conversion linearity.

The initial selected tap is Tap⟨1⟩ with CN = '1' and the rising edge of Tap⟨2⟩ is chosen to be the falling edge of the output clock. When CN = '5', the initial tap is still Tap⟨1⟩, but the falling edge of the output clock is at the second rising edge of Tap⟨2⟩ since the lap selector set the output of the AND gate to zero to prevent the first rising edge of Tap⟨2⟩ from passing through.

Figure 7 demonstrates the generation of the CLK1 for

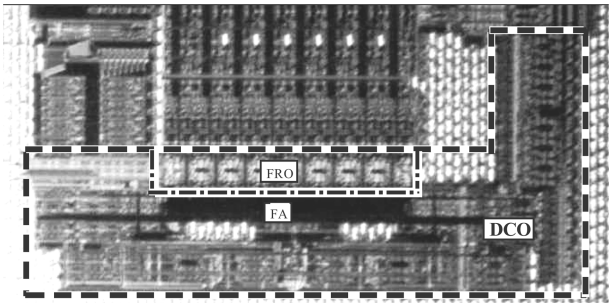

Fig. 8. Chip photomicrograph of the DCO.

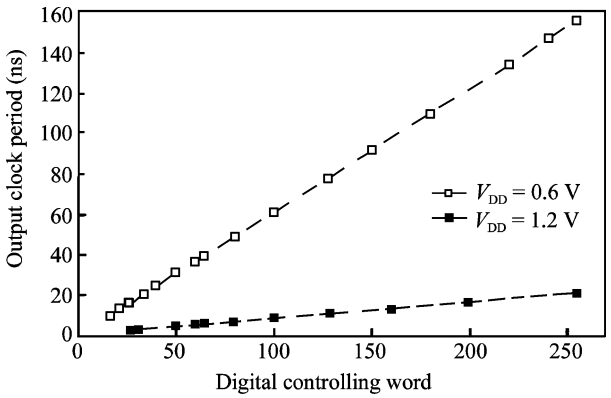

Fig. 9. Measurement result of the output CLK period versus control number.

different CN values. In the flying-adder shown in Fig. 3, signals CLR, CLK and S⟨3:0⟩ of the LS are connected to CLK1, the output of the 32 to 1 MUX, and CN⟨22:19⟩, respectively. When CN = '5', the control number CN⟨22:18⟩ of the flying-adder is equal to '00101' for four output taps of the FRO. The bottom tap selector of the flying-adder chooses Tap⟨1⟩ and Tap⟨3⟩ alternately if Tap⟨1⟩ is initially selected. The top tap selector would alternately choose Tap⟨2⟩ and Tap⟨4⟩, as explained in Ref. [8]. Upon the arrival of the first rising edge of Tap⟨1⟩, CLK1 changes to '0' in between B and C of Tap⟨2⟩. The signal Tap⟨2⟩ is low because CN⟨19⟩ is '0' and the counter B in the LS is selected to count the laps. When CN = '7', the control number CN⟨22:18⟩ of the flying-adder is equal to '00111' for the FRO with four output taps. Now the counter A of the lap-selector is selected to count the laps because CN⟨19⟩ is '1'.

Therefore, it is seen from the above description that the lap selector causes the FA to output lower frequency and thereby enlarge the frequency range.

3. Experimental results and discussion

The proposed DCO was fabricated in SMIC (Semiconductor Manufacturing International Corporation) standard 0.13 μm CMOS process. Figure 8 shows the chip micrograph of the fabricated DCO, which occupies 0.018 mm^2. Figure 9 shows the measured conversion curve of the fabricated DCO. It is seen that an excellent linearity in the DCO gain is achieved. The CLK period, in ns, instead of the conventional frequency in MHz, is used for the Y axis in the DCO gain curve since this DCO is designed for ADPLL applications

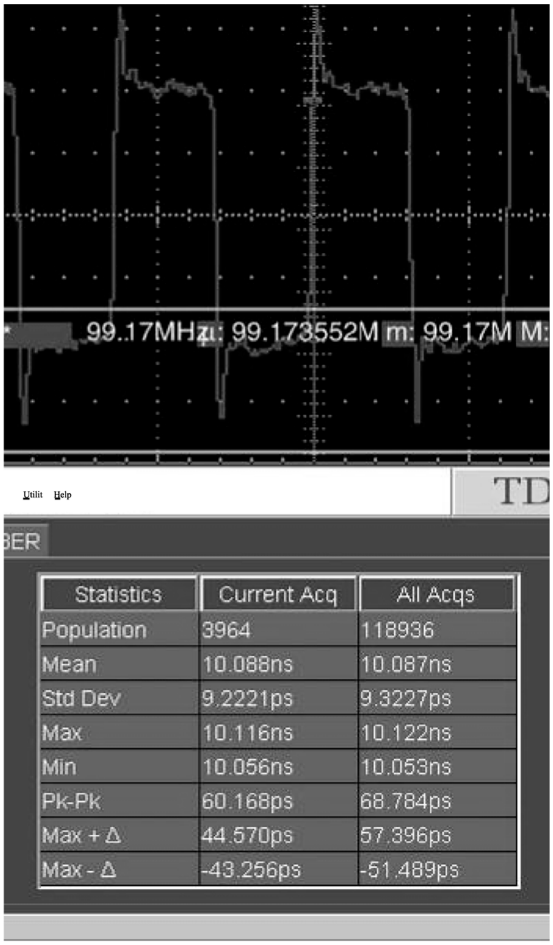

Fig. 10. Standard deviation jitter measurement of the DCO output.

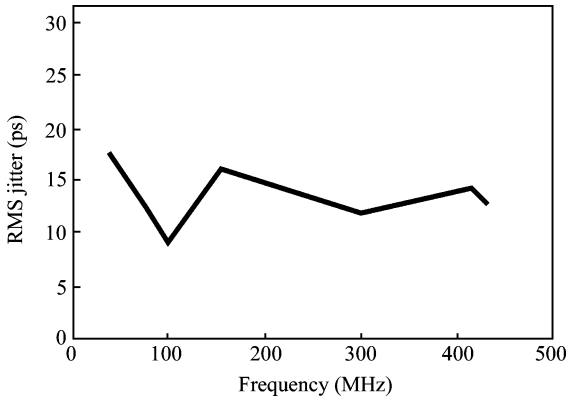

Fig. 11. Jitter performance over different output frequencies.

where the time resolutions of both the time-to-digital converter (TDC) and the DCO are determined by the common FRO. The measurement also verified that the DCO works well at a wide supply voltage range from 0.6 to 1.6 V. The output clock frequency range of the DCO is measured to be from 47 to 510 MHz at 1.2 V and from 6.4 to 101.2 MHz at 0.6 V. The output clock RMS jitter measured by Tektronix TDSJIT3 jitter analyzer is 9.3 ps at 100 MHz, as shown in Fig. 10. Figure 11 shows the jitter performance over different output frequencies.

The main experimental results with the proposed DCO are listed in Table 1. Included also are those reported previously by other groups[4, 5, 8, 10]. It can be seen the proposed DCO in this work has in general a notable improvement in

Table 1. DCO performance comparison.

Work	This design	Ref. [4]	Ref. [5]	Ref. [8]	Ref. [10]
Process (μm)	0.13	0.35	0.35	0.35	0.13
Supply voltage (V)	0.6–1.2	3.3	3.3	3.3	1.2
Power consumption (mW)	4 @ 500 MHz	100 @ 450 MHz	18 @ 200 MHz	< 180	16
Chip area (mm^2)	0.018	< 0.7	0.04	< 1.8	0.0484
DCO output frequency (MHz)	47–510 @ 1.2 V	45–450 @ 3.3 V	18–214 @ 3.3 V	10–80 @ 3.3 V	1.6–880 @ 1.2 V

performance and properties compared to the others. Compared with the DCOs in Refs. [4, 5, 8, 10], this DCO has lower power consumption, since this DCO with the FRO and FA structure represents more of a refinement over the other DCOs.

4. Conclusion

A new time-domain DCO has been proposed and experimentally demonstrated in this work. The DCO is composed of a flying-adder and an FRO. The experimental results show that the DCO has a wide output frequency range and an excellent conversion linearity with gain variation of less than 10%. It functions well with a low jitter performance in a wide supply voltage range from 0.6 to 1.6 V. With these confirmed benefits, the proposed DCO is very attractive for high speed time-domain ADPLL applications.

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