A dual-band reconfigurable direct-conversion receiver RF front-end*

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Abstract: A dual-band reconfigurable wireless receiver RF front-end is presented, which is based on the direct-conversion principle and consists of a low noise amplifier (LNA) and a down-converter. By utilizing a compact switchable on-chip symmetrical inductor, the RF front-end could be switched between two operation frequency bands without extra die area cost. This RF front-end has been implemented in the 180 nm CMOS process and the measured results show that the front-end could provide a gain of 25 dB and IIP3 of 6 dBm at 2.2 GHz, and a gain of 18.8 dB and IIP3 of 7.3 dBm at 4.5 GHz. The whole front-end consumes 12 mA current at 1.2 V voltage supply for the LNA and 2.1 mA current at 1.8 V for the mixer, with a die area of 1.2×1 mm^2.

Key words: RF; CMOS; reconfigurable receiver; direct-conversion; switchable inductor
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1. Introduction

Wireless communication has exploded in the last ten years, and may grow faster in the future. This has resulted in many different standards for various wireless applications. For example, there are GSM, CDMA, WCDMA and TD-SCDMA standards for cell phone applications, and IEEE 802.11a/b/g standards for wireless local area network (WLAN) applications. To lower product cost and ease switching between different wireless communication standards, reconfigurable transceivers which can support more than one standard have become a hot issue recently[1]. Multi-band multi-mode operation is one of the key requirements for reconfigurable wireless transceivers, and it brings many severe challenges to the implementation of reconfigurable RF front-ends. References [2–4] present some implementations of dual-band transceivers for various applications, but actually only the IF baseband processing blocks are shared between dual-band operations; the critical RF blocks (such as the LNA and PA preamplifier) only work for one specific operation band, not reconfigurable ones. This architecture may achieve an excellent performance, but it would consume a great deal of power and die area.

Reference [5] presents a reconfigurable multiband wireless receiver RF front-end, and the critical RF blocks are all shared among the different operation bands, but it consists of many on-chip inductors in the mixer.

In this paper, a dual-band reconfigurable wireless receiver RF front-end is presented. The receiver RF front-end is based on the direct-conversion principle and consists of a low noise amplifier (LNA) and a down-converter. By utilizing a compact switchable on-chip symmetrical inductor, all the blocks are shared and the RF front-end can be switched between two operation frequency bands without extra die area cost. Due to the sharing of all these blocks, the die areas are largely lowered, which will be more obvious when the front-end supports more than two bands. This RF front-end has been implemented in the 180 nm CMOS process and the measured results show that it works very well and only consumes a small die area.

2. Circuit design

2.1. Topology of the two-stage LNA

A low noise amplifier is the first stage of the receiver, and therefore the noise performance and the power gain should be carefully considered. For a cascade receiver system, an LNA with sufficient gain can lower the noise contribution of subsequent blocks such as the down-converter. Meanwhile, implementation of the input impedance matching in each operation frequency band is a great challenge since it is difficult to control the input impedance with the insertion of the switch.

Comparing two popular LNA topologies, the source degeneration common-source cascode amplifier can achieve better performance than the common-gate amplifier in a single band application, better input impedance matching, lower noise figure and higher power gain with the same power consumption. But in a dual-band application, a switch is needed to change the operation bands. The insertion of the switch in the input node of the common-source cascode amplifier would worsen the noise performance of the LNA a lot, especially in high frequency bands[6, 7].

The traditional common gate LNA can reach input matching in a wideband, but this will change in the high frequency range, and its noise performance is worse than the common source ones. So an improved common-gate amplifier is utilized in our work, with a positive feedback loop added to

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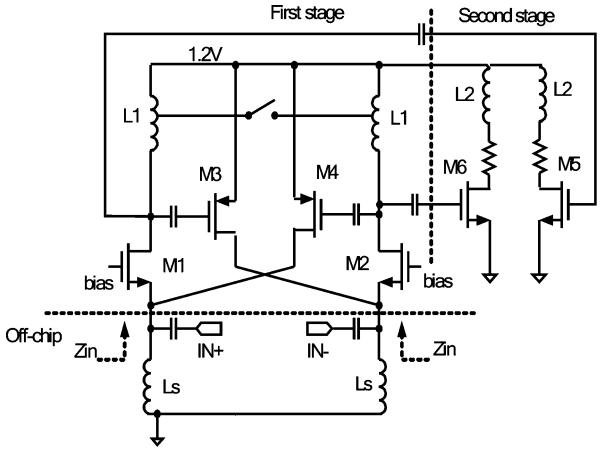

Fig. 1. Schematic of the presented LNA.

realize the switchable input impedance matching and the output load resonance at the same time[8, 9], as shown in Fig. 1. The LNA consists of two stages: the first stage is dual-band reconfigurable and provides some gain to lower than the noise contribution from the following circuits. The input impedance is coupled with the load by utilizing the cross coupling pair M3/M4 and could achieve 50 Ω real impedance in two frequency bands; this principle will be explained in more detail in the next section. The second stage is a wideband amplifier to provide the extra gain. Because the insertion of the control switch is not at the input nodes, the influence of the dual-band on noise performance is lower than the common source amplifier. The bias can also be carefully optimized to reach better linearity and noise performance.

2.2. Input matching

Impedance matching is very important in high frequency circuits, so the input impedance of LNA should match 50 Ω. In contrast to the common source amplifier, the input matching of this common gate amplifier with positive feedback is tight to the load impedance of the first stage. Through a cross coupling pair, the input impedance can be described by

$$Z_{\text{in}}=\frac{1}{g_{\text{m1}}(1-g_{\text{m2}}Z_{\text{load}})}, \tag{1}$$

where Z_{in} and Z_{load} are the input and load impedance of the LNA's first stage, g_{m1} is the transconductance of M1 and M2, while g_{m2} is that of M3 and M4. Z_{load} will become a real value when the load LC tank resonates, then Z_{in} can be adjusted to 50 Ω by controlling the value of g_{m1} and g_{m2} carefully. Because of this coupling between the input impedance and load impedance, to change one of them can control both. Due to the higher quality factor, this work changes the inductance instead of the capacitance to change the load resonant frequency. So a control switch is inserted in the load nodes to change the operation bands of both the input matching and the load resonance. Both 2.2 GHz and 4.5 GHz bands can be supported by changing the load inductance, meanwhile the input impedance can stay around 50 Ω by carefully choosing the values of g_{m1} and g_{m2}.

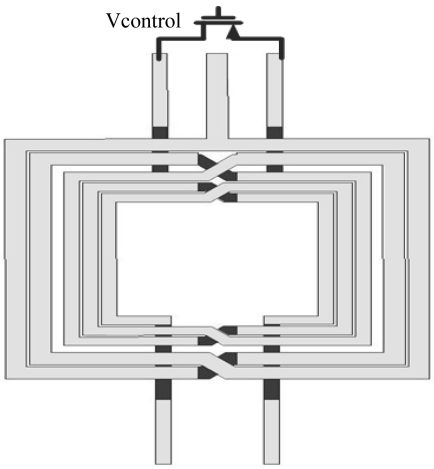

Fig. 2. Layout of the on-chip switchable inductor.

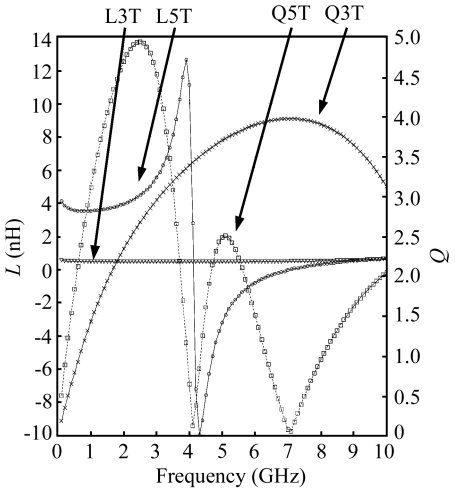

Fig. 3. Inductance and quality factor of the on-chip switchable inductor.

2.3. Switchable inductor

The key issue of this LNA is the reconfigurable load. A switchable on-chip symmetrical inductor is customized: this topology can save three inductors, reducing the chip area a lot[10]. At the same time, the symmetrical topology can reach a higher quality factor than traditional ones. Also, a switch is inserted to short part of the inductor while working in the higher frequency band. It resonates with the node parasitic capacitance to provide the load impedance. The layout of the inductor is shown in Fig. 2: it has an inner diameter of 180 μm and metal width of 10 μm, an outer diameter of 324 μm and metal width of 14 μm. The inductor utilizes the top metal of 20 kÅ, tapping out from the third turn of the total five turns. For higher frequency applications, the outer turns are shorted. As shown in Fig. 3, L5T is the inductance of the whole 5 turns and L3T is that of 3 turns. Similarly, Q5T is the quality factor of the whole 5 turns while Q3T is the quality factor with switch on. Also, the whole 5 turn symmetrical inductor is used as the load when it works in 2.2 GHz bands, so it can reach a higher quality factor: we can see from Fig. 3 that the quality factor reaches its peak at about 2.5 GHz. In addition, the self resonant frequency is higher than 4 GHz, easily covering

the desired band (2.2 GHz). When the switch is on, the outer part of the inductor is shorted to a common point. However, the switch is not an ideal one, and extra parasitic resistances are brought in when the switchable inductor operates in 4.5 GHz bands. Therefore, the quality factor is reduced. But the self resonant frequency is higher than 10 GHz.

2.4. Noise figure

Considering the noise performance, with the positive feedback loop, the transconductance of the input transistors is no long limited to 20 mS for input matching as in the traditional common-gate amplifier. As shown in Eq. (2), this LNA can reduce the noise figure largely by increasing g_{m1}.

$$\mathrm{NF} = 1+\frac{\gamma}{g_{m1}R_S} + \gamma g_{m2}R_S + \frac{(1+g_{m1}R_S)^2}{g_{m1}^2 R_S R_{load}} + \frac{F_2-1}{G_1}, \qquad (2)$$

where R_S is the source resistance, setting to 50 Ω in this work, and R_{load} is the resistance of the load LC tank of the first stage at resonance. F_2 is the noise figure of second stage of LNA and G_1 is the gain of the first stage. The second stage contributes only a little to the noise figure due to the gain of the first stage, so the first stage draws most of our attention. The parameter γ has a value of unity in short-channel devices and decreases toward a value of 2/3 in long-channel devices. Obviously, the noise figure can be reduced by increasing the transconductance of M1, and also by reducing g_{m2} to an acceptable value for good input impedance matching.

2.5. Power gain

The low noise amplifier also needs to provide a high enough power gain to reduce the noise contribution from the following blocks. A buffer stage is added to provide sufficient gain. We can get the overall gain of the LNA from Eq. (3), in which g_{m3} is the transconductance of M5 and M6. R_{load3} is the load impedance of the second stage.

In contrast to the 1.8 V voltage supply of mixer, the LNA uses a 1.2 V voltage supply here to save power consumption.

$$\mathrm{Gain} = \frac{g_{m1}R_{load}g_{m3}R_{load3}}{1+g_{m1}R_S(1-g_{m2}R_{load})}. \qquad (3)$$

2.6. Direct down-converter

The ac couple is used between the LNA and the down-converter. The input of the mixer resonates with the load inductance of the LNA. As the last stage of the RF front-end, the down- converter has a more important effect on the linearity[11]. Due to the better IIP3 performance and higher isolation, a double balance Gilbert architecture (Fig. 4) is chosen. Because three transistors consume a lot of voltage swing, the supply voltage of the mixer is improved to 1.8 V to achieve a higher linearity and the tail current source is taken away to allow a larger swing. With an active mixer topology, the down-converter can easily achieve a conversion gain of 5 dB with a small bias current, only 1.1 mA. Equation (4) shows the ideal gain of the mixer.

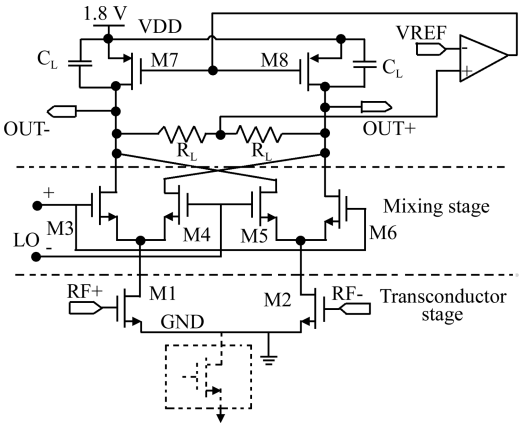

Fig. 4. Topologies of the mixer.

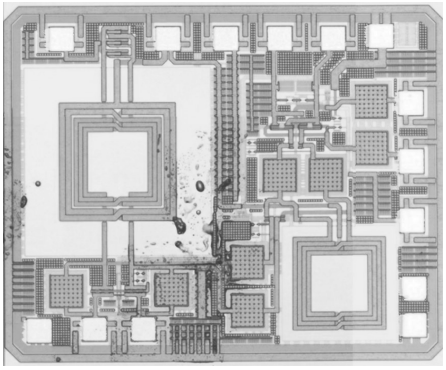

Fig. 5. Die photo of the front-end.

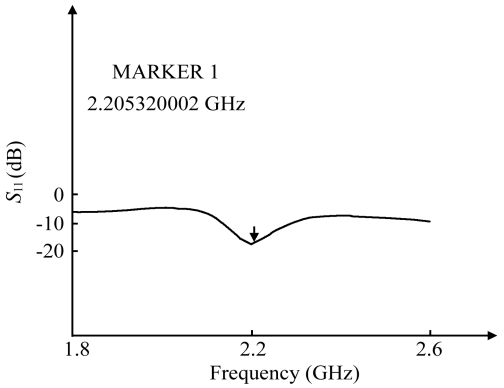

Fig. 6. S_{11} at 2.2 GHz frequency band.

$$G_v = g_m \frac{2}{\pi} R_L. \qquad (4)$$

The size of the switch pairs is carefully optimized to reach a good trade-off between noise figure and linearity, and the load of the mixer can be adjusted to provide different output pole frequencies for different standards, i.e. 20 MHz for 4.5 GHz and 8.6 MHz for 2.2 GHz.

3. Measurement results

The presented reconfigurable receiver RF front-end is fabricated in the UMC 0.18-μm 1P6M RF CMOS process. The die area is reduced to 1.2×1 mm^2 due to the symmetrical inductor, including pads and ESD protection circuits. Figure 5 shows a die photo of it.

Measurement results are shown in Figs. 6–11. In Fig. 6,

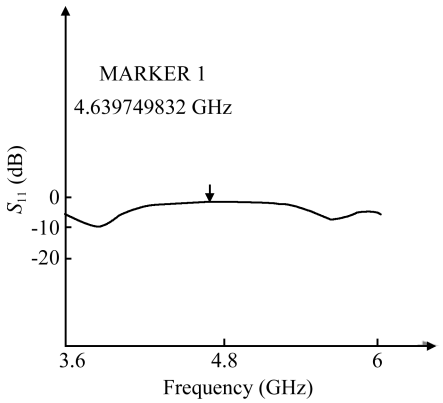

Fig. 7. S_{11} at 4.5 GHz.

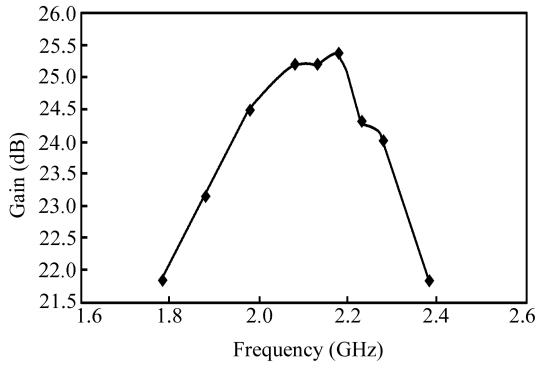

Fig. 8. Gain of 2.2 GHz band.

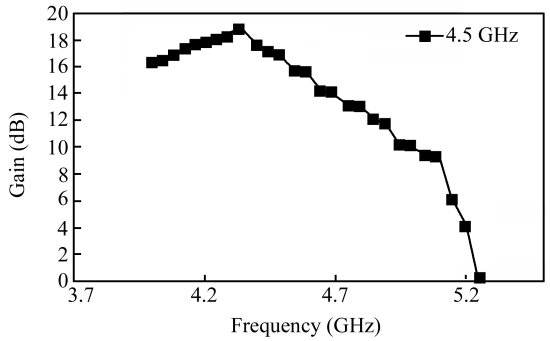

Fig. 9. Conversion gain of the dual-band RF front-end.

S_{11} is lower than –10 dB in the 2.2 GHz frequency band. But from Fig. 7, S_{11} at 4.5 GHz is not the lowest; this may be caused by the parasitic capacitance at the input node, which can not be ignored, while the frequency is twice as high. So the input matching point is lowered to about 4 GHz as we see in Fig. 7, and it can provide a conversion gain of 25 dB at 2.2 GHz, and 18.8 dB at 4.5 GHz. As shown in Figs. 8 and 9, the conversion gain is about 6 dB higher in the 2.2 GHz frequency than 4.5 GHz, due to the higher quality factor of the on-chip inductor in this frequency band. But the linearity of 2.2 GHz is a little lower than 4.5 GHz for its higher gain, which is shown in Figs. 10 and 11. The IIP3 is 6 dBm at 2.2 GHz and 7.3 dBm at 4.5 GHz. The noise figure of the front-end is 9.8 dB at the 2.2 GHz band and 10.6 dB at the 4.5 GHz band. The noise contribution of the back stages may be not reduced effectively, therefore the noise figure is not as we expected. Also the insertion loss of the switch may worsen the noise figure. The LNA

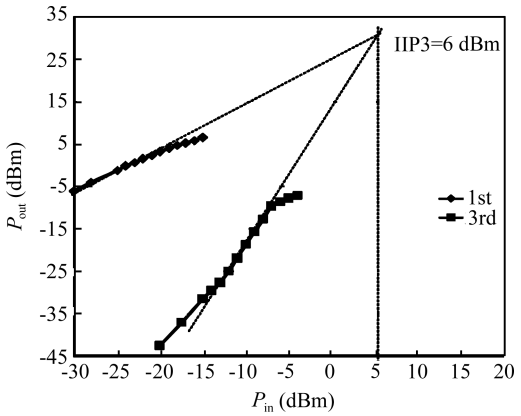

Fig. 10. IIP3 at 2.2 GHz band.

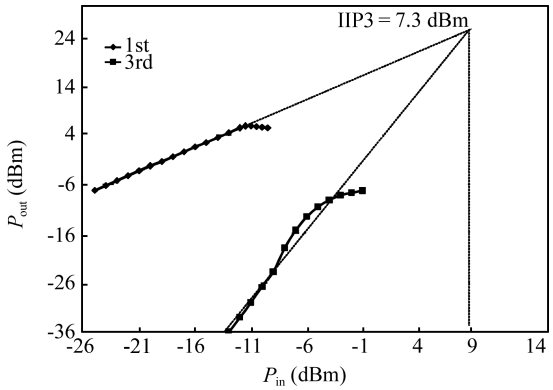

Fig. 11. IIP3 at 4.5 GHz band.

consumes a current of 12 mA under a 1.2 V voltage supply while the down-converter consumes a 2.1 mA current under 1.8 V voltage.

4. Conclusions

A dual-band reconfigurable direct-conversion receiver RF front-end in 180 nm CMOS is presented. The key block is the reconfigurable common gate LNA, using a cross coupling pair to reach dual-band application. This topology makes it easily switched from one operation band to another by an on-chip switchable inductor. The measured results show that the front-end works very well and only consumes a small die area.

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