Noise and mismatch optimization for capacitive MEMS readout*

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Abstract: This paper presents a high precision CMOS readout circuit for a capacitive MEMS gyroscope. A continuous time topology is employed as well as the chopper noise cancelling technique. A detailed analysis of the noise and mismatch of the capacitive readout circuit is given. The analysis and measurement results have shown that thermal noise dominates in the proposed circuit, and several approaches should be used for both noise and mismatch optimization. The circuit chip operates under a single 5 V supply, and has a measured capacitance resolution of 0.2 aF/$\sqrt{\text{Hz}}$. With such a readout circuit, the gyroscope can accurately measure the angular rate with a sensitivity of 15.3 mV/°/s.

Key words: high precision; readout; capacitive MEMS

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1. Introduction

Capacitive microsensors show great advantages, such as low power, high sensitivity, relatively simple structure, and also availability for electrostatic actuation, which results in the reduced complexity of closed-loop microsensors[1]. Recently, with the advanced micro-processing and circuit design techniques, micro-electro-mechanical system (MEMS) sensors with high precision have begun to proliferate more into strategic application markets, such as defense, aviation and space industries, and higher quality and better long term performance are demanded[2].

To intensively increase the signal-to-noise ratio (SNR) is the major challenge for high precision sensor realization. The majority of the reported capacitive MEMS sensor readout circuits adopt a switched-capacitor (SC) or continuous-time (CT) topology, together with correlated-double-sampling (CDS) and a chopper technique to cancel noise so as to optimize the resolution in the system level[3–6]. Another challenge lies in the biasing of the interface nodes between the sensors and the readout circuits. For capacitive sensors, these nodes are of very large impedance, and therefore need to be properly biased to guarantee the system functioning well. Conventional SC design solves this problem at the cost of increased noise, while the CT design maintains a relatively low level of noise, but with more complex biasing circuits, giving rise to degradation of other aspects of performance including the linearity range.

This paper presents a novel topology for high precision capacitive gyroscope readout design. With the combination of SC biasing and CT charge integrating, the readout circuit has been shown by experiment to give excellent performance in terms of both noise and linear dynamic. A detailed analysis on the noise and mismatch of the capacitive readout circuit is given, as are the related methods for optimization. Such analysis results should facilitate analogous designs.

2. Gyroscope description

The proposed interface circuit is designed with the aim of the readout of a bulk micro-machined electro-magnetically driven tuning fork gyroscope in mind[7]. Such a MEMS gyroscope consists of bar structure proof masses and can work at atmospheric pressure as shown in Fig. 1(a). Usually, it has a resonance frequency of 2.75 kHz and signal band of less than 20 Hz. Capacitive sensing is used in the gyroscope design to convert the rotation rate input to the capacitance variance output, by measuring the displacement of the proof mass in a direction orthogonal to both the driven motion and the axis about which rotational motion is to be sensed.

Figure 1(b) shows the equivalent schematic of the gyroscope. It can be seen as a passive three-terminal device. The differential capacitors oscillate inversely, and a differential amplitude-modulated (AM) signal is generated with the

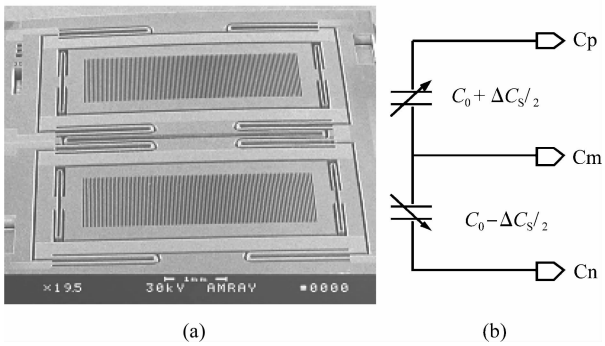

Fig. 1. (a) SEM of the MEMS vibratory gyroscope; (b) Equivalent schematic.

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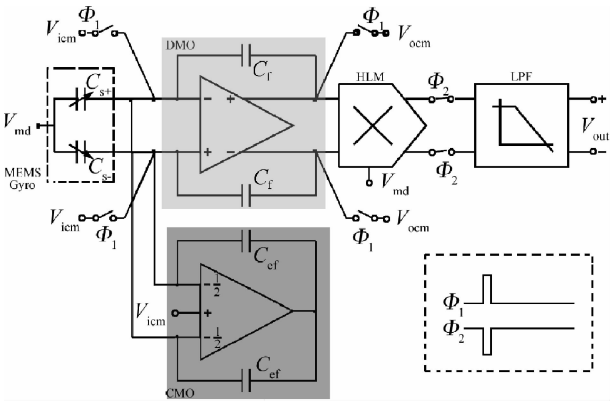

Fig. 2. Block diagram of the readout circuit.

envelop reflecting the rotation rate.

3. High precision readout

In order to maximize the SNR of the readout circuit, a CT voltage sensing amplifier is designed so that the noise performance is not degraded by noise folding or switch noise as in SC circuits. To further cancel the flicker noise, chopper stabilization is used. Also, corresponding to the differential capacitance input, we choose the full differential topology for each part of the circuit design to reject common-mode interference.

A block diagram of the readout circuit is shown in Fig. 2. The chopper carrier signal $V_{\rm md}$ modulates $\Delta C_{\rm s}$ (i.e. the difference between $C_{\rm s+}$ and $C_{\rm s-}$) into the AM form. The chopper frequency is chosen around 1 MHz, below the frequency where the Brownian noise starts to dominate. A differential mode op-amp (DMO) serves as the low-noise charge transfer front-end, converting the AM capacitance into AM voltage. The subsequent optimized high linearity multiplier (HLM) and low-pass filter (LPF) carry out the demodulation.

Note that both the input and output ends of the DMO are high impedance nodes, which means that, without proper dc biasing, the potentials are unpredictable and vulnerable to interference. In this work these nodes are established by low-duty-cycle periodic reset, which is quite common in SC realizations. Such a bias scheme provides a low-impedance dc path, ultra-high ac impedance, ultra-small parasitic capacitance, and minimum noise injected by the biasing circuit.

However, extra common mode stabilization is required when the switches turn off. This is essential for a high dynamic implementation. To suppress the disturbance of the strong carrier, a common mode op-amp (CMO) is adopted. The op-amp maintains adequate bandwidth and gain, which guarantees an effective virtual short between the DMO input and $V_{\rm icm}$. Actually we have chosen a sinusoidal modulation signal instead of the conventional square wave, because the sinusoidal signal with its mono frequency considerably relieves the bandwidth requirement of the op-amp to achieve an equal stabilization result and signal integrity.

After the multiplier, another pair of switches is added, which stops the invalid signals when the resetting is in progress. With such a scheme, the output signal integrity is quite promising.

4. Chopper technique

In CMOS circuits without any compensation, flicker noise usually makes the major contribution in the low frequency band. In some applications, signal sensing varies slowly; therefore, cancelling the flicker noise is the most direct way to increase the resolution. The chopper technique has been widely used to achieve this.

The chopper technique applies modulation to transport the signal to a higher frequency where there is no flicker noise, and then demodulates it back to the baseband after amplification. The chopper amplification principle is illustrated in Fig. 3.

As the noise in a chopper scheme is not sampled or held, the broadband noise is not aliased into the baseband like in a CDS scheme where the power spectrum density (PSD) of the baseband noise increases proportionally with the ratio of the noise bandwidth and the sampling frequency[8]. However, it should be noted that in order to maximize the effect of flicker noise cancellation, the chopper frequency should be chosen higher than the flicker noise corner frequency and lower than the amplifier –3 dB corner frequency.

In our design, as shown in Fig. 2, the chopper modulation is carried out by $V_{\rm md}$ driving the proof mass. Here the input signal is no longer a voltage but a differential capacitance, and the amplification is rather a linear conversion from capacitance to voltage. In some of the literature, square waves instead of sinusoidal waves are used for modulation. Comparatively, the residual noise PSD in the baseband slightly increases as a result of the noise aliasing from the odd harmonics. Also, the sinusoidal wave with its mono frequency considerably relieves the bandwidth requirement of the amplifier, and the complexity of compensation circuits for common mode potential stabilization.

5. Noise analysis

For clarity in the following analysis, a single-ended representation of the differential readout is shown in Fig. 4. Noise contribution from the successive stages can be neglected since the signal has already been amplified. $C_{\rm s}$ is the nominal sensing capacitor. $C_{\rm p}$ represents the sum of interconnect parasitic capacitances. The input transistors of the CMO and the DMO are identical, and their input capacitance is $C_{\rm g}$. The two voltage sources represent the chopper driving signal and the equivalent noise source respectively.

The noise PSD at the output of the amplifier is given by

$$\sqrt{\frac{\overline{v_{\rm o}^2}}{\Delta f}} = \sqrt{\frac{\overline{v_{\rm n}^2}}{\Delta f}}\frac{C_{\rm t}}{C_{\rm i}}, \tag{1}$$

where $C_{\rm t}$ is the total capacitance at the input.

$$C_{\rm t} = C_{\rm s} + C_{\rm p} + C_{\rm cf} + 2C_{\rm g} + C_{\rm i}. \tag{2}$$

The capacitance resolution is thus derived as

$$\sqrt{\frac{\overline{C_{\rm s}^2}}{\Delta f}} = \sqrt{\frac{\overline{v_{\rm o}^2}}{\Delta f}}\bigg/\frac{{\rm d}v_{\rm o}}{{\rm d}C_{\rm s}} = \sqrt{\frac{\overline{v_{\rm n}^2}}{\Delta f}}\frac{C_{\rm t}}{V_{\rm md}}. \tag{3}$$

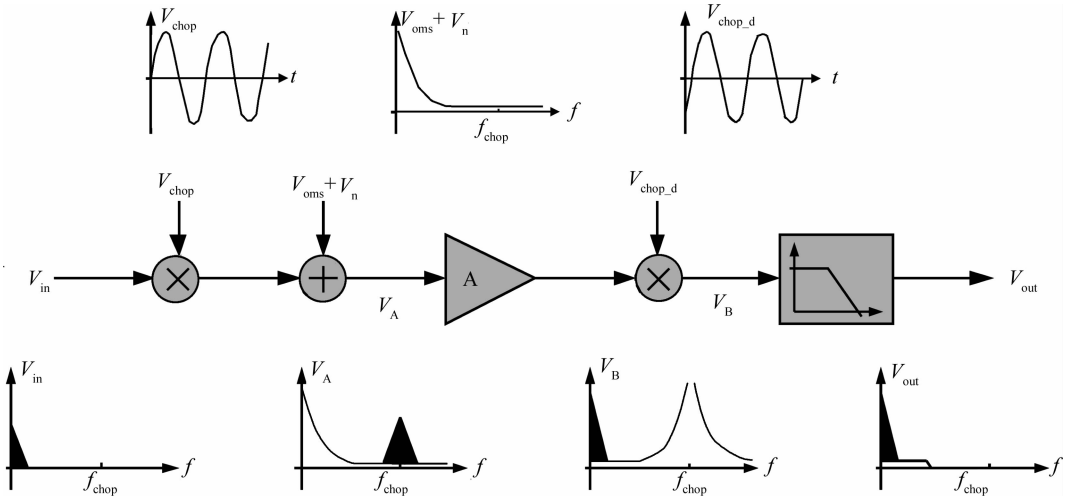

Fig. 3. Chopper amplification principle.

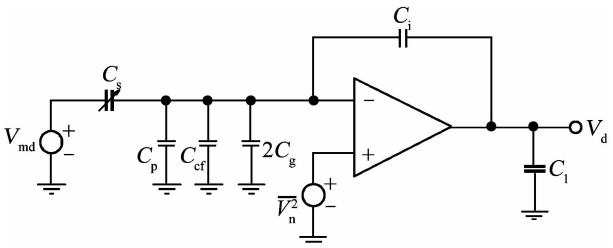

Fig. 4. Single ended schematic of the readout front end for noise calculation.

In order to improve the accuracy of capacitance measurement, the following approaches should be used: (1) minimize the input-referred noise of the OTA, (2) maximize the amplitude of the chopper driving signal, and (3) try to reduce the parasitic capacitance of the bonding wire, by single-chip integration for example.

Since chopper stabilization is employed, thermal noise is the only noise source that matters. A closer look at Eq. (3) indicates another way to optimize the capacitance resolution. The OPA input-referred thermal noise can be expressed as a function of the input transistor size, and with some calculations equation (3) can be rewritten as

$$\sqrt{\frac{\overline{C_s^2}}{\Delta f}} = 4\sqrt[4]{\frac{(1+\gamma)k_B^2T^2L^2}{27\mu I_D C_g}}\frac{C_t}{V_{md}}, \tag{4}$$

where k_B is Boltzmann's constant (1.38×10^{-23} J/K), T is absolute temperature, and γ is the ratio between C_{gs} and C_{gd} which constitute C_g.

So for the minimum capacitor resolution, the optimum C_g is given by

$$C_g = \frac{1}{6}(C_s + C_p + C_{cf} + C_i). \tag{5}$$

If the sensing capacitor and the parasitic capacitance are small as in the case of monolithic surface-processed MEMS, optimum sized input transistors are easily implemented. However, in bulk-processed MEMS where the sensing capacitor is in the order of pF, and when the sensor and the readout circuit are not integrated on the same substrate, the optimum C_g might be difficult to choose. Therefore, using relatively large input transistors should be a better choice for noise minimization.

During the reset phase, on-resistance noise of the reset switch is sampled at the input node of DMO, forming another noise source. Such kT/C noise is uniformly distributed in the frequency range [0, $f_s/2$], and its PSD is given as

$$\frac{\overline{v_{ns}^2}}{\Delta f} = \frac{2k_BT}{C_t f_s}. \tag{6}$$

Apparently, either increasing the total capacitance and the reset frequency can lower the kT/C noise.

6. Mismatch

6.1. Capacitor mismatch

The differential readout has several important advantages, including improved power-supply rejection ratio and first-order rejection of common-mode errors, such as switch charge injection and substrate noise. The differential interface also allows the ground-plain shielding needed to prevent electrostatic pull-down of the proof mass. Finally, driving the proof mass as proposed in this paper (see Fig. 2) allows multiple sets of sensing capacitors to be simultaneously force balanced with feedback loops[9].

Mismatch is one of the most critical issues in differential circuits, because severe mismatch might degrade the sensitivity, the linear range, and even cause malfunction. Figure 5 shows a conventional differential CT capacitance readout scheme. Capacitors $C_{p1,2}$ are parasitic capacitors that include both the structural wiring capacitance and the gate capacitance of the charge integrator.

When the drive signal V_{md} is applied, the capacitive imbalance ($\Delta C_s = C_{s1} - C_{s2}$) generates a different amount of charge to flow from the sensing capacitors onto the integrating capacitors. Meanwhile the differential output is given by

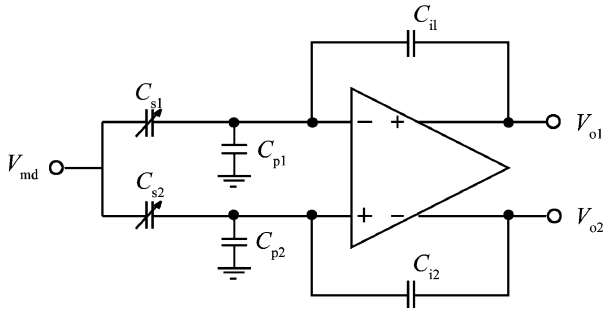

Fig. 5. A conventional differential CT capacitance readout scheme.

$$\Delta V_o = V_{o1} - V_{o2} = -\frac{\Delta C_s}{C_i}(V_{md} - \Delta V_{icm}), \tag{7}$$

where ΔV_{icm} is the swing amplitude of the input common-mode potential.

In our design, a CMO is added to handle the common mode shift as shown in Fig. 1. The DC loop gain is larger than 60 dB, establishing an ideal virtual ground for the integrator input. ΔV_{icm} is thus suppressed below a negligible level. As a result, the parasitic capacitors are shorted, and their mismatch will no longer affect the readout precision. Moreover, the requirement on the common-mode rejection of the charge integrator is considerably reduced.

With ΔV_{icm} calculated, Equation (7) can be rewritten as

$$\Delta V_o = -\frac{V_{md}}{C_i}\left(\Delta C_s - \underbrace{\Delta C_{fb}\frac{C_s}{C_{fb}}}_{\text{Offset error}}\right). \tag{17}$$

Only the mismatch of the CMO feedback capacitors ΔC_{fb} shows up, which can be minimized through an interleave layout. C_{fb} should also be properly increased, but not too large to compromise the readout resolution (see Eq. (4)).

6.2. Charge integrator offset

In fact, all the aforementioned analysis is based upon the assumption that the input and the output of the charge integrator have stable DC operating points. In CT implementation, the capacitive feedback can only suppress the high frequency oscillation, but for DC it can be seen as an open loop. The DC biasing is required to be able to provide a low impedance DC path, and the same time ultra high AC impedance. It also should be invulnerable to the offset, because with a large DC gain, only an offset of several millivolts can pull the output to the rail.

In some published works, reverse-biased diodes, subthreshold MOS transistors, long-channel MOS transistors and large resistors have been used to realize such DC biasing[10–13]. The main trade-off is the AC impedance and their noise contribution. These devices usually have been made quite large to realize AC impedance of several million ohms, while at the same time, an acceptable level of noise density is introduced. In our work, we have got the idea from the SC

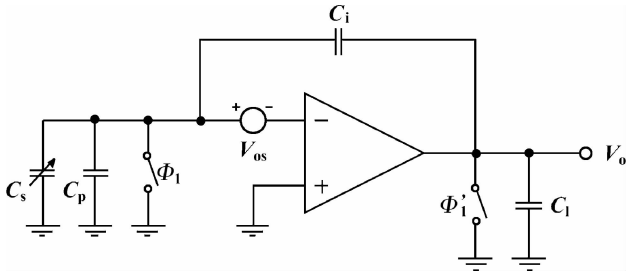

Fig. 6. Principle of offset cancelling in DC biasing with switches.

readout topology, where periodic resetting of the DC bias by switch is quite common. Its kT/C noise is relatively low, and it can easily eliminate the effect of offset.

Figure 6 helps to explain the principle of offset cancelling. V_{os} is the equivalent offset voltage present at the input of the charge integrator. The input and the output of the integrator are simultaneously reset to their own DC potentials every 512 modulation cycles. A very short time later, the switches open at the same time, and the circuit restarts working. So the offset voltage can be seen as a step signal at the very moment the reset switches reopen, the Laplace domain representation of which is

$$V_{os}(s) = \frac{V_{os}}{s}. \tag{18}$$

The loop transfer function of the amplifier is given by

$$A(s) = \frac{A_0}{1 + s/\omega_0}, \tag{19}$$

where A_0 is the DC gain, and ω_0 is the –3 dB cut-off frequency.

The output thus can be calculated as

$$V_o(s) = \frac{\dfrac{V_{os}}{s}\dfrac{A_0}{1 + s/\omega_0}}{1 + \dfrac{C_i}{C_t}\dfrac{A_0}{1 + s/\omega_0}} = V_{os}\frac{C_t}{C_i}\left[\frac{1}{s} - \frac{1}{s + (A_0C_i/C_t + 1)\omega_0}\right], \tag{20}$$

where C_t is the sum of all the capacitance.

Clearly we can see that when the output is stable, the offset is only magnified by the feedback coefficient C_t/C_i, instead of the open-loop DC gain. The time required is inversely proportional to the amplifier gain and the bandwidth. Such an output drift can hardly be large enough to cause swing or linearity deterioration. Also, since it is a DC signal, which is not chopper modulated, it will be cancelled like the low frequency noise and will not affect the readout resolution.

7. Implementation and measurement results

According to the noise and mismatch optimization methods summarized in the previous sections, we have designed a CMOS ASIC for a capacitive gyroscope readout. A full differential scheme is applied, and the chopper technique with 1 MHz frequency is employed. The individual blocks of the circuit, such as the amplifiers and the bandgaps, were optimized to achieve a lower noise floor.

The readout chip was designed in a Chartered 0.35 μm 3-metal 2 poly n-well CMOS process. Figure 7 shows a die mi

Table 1. Performance parameters of the capacitive gyroscope readout chip.

Parameter	Size (mm^2)	Power dissipation (mW)	Sensitivity (mV/fF)	Resolution (aF/ $\sqrt{Hz}$)	Dynamic range (dB)
This work	2	5	0.2	0.2	130
Amini[14]	2	6	2	4	85
Saukoski[15]	0.4	4	0.25	0.25	43
Suster[16]	4	4.5	1.6	0.24	81

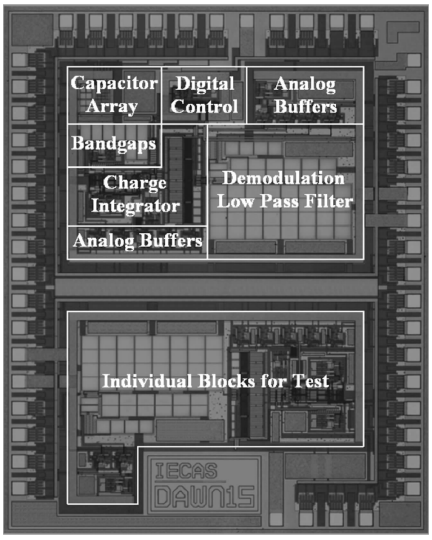

Fig. 7. Die micrograph of the fabricated circuit.

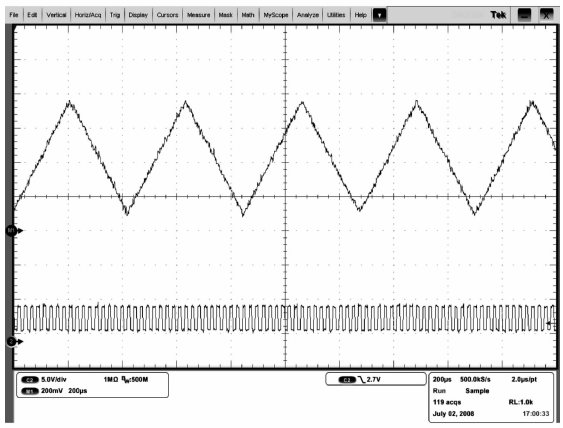

Fig. 8. Readout circuit transient response to a triangle-varying capacitance input.

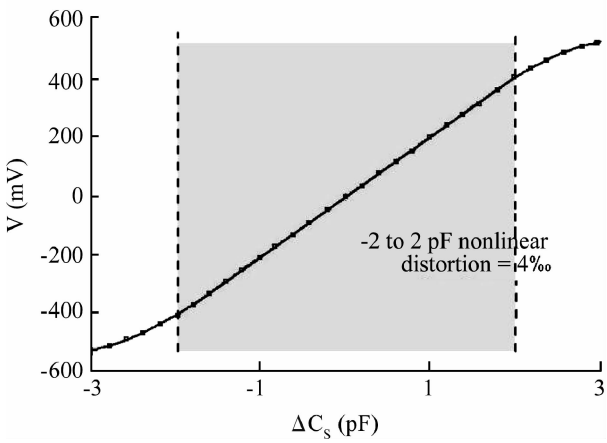

Fig. 9. Linearity performance of the readout circuit.

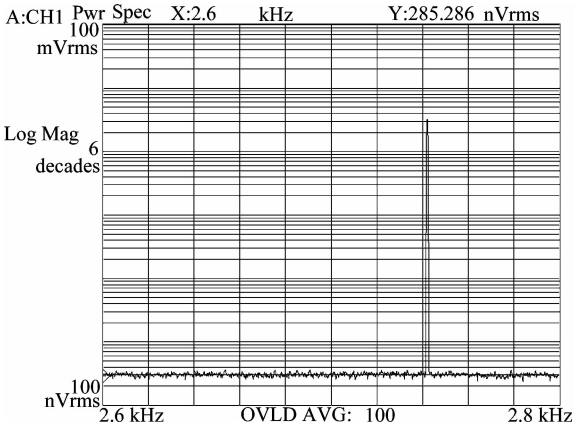

Fig. 10. Frequency spectrum of the circuit output with zero capacitance input.

crograph of the fabricated circuit. All critical individual blocks show up in the chip twice, once in the integrated system, and once discretely, so that their functions can be measured more precisely. A capacitor array with a unit of 100 fF is added in the chip for two purposes, first to facilitate the readout circuit test, and second to compensate for the gyroscope. The circuit dissipates about 5 mW from a single 5 V supply. The performance parameters of the chip are summarized in Table 1, together with some other works for comparison. Amini [14] has chosen a switch-capacitor scheme for capacitance readout, and the noise level is relatively high. Saukoski and Suster [15, 16] have both adopted different continuous time sensing schemes which show great advantage in the resolution, but with less dynamic range.

Figure 8 validates the transient response of the readout circuit using the capacitor array integrated in the chip to generate the capacitance input. It is controlled by a computer programmed signal to realize triangle variation. The square wave at the bottom is the clock of the control signal, and the output of the readout circuit changes at each rising edge of the clock. The output shows great integrity, which should simplify the design of the following stages, such as the sample and hold circuit for digitization.

Figure 9 shows the transfer function of the readout output versus the capacitance input. When a 1 V_{pp} sinusoidal signal is applied as the chopper carrier, the circuit exhibits a sensitivity of around 0.2 mV/fF. The curve shows that in the range of –2 pF to 2 pF capacitance input, the circuit can make the C–V transfer with nonlinear distortion less than 4 ‰. The corresponding output swing is thus 0.8 V.

The output noise floor of the readout circuit is measured by a frequency spectrum analyzer. As shown in Fig. 10,

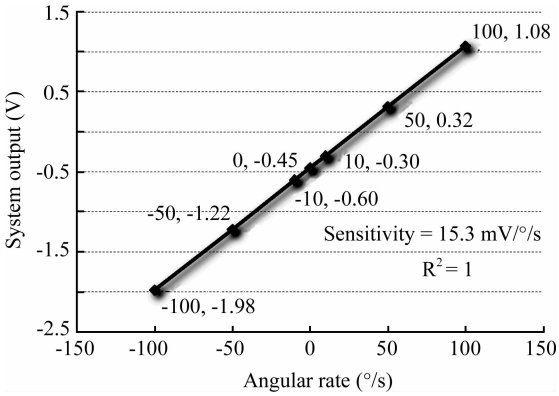

Fig. 11. System output versus angular rate.

with a frequency resolution of 1600 lines, the noise floor reads 285 nVrms, corresponding to 400 nV per root unit bandwidth. Divided by the highest possible readout sensitivity of 2 mV/fF,that results in a minimum capacitance resolution of 0.2 aF/ $\sqrt{\text{Hz}}$. So, when the circuit is used to provide a readout for a gyroscope with 20 Hz signal bandwidth, it can detect a minimum capacitance of 0.9 aF, which also means the dynamic range is larger than 130 dB.

A combined test of the readout chip with the gyroscope is also carried out. Figure 11 shows the system outputs when constant angular rates are applied. A sensitivity of 15.3 mV/°/s is observed with excellent linearity.

8. Conclusion

A high precision CMOS readout circuit for a capacitive MEMS gyroscope has been analyzed in terms of noise and mismatch to identify the limiting factors and an optimized system has been implemented. For the proposed topology, low frequency noise has been effectively eliminated by the chopper technique, leaving thermal noise dominant, which can be limited by sizing the amplifier input transistors properly. The analysis also indicates that mismatch is another critical issue for readout performance. However, the system has shown great immunity to such nonideality, and by careful layout its negative effect should be negligible. The readout circuit chip has been fabricated and measured. A capacitance resolution of 0.2 aF/ $\sqrt{\text{Hz}}$ is observed with a sensitivity of 0.2 mV/fF. Finally, a gyroscope using such a readout chip has achieved an angular rate sensitivity of 15.3 mV/°/s.

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