1-Gb/s zero-pole cancellation CMOS transimpedance amplifier for Gigabit Ethernet applications*

Huang Beiju(黄北举)†, Zhang Xu(张旭), and Chen Hongda(陈弘达)

(State Key Laboratory of Integrated Optoelectronics, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)

Abstract: A zero-pole cancellation transimpedance amplifier (TIA) has been realized in 0.35 μm RF CMOS technology for Gigabit Ethernet applications. The TIA exploits a zero-pole cancellation configuration to isolate the input parasitic capacitance including photodiode capacitance from bandwidth deterioration. Simulation results show that the proposed TIA has a bandwidth of 1.9 GHz and a transimpedance gain of 65 dB·Ω for 1.5 pF photodiode capacitance, with a gain-bandwidth product of 3.4 THz·Ω. Even with 2 pF photodiode capacitance, the bandwidth exhibits a decline of only 300 MHz, confirming the mechanism of the zero-pole cancellation configuration. The input resistance is 50 Ω, and the average input noise current spectral density is 9.7 pA/$\sqrt{\text{Hz}}$. Testing results shows that the eye diagram at 1 Gb/s is wide open. The chip dissipates 17 mW under a single 3.3 V supply.

Key words: CMOS; transimpedance amplifier; Gigabit Ethernet
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1. Introduction

Urgent demand in internet and multimedia applications has led network communication systems to support data transmission capacities up to the Gigabit/s range. For high speed data transmission systems, electrical interconnection proves to be the bottleneck of high frequency applications for its intrinsic transmission delay resulting from the RC time constant. Fortunately, optical data links may offer a solution for the increased bandwidth demand in high speed communication systems[1, 2] because of their low crosstalk and large bandwidth.

Gigabit Ethernet standards, based on optical fiber physical layers, are the best options for low-cost, high speed local area networks (LANs). The Gigabit Ethernet is the extension of the IEEE 802.3 Ethernet standard developed for Gigabit/s communications[3]. The Gigabit Ethernet standard covers two main transmission schemes over fiber: 1000Base-SX (at 850 nm) and 1000Base-LX (at 1300 nm)[4]. The Gigabit Ethernet optical transceiver system comprises both optical devices and integrated circuits. The transmitter is composed of laser and driver circuitry, while the receiver consists of a photodetector, a low-noise transimpedance amplifier (TIA) and a high-gain main amplifier.

The front-end TIA[5, 6] is a critical element in optical receivers, affecting the total system performance. Therefore, III–V semiconductor compounds such as GaAs and InP–InGaAs[7, 8] have been exploited to realize such circuits due to their inherently high-speed, high transconductance and low-noise characteristics. Though these components can meet the requirements for high speed and high performance, their high manufacturing cost limits their wide use in short-distance applications. In contrast, silicon technology—particularly submicron CMOS technology—has recently become very attractive due to its low cost and high integration. Using submicron CMOS technologies, designers can reduce cost, achieve the transmission rates required and obtain great integration levels[9].

In this paper, we design a zero-pole cancellation CMOS TIA for Gigabit Ethernet applications. We summarize the conventional TIA configuration. We also present the TIA with zero-pole configuration to isolate the influence of parasitic capacitance on bandwidth deterioration, and analyze the bandwidth, noise and sensitivity.

2. Conventional TIA configuration

The parasitic capacitance of the photodetector is on the order of pF. Thus, the input impedance of the amplifier should be as small as possible to reduce the RC constant, which alleviates the large capacitance influence on the bandwidth. In a common TIA configuration, shown in Fig. 1, the input

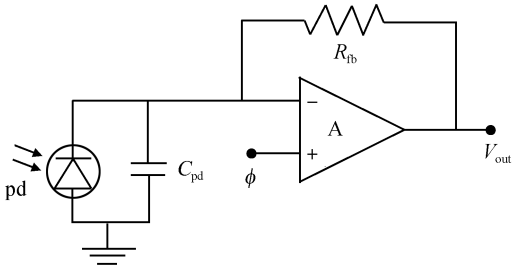

Fig. 1. Conventional TIA implementation.

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† Corresponding author. Email: bjhuang@semi.ac.cn

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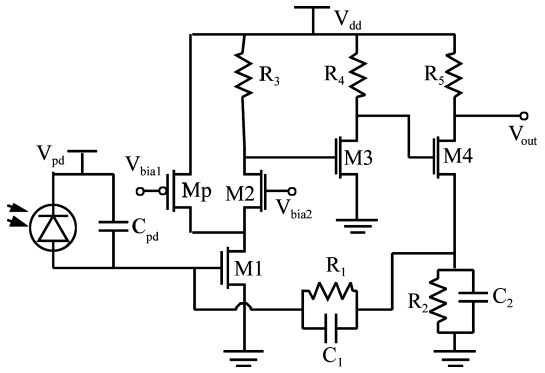

Fig. 2. Preamplifier with zero-pole cancellation configuration.

impedance depends on the value of the feedback resistor R and amplifier gain A:

$$Z_{\text{in}} = \frac{R}{A+1}\frac{1}{1+s\dfrac{RC_{\text{p}}}{A+1}}. \tag{1}$$

Thus, a small feedback resistor value and a large value of amplifier gain A are desired to obtain low input impedance. The transimpedance gain of the TIA is the product of A and Z_{in}.

$$\text{Gain} = AZ_{\text{in}} = R\frac{\dfrac{A}{A+1}}{1+s\dfrac{RC_{\text{p}}}{A+1}}. \tag{2}$$

The gain is almost dependent on the feedback resistor since the amplifier gain A is rather large. On the other hand, the input referred current noise is also strictly dependent on the value of the feedback resistor. The value of the feedback resistor should be large to increase the transimpedance gain and decrease the input noise. But a large value of feedback resistor results in large input impedance Z_{in}, which induces bandwidth deterioration. The large input impedance Z_{in} together with input capacitance as well as photodiode parasitic capacitance limits the electrical bandwidth of the TIA.

These considerations lead to a trade-off between noise, gain and bandwidth, which indicate that it is not possible to optimize noise, gain and bandwidth performance together in the classical TIA. In order to optimize all of these parameters, we propose a shunt series feedback TIA based on the Miller effect using zero-pole cancellation.

3. Zero-pole cancellation TIA

Figure 2 shows a schematic diagram of the zero-pole cancellation TIA consisting of a cascode stage, a common source stage, a common drain stage, a feedback network and a differential amplifier. M1 and M2 form the cascode stage that amplifies the photo-current to the drain of M2. Mp is used to reduce the current of M2 and R_3, which means that the gate voltage of M2 can be biased at low levels, saving the voltage swing room of the cascode. M3 and M4 are the common source stage used as the voltage gain stage. R_1, C_1, R_2 and C_2 constitute the feedback network to enhance the bandwidth by zero-pole cancellation.

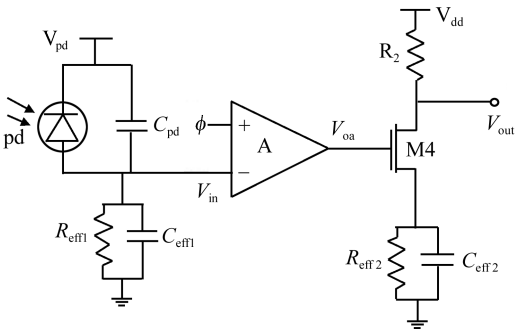

Fig. 3. Equivalent circuit of the TIA in Fig. 2.

3.1. Bandwidth analysis

The single-ended preamplifier can be simplified as shown in Fig. 3. A is the amplifier gain of the cascode stage and the common source stage (M3), given by:

$$A = g_{\text{m1}}R_3g_{\text{m3}}R_4. \tag{3}$$

C_{pd} is the parasitic capacitance of the photodetector. R_{eff1}, C_{eff1}, R_{eff2} and C_{eff2} are the equivalent resistance and capacitance of the feedback network by the Miller effect, which can be described by Eqs. (2) to (5) when considering the transistor M4 as an ideal buffer.

$$R_{\text{eff1}} = \frac{R_1}{1+A}, \tag{4}$$

$$C_{\text{eff1}} = (1+A)C_1, \tag{5}$$

$$R_{\text{eff2}} \cong \frac{R_1R_2}{R_1+R_2}, \tag{6}$$

$$C_{\text{eff2}} \cong C_1 + C_2. \tag{7}$$

From the simplified single-ended circuit in Fig. 3, we derive the expression of transfer function as follows:

$$\begin{aligned} H(s) &= \frac{V_{\text{out}}}{I_{\text{pd}}} = \frac{V_{\text{in}}}{I_{\text{pd}}}\frac{V_{\text{oa}}}{V_{\text{in}}}\frac{V_{\text{out}}}{V_{\text{oa}}} \\ &= -\frac{R_{\text{eff1}}}{1+sR_{\text{eff1}}(C_{\text{eff1}}+C_{\text{pd}})}A\frac{R_5}{\dfrac{1}{g_{\text{m4}}}+R_{\text{eff2}}//C_{\text{eff2}}} \\ &\cong -\frac{AR_5R_{\text{eff1}}}{1+sR_{\text{eff1}}(C_{\text{eff1}}+C_{\text{pd}})}\frac{1+sR_{\text{eff2}}C_{\text{eff2}}}{R_{\text{eff2}}}. \end{aligned} \tag{8}$$

The transfer function contains a zero and a pole induced by the feedback network. In order to obtain the pole cancellation, we force the frequency of zero to be equal to the frequency of pole. Thus, we obtain a value of C_2 to meet zero-pole cancellation:

$$C_2 = \frac{R_1}{R_2}C_1 + \left(1+\frac{R_1}{R_2}\right)\frac{C_{\text{pd}}}{1+A}. \tag{9}$$

Substituting Eq. (10) into Eq. (9), the transfer function can be simplified as:

$$H(s) = -\frac{AR_5R_{\text{eff1}}}{R_{\text{eff2}}} = -\frac{A}{1+A}R_5\left(1+\frac{R_1}{R_2}\right) \cong -R_5\left(1+\frac{R_1}{R_2}\right). \tag{10}$$

This means that the gain is mainly related to the load resistor and the ratio between the resistors in the feedback network. More importantly, Equation (10) means that the final

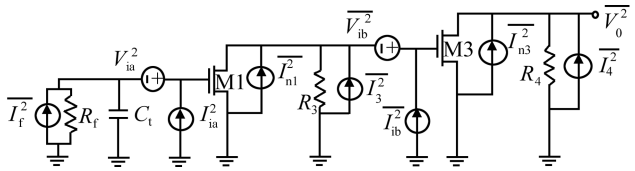

Fig. 4. Simplified schematic of the noise model of the amplifier including feedback loading and noise sources.

bandwidth is determined by the amplifier, not the input parasitic capacitor and feedback resistor as long as the feedback capacitor meets the requirements of Eq. (9). This is the significant difference between the zero-pole cancellation TIA and a conventional TIA where the final bandwidth is determined by the input capacitor and feedback resistor. The feedback resistor not only influences the bandwidth, but also gain and noise make it impossible to optimize bandwidth, gain and bandwidth performance simultaneously in the conventional TIA. In the zero-pole cancellation TIA, the bandwidth is determined by the amplifier, the gain is determined by the feedback resistor ratio and the noise is determined by the value of the feedback resistor. Thus, we can optimize all the parameters separately and independently. For example, we can choose a big feedback resistor value and keep the feedback resistor ratio constant to produce a noise benefit without affecting the bandwidth and gain.

3.2. Noise analysis

The noise performance of the preamplifier is crucial for the receiver because the photo-current is rather weak; the equivalent input noise level should be low enough to ensure that the receiver operates at high sensitivity for a low bit-error-rate. Figure 4 shows the noise equivalent circuit of the preamplifier; only the first two stages are taken into account since the gain is high enough that the noise of the following stage is negligible. Omitting the flicker noise, the main noise source of the circuit is the channel noise of the active devices and the thermal noise sources of the resistors. The noise of M2 and Mp contributes negligibly to the output since the impedance at the drain of M1 is large[10], so it is ignored in Fig. 4. R_f and C_t are equivalent input resistance and capacitance:

$$R_f = R_1 + R_2, \tag{11}$$

$$C_t = \frac{C_1 C_2}{C_1 + C_2}. \tag{12}$$

The equivalent input-referred voltage and current noise of M3 can be written as:

$$\overline{V_{ib}^2} = \left(4kT\gamma g_{m3} + \frac{4kT}{R_4}\right)\Big/ g_{m3}^2, \tag{13}$$

$$\overline{I_{ib}^2} = 2qI_{G3} + \frac{\omega^2 C_{gs3}^2}{g_{m3}^2}\left(4kT\gamma g_{m3} + \frac{4kT}{R_4}\right), \tag{14}$$

where I_{G3} is the gate leakage current, which is very small. In the same way, the equivalent input-referred voltage and current noise of M1 can be written as:

$$\overline{V_{ia}^2} = (\overline{I_{n1}^2} + \overline{I_3^2} + \overline{I_{ib}^2} + \frac{\overline{V_{ib}^2}}{R_3^2})\Big/ g_{m1}^2, \tag{15}$$

$$\overline{I_{ia}^2} = 2qI_{G1} + \omega^2 C_{gs1}^2 \overline{V_{ia}^2}. \tag{16}$$

Considering the equivalent input resistance and capacitance, the total input noise current spectral density can be expressed as:

$$\overline{I_{i,tot}^2} = \overline{I_f^2} + \overline{I_{ia}^2} + \left(\frac{1}{R_f^2} + \omega^2 C_t^2\right)\overline{V_{ia}^2}, \tag{17}$$

where $\overline{I_f^2}$ is thermal noise of R_f, equaling $4kT/R_f$. Substituting Eqs. (14, 15, 16) into Eq. (17) and simplifying the result, we obtain:

$$\overline{I_{i,tot}^2} = \frac{4kT}{R_f} + 2qI_{G1} + \frac{1}{g_{m1}^2}\left(\frac{1}{R_f^2} + \omega^2 C_t^2 + \omega^2 C_{gs1}^2\right)\Bigg[4kT\gamma g_{m1} + \frac{4kT}{R_3} + 2qI_{G3} + \left(4kT\gamma g_{m3} + \frac{4kT}{R_4}\right)\left(\frac{\omega^2 C_{gs3}^2}{g_{m3}^2} + \frac{1}{g_{m3}^2 R_3^2}\right)\Bigg]. \tag{18}$$

According to Eq. (18), R_f, R_3, R_4, g_{m1} and g_{m3} should be as large as possible, and C_{gs1}, C_{gs3} and C_t should be as small as possible to reduce the total noise. To increase g_{m1}, g_{m3}, either the bias current or the transistor aspect ratio W/L should be increased, while a large bias current not only leads to high power consumption but also means that R_3 (R_4) should be reduced to make sure that M1 (M3) operates in the saturation region, which consequently increases the noise. Additionally, a large transistor aspect ratio increases capacitance C_{gs1}, C_{gs3}, which results in noise degeneration. Hence, a choice of proper ratio W/L and bias current is necessary to optimize the noise performance. In addition, R_f should be large enough to minimize noise. Unlike the common TIA, we enhance the –3 dB bandwidth by zero-pole cancellation, which means that the influence of R_f on the bandwidth is negligible. So, it is possible to break the compromise between noise, gain and bandwidth with this proposed architecture. A high gain can be achieved by choosing a large constant value of the ratio between R_1 and R_2. A larger value of R_1 increases the gain and decreases noise, while it has almost no influence on the bandwidth as long as a proper value of C_2 is chosen to satisfy Eq. (9).

3.3. Sensitivity analysis

The total input noise current is obtained by integration of Eq. (18):

$$\overline{I_{n,in}^2} = \int_0^B \overline{I_{i,tot}^2}\,\mathrm{d}f, \tag{19}$$

where B is the bandwidth of the amplifier. The probability of a wrong decision, called the bit-error-rate, can be expressed as[11]:

$$\mathrm{BER} \cong \frac{1}{\sqrt{2\pi}}\exp\left(-\frac{Q^2}{2}\right)\left(1 - \frac{1}{Q^2}\right). \tag{20}$$

Q is the noise distance determined by the signal current and input noise current. For a typical value BER of 10^{-9} in practice, Q is equal to 6. To achieve a certain low BER described in Eq. (20), the input optical power should be large enough to

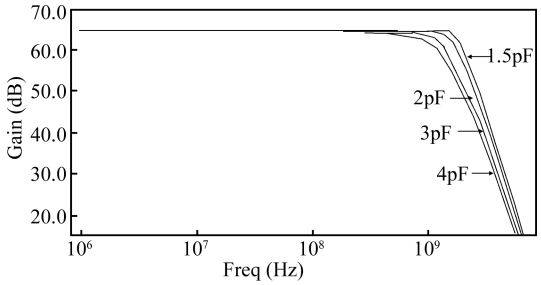

Fig. 5. Bandwidth of the TIA at different input parasitic capacitance values.

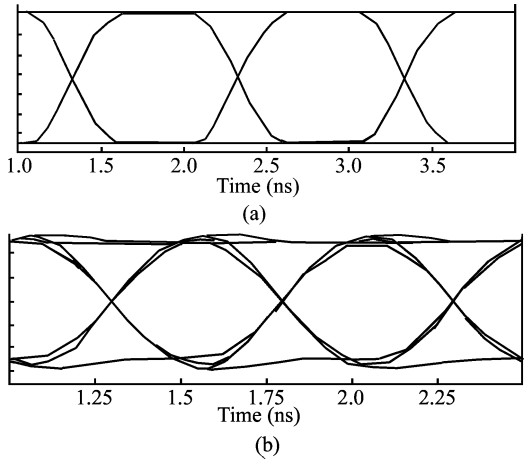

Fig. 6. Eye diagrams of the TIA for 1 μA input current: (a) 1 Gb/s eye diagrams for 4 pF input capacitance; (b) 2 Gb/s eye diagrams for 3 pF input capacitance.

obtain the required value of the signal current. This lowest detectable optical power is usually defined as sensitivity[11]:

$$S = \frac{Q\sqrt{I_{\mathrm{n,in}}^2}}{R_0}, \tag{21}$$

where R_0 is the responsivity of the photodetector. For a high speed CMOS compatible photodetector[12], the responsivity is very small (typically 0.04 A/W), which demands more stringent noise performance requirements from the TIA to obtain high sensitivity.

4. Simulation and measurement results

Figure 5 shows the –3 dB bandwidth of the TIA at different input parasitic capacitances. For 1.5 and 2 pF input capacitance, the bandwidth is 1.9 and 1.6 GHz respectively. When input capacitance increases to 3 and 4 pF, the bandwidth decreases to 1.3 and 1 GHz. The transimpedance gain is as high as 65 dB·Ω. The gain-bandwidth product (3.4 THz·Ω) is higher than the conventional TIA[13], which clarifies the advantage of the zero-pole cancellation configuration. The input impedance of TIA is 50 Ω within the bandwidth without peaking when input capacitance is larger than 3 pF. A slight peaking occurs around 1.5 GHz when input capacitance is smaller than 2 pF.

Figure 6 shows eye diagrams of the TIA at bit rates of 1 and 2 Gb/s. The two eye diagrams are both wide open which can be attributed to the excellent structure of the proposed preamplifier.

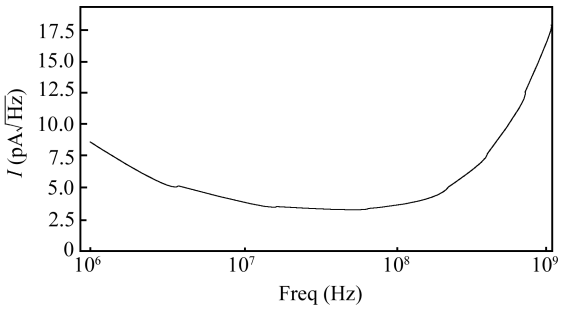

Fig. 7. Input noise current spectral density.

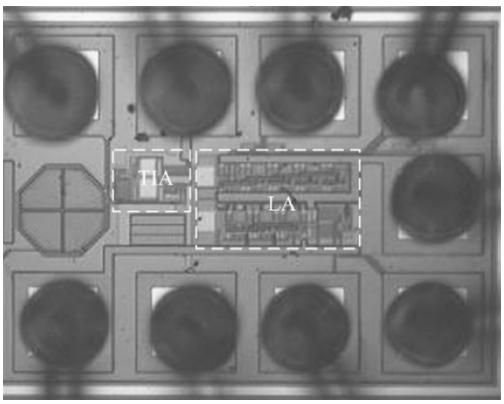

Fig. 8. Die photograph of TIA.

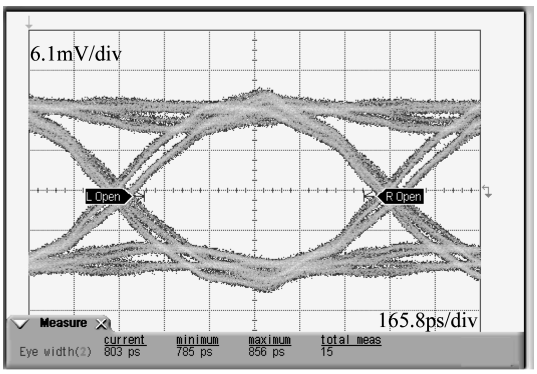

Fig. 9. Testing eye diagrams at 1 Gb/s.

Figure 7 depicts the simulation of input noise current spectral density, where the minimum and average noise current spectral densities are 3.2 and 9.7 pA/$\sqrt{\mathrm{Hz}}$ within the 1 GHz bandwidth. A chip photograph is shown in Fig. 8; this integrates the TIA and the limiting amplifier (LA). The whole die size is 650 × 400 μm^2. The TIA core occupies only 100 × 100 μm^2. The Agilent ParBEERT 81250A outputs a pseudorandom bit sequence (PRBS) to test the TIA eye diagrams. Figure 9 demonstrates the measured eye diagrams at a data rate of 1 Gb/s for 2^{-31}– 1 PRBS with 30 μA equivalent photocurrent. The degeneration of the bit rate is mainly because of the parasitic capacitance of the test PCB board and test equipment. The amplitude of the eye diagram is 24 mV, and the jitter is 80 ps. The TIA dissipates 17 mW under a single 3.3 V supply.

5. Conclusion

A zero-pole cancellation transimpedance amplifier (TIA) has been realized in 0.35 μm RF CMOS technology for

Gigabit Ethernet applications. On analyzing the bandwidth, noise and sensitivity of the zero-pole cancellation TIA, it shows better performance than a conventional TIA. The bandwidth, gain and noise can be optimized separately and independently, which means that noise-bandwidth and gain-bandwidth trade-offs are not necessary. Simulation and testing results show that the TIA is very promising for Gigabit Ethernet applications.

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