# Adjustment of NiSi/n-Si SBH by post-silicide of dopant segregation process

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**Abstract:** The post-silicide of dopant segregation process for adjusting NiSi/n-Si SBH (Schottky barrier height) is described. Adopting the analysis of the *I–V* characteristic curve and extrapolating the SBH of NiSi/n-Si Schottky junction diodes (NiSi/n-Si SJDs), the effects of different of process parameters dopant segregation, including segregation anneal temperature and dopant implant dose, on the properties of the NiSi/n-Si SJDs have been studied, and the corresponding mechanisms are discussed.

**Key words:** NiSi/n-Si SJD; SBH; dopant segregation

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## 1. Introduction

As the feature dimensions of MOSFETs scale into the nanometer regime, instead of an impurity doped S/D, a metal S/D has been considered as the most promising candidate, due to its atomically abrupt junctions, to minimize short-channel effects, low source/drain series resistances and contact resistance. In addition, the low-temperature process for S/D formation enables the integration of critical new materials, such as high-*k* gate insulators, metal gates, strained silicon substrate, etc. However, the traditional metal S/D MOSFET has a low drive current in the on state due to its high Schottky barrier height (SBH) at the source/channel interface, and has high leakage current in the off state due to its low SBH at the drain/channel interface[1]. So, since SB MOSFETs have been introduced, researchers have studied the SBH tuning techniques to overcome the inherent defects of SB MOSFETs, in order to achieve *I–V* characteristics similar to those of the traditional doped S/D MOSFET.

Among the many SBH tuning techniques, the post-silicide of dopant segregation process[2] uses the same kind of metal silicide, thus not only satisfying the requirement of NMOS and PMOS, but also simplifing the process flow. Furthermore, this process separates the silicide formation process from the dopant segregation process, which avoids the effect of implant impurities on silicide formation, resulting in an excellent metal silicide film. Moreover, the implant process with low implanted energy reduces implant damage in the silicide film, which maintains the integrity of the silicide/Si interface. We believe that the post-silicide of dopant segregation process will be the most promising SBH tuning technique to realize high performance metal S/D MOSFETs.

## 2. Experiment

Blanket n-type (2–4 Ω·cm) Si (100) substrates were used in this work. Following oxidation, photolithography and wet etching, many circular windows with diameter 250 $\mu$m were formed. Then, TiN/Ni multi-layer metal films were prepared on these wafers by alternate deposition of Ni film and TiN film. The Ni-silicide formation process was carried out *ex situ* by two-step rapid thermal processing (RTP) in high pure nitrogen ambient. The two-step Ni silicide formation process followed the procedure of low temperature RTP, selective etching and higher temperature RTP. Later, some of the wafers were treated with different process conditions of the dopant segregation process and other wafers were untreated. Finally, metal Al was deposited at both sides of the wafer to form a metal electrode. Figure 1 is a diagram of the experimental procedure. A four-point probe (FPP) was used to measure the sheet resistance of the formed Ni-silicide films. X-ray diffraction (XRD) with Cu K$\alpha$ radiation was employed for Ni-silicide phase analysis, and high resolution transmission electron microscopy (HRTEM) was used to analyze the character of the Ni-silicide/Si interface and to measure the thickness of the Ni-silicide films. A Keithley-4200-SCS was used to measure the *I–V* characteristic of NiSi/n-Si at room temperature (300 K).

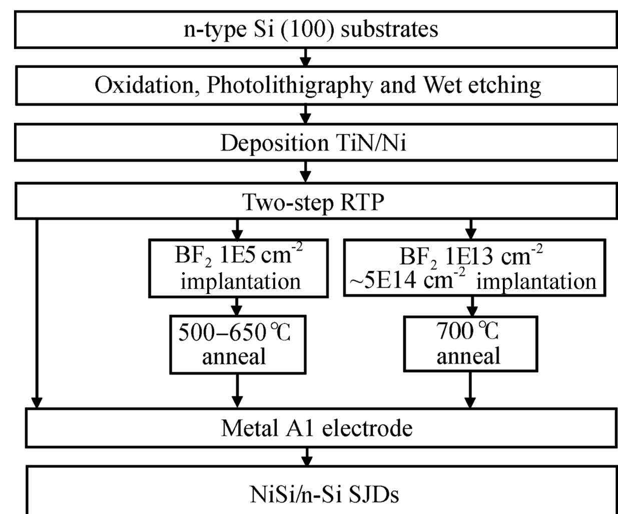


Fig. 1. Experimental procedure diagram.

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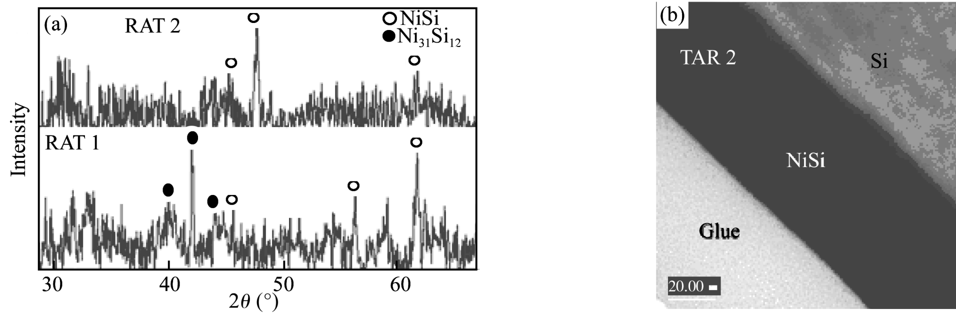


Fig. 2. TiN(120 Å)/Ni(220 Å)/Si sample after two-step RTP: (a) XRD spectra; (b) Cross-sectional HRTEM image.

## 3. Results and analysis

Figure 2 shows the XRD spectra and the cross-sectional HRTEM image of the TiN(120 Å)/Ni(220 Å)/Si sample after two-step RTP. From Fig. 2 it can be seen that only the NiSi phase exists and the NiSi/Si interface is smooth. Measuring from the HRTEM image of RTA2, the thickness of NiSi is 48 nm. This ratio of Ni transforming to NiSi is consistent with the results of Ref. [3]. So from this result we deduce the requirement process parameters for 35 nm NiSi film formation.

According to one dimensional thermionic emission theory[4], the current transport equation for SJD and the SBH equation are given by

$$I = AA^*T^2 \exp\left(-\frac{\phi_B}{V_T}\right)\left(\exp\frac{V-IR}{nV_T}-1\right)$$
$$= I_{ST}\left(\exp\frac{V-IR}{nV_T}-1\right), \tag{1}$$

$$\phi_B = V_T \text{Im}\frac{AA^*T^2}{I_{ST}}, \tag{2}$$

where $A$ is the square of the SJD, $A^*$ is the effective Richardson constant for thermionic emission, $T$ is the thermodynamic temperature in Kelvin, $V_T = kT/q$ is the thermal voltage, $n$ is the ideality factor and $R$ is the series resistance. $\phi_B$ is $\phi_{Bn}$ or $\phi_{Bp}$, where $\phi_{Bn}$ ($\phi_{Bp}$) is the effective SBH between the metal and n-Si (p-Si) substrate. $I_{ST}$ is the reverse saturation current. When $V > V_T$ and we ignore the influence of $IR$, the current transport equation for SJD is given by

$$I = I_{ST}\exp\frac{V}{nV_T}, \tag{3}$$

$$\ln I = \ln I_{ST} + \frac{1}{nV_T}V. \tag{4}$$

In a semilog coordinate system, the curve of $\ln I$–$V$ is a line, with gradient $1/nV_T$ and intercept $\ln I_{ST}$. So selecting proper curve data at the linear part to fit Eq. (4), we can deduce $n$ and $\phi_{Bn}$ ($\phi_{Bp}$). If we know one of $\phi_{Bn}$ or $\phi_{Bp}$, then the other one can be calculated using[4]:

$$\phi_{Bn} + \phi_{Bp} = E_g, \tag{5}$$

where $E_g$ is the band gap of Si[4].

Figure 3(a) shows an untreated NiSi/n-Si SJD $I$–$V$ characteristic curve. All the constants are taken from Ref. [4] and

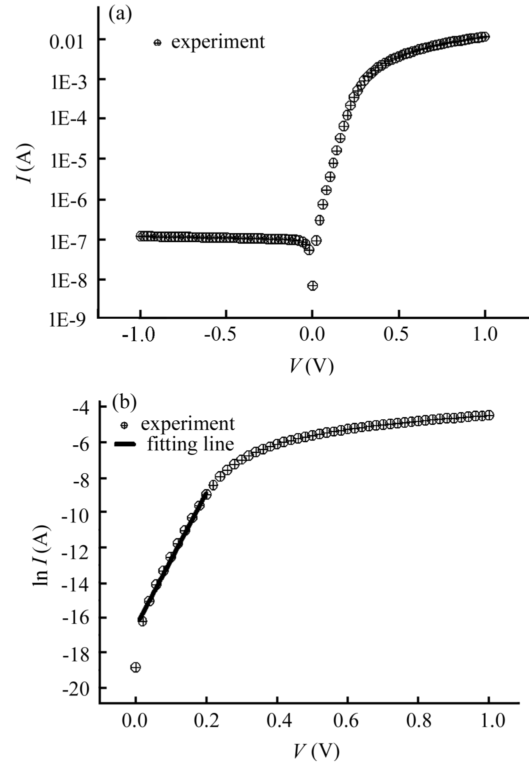


Fig. 3. (a) Abs($I$)–$V$ and (b) forward ln $I$–$V$ characteristic curve of an untreated NiSi/n-Si SJD.

taking $\phi_{Bn}$ and $n$ as unknown parameter, we select partial curve data which is shown in Fig. 3(b) to fit Eq. (4). The fitted results are $n = 1.01$ and $\phi_{Bn} = 0.705$ eV, so $\phi_{Bp} = 0.415$ eV.

In order to investigate the adjusting mechanism of the dopant segregation process, some wafers were treated under different process conditions and $\phi_{Bn}$ and $n$ were abstracted with the above-mentioned method.

Some wafers were treated with various doses ($1 \times 10^{13}$–$5 \times 10^{14}$ cm$^{-2}$) of $BF_2$ ion implantation at the same implantation energy and segregation annealing at 700 °C for 30 s. Figures 4(a) and 4(b) respectively show the Abs($I$)–$V$ characteristic curve which were measured without avoiding light and the change curve of $\phi_{Bn}$ and $n$ without and with various doses of the dopant segregation process for a NiSi/n-Si SJD. Figure 4(a) shows that the reverse current of the NiSi/n-Si SJD decreases and the zero point drift in the forward direction increases with increased implanting dose. The main reason for the first phenomenon is the impurity segregation effect in the post-silicide process. A mass of B atoms segregated at the

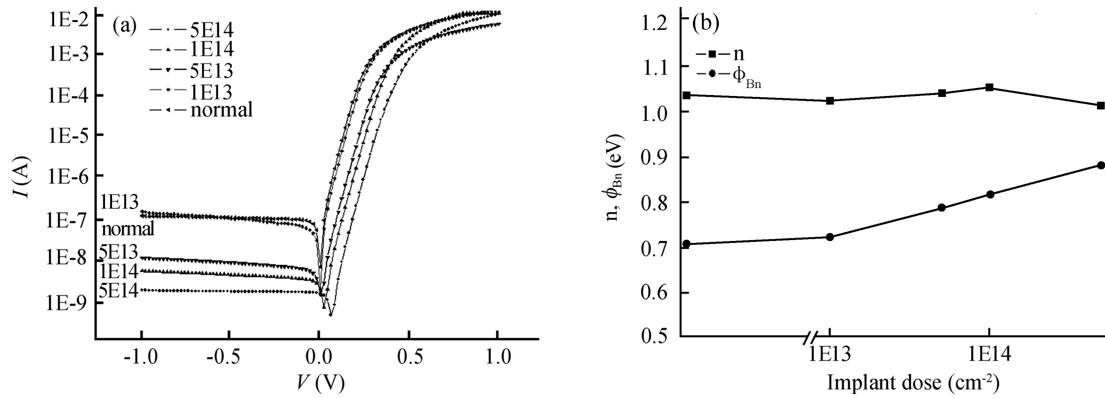


Fig. 4. (a) Abs($I$)–$V$ characteristic curve and (b) $\phi_{Bn}$ and $n$ change curve as the function of implant dose without and with various doses of the dopant segregation process for NiSi/n-Si SJDs.

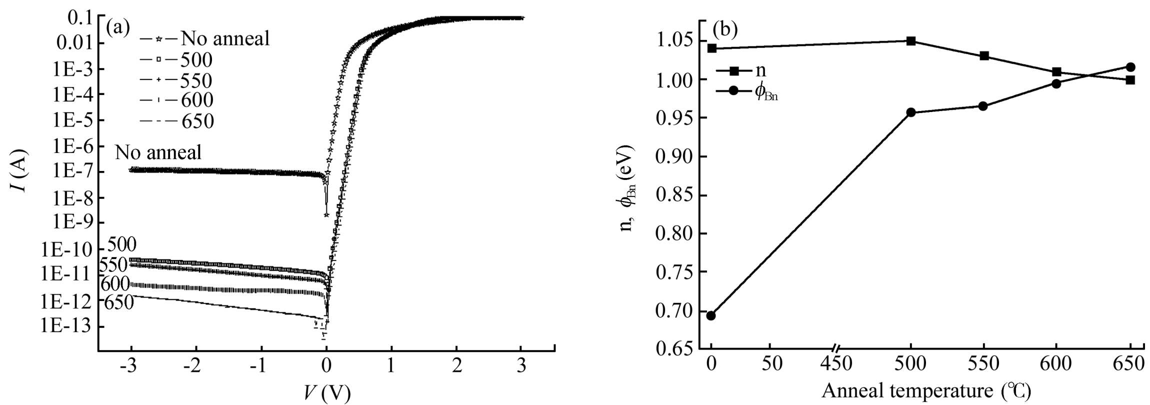


Fig. 5. (a) Abs($I$)–$V$ characteristic curve and (b) $\phi_{Bn}$ and $n$ change curve as the function of the temperature without and with various segregation annealing temperatures of the dopant segregation process for NiSi/n-Si SJDs.

NiSi/Si interface form a thin spike with high doping concentration and the concentration increases with th increased implanting dose[5]. This high concentration range of B accumulated at the NiSi/n-Si interface induces an increase in $\phi_{Bn}$[4]. Furthermore, some of the segregation B atoms replacing Si atoms at the Si side of the interface generate an electric dipole layer across the interface. The B electric dipole layer is expected to be negatively charged and to deform the energy band upward leading to an increase in $\phi_{Bn}$[6–9]. As shown in Fig. 4(b), $\phi_{Bn}$ increases with increased implanting dose and $n$ is near to 1. Because the decrement of the reverse current with increased implanting dose is obvious, the implanting dose is more efficient for tuning $\phi_{Bn}$ at the same segregation annealing temperature.

Other wafers were treated with the dose $1 \times 10^{15}$ cm$^{-2}$ $BF_2$ ion implantation with the same implantation energy as in Fig. 4 and various segregation annealing temperatures (500–650 °C) for 30 s. Figure 5(a) show Abs($I$)–$V$ characteristic curve which were measured with avoiding light, and the reverse current of NiSi/n-Si SJD is decrease with increasing segregation annealing temperature, but the zero point drift phenomenon is disappear. So the reason of zero point drift is that $I$–$V$ characteristic curve measurement is performed without avoiding light environment. And the reason for regular change of zero point is that SJDs with different $\phi_{Bn}$ need different forward voltage to make up for the photocurrent response. Moreover, the greater of $\phi_{Bn}$ needs greater forward voltage to make up for the photocurrent response. So, zero point drift is increasing with the increasing of $\phi_{Bn}$. As show in Figure 5(b), $\phi_{Bn}$ is increasing with the increasing of the segregation annealing temperature. Following the increase of segregation annealing temperature, the decrement of the reverse current is tiny. As shown in Fig. 5(b), $\phi_{Bn}$ increases with increasing segregation annealing temperature and $n$ is also near to 1, but the extent of the increase in $\phi_{Bn}$ is small. The conclusion is that the segregation annealing temperature can only make a fine adjustment of $\phi_{Bn}$ at the same implanting dose. The SBH of the wafer treated with 650 °C of segregation annealing is extrapolated to have $\phi_{Bn}$ = 1.017 eV and $\phi_{Bp}$ = 0.103 eV.

## 4. Summary

In this paper, the post-silicide of dopant segregation process and a method of extrapolating the SBH were described. The effect of different process parameters of dopant segregation, including segregation anneal temperature and implanting dose, on the properties of the NiSi/n-Si SJDs have been studied. The results show that there are two main adjusting mechanisms of the dopant segregation process: one is a thin spike with high doping concentration at the NiSi/Si interface and the other is an electric dipole layer at the NiSi/Si interface. Furthermore, the extent of the adjustment increases with in-

creased implanting dose and segregation anneal temperature. The SBH of the NiSi/n-Si SJD treated with the dose $1 \times 10^{15}$ $cm^{-2}$ $BF_2$ ion implantation and segregation annealing at 650 °C for 30s is extrapolated to have $\phi_{Bn} = 1.017$ eV and $\phi_{Bp} = 0.103$ eV.

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