A reconfigurable analog baseband circuit for WLAN, WCDMA, and Bluetooth*

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Abstract: A reconfigurable analog baseband circuit for WLAN, WCDMA, and Bluetooth in 0.35 μm CMOS is presented. The circuit consists of two variable gain amplifiers (VGA) in cascade and a G_m–C elliptic low-pass filter (LPF). The filter-order and the cut-off frequency of the LPF can be reconfigured to satisfy the requirements of various applications. In order to achieve the optimum power consumption, the bandwidth of the VGAs can also be dynamically reconfigured and some G_m cells can be cut off in the given application. Simulation results show that the analog baseband circuit consumes 16.8 mW for WLAN, 8.9 mW for WCDMA and only 6.5 mW for Bluetooth, all with a 3 V power supply. The analog baseband circuit could provide -10 to $+40$ dB variable gain, third-order low pass filtering with 1 MHz cut-off frequency for Bluetooth, fourth-order low pass filtering with 2.2 MHz cut-off frequency for WCDMA, and fifth-order low pass filtering with 11 MHz cut-off frequency for WLAN, respectively.

Key words: analog integrated circuits; receiver; reconfigurable baseband; analog filter; VGA
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1. Introduction

The mobile phone has evolved into a portable information processing platform due to the rapid development of the information technology. Many wireless applications are being or will be integrated into this platform, such as GPS positioning, digital TV, and WLAN/Bluetooth-based high speed local wireless data transfer. Traditionally, each wireless application should be implemented with a set of standalone hardware, so mobile phone integrating multiple wireless applications would be bulky and costly. To reduce the cost and the volume, reconfigurable wireless transceivers have been proposed in Refs. [1, 2]. The transceiver could be shared among various applications in the greatest degree and would be dynamically reconfigured to satisfy the requirements of different applications.

The reconfigurable analog baseband circuit is one of the key blocks in the reconfigurable wireless transceiver and usually consists of cascaded variable gain amplifiers (VGA) and an active low-pass filter (LPF), as shown in Fig. 1. References [3, 4] have proposed some sort of reconfigurable analog baseband circuits, whose reconfigurability is limited due to the fixed filter-order of the LPF. Another problem is that the bandwidth of the VGAs remains constant and all G_m-cells in the LPF are working in each application. So the power consumption for the different applications varies little and is obviously not optimal since the analog baseband circuit should be designed to satisfy all the requirements of various applications and the design margin is too large for one given application. The cascade biquadratic LPF also suffers a lot from PVT (process, supply voltage and temperature) variation and aging.

In this paper, a novel reconfigurable analog baseband circuit for three different applications (WLAN, WCDMA and Bluetooth) is presented. The circuit consists of two variable gain amplifiers (VGA) in cascade and a G_m–C elliptic low-pass filter (LPF). The filter-order and the cut-off frequency of the LPF could be reconfigured to satisfy the different requirements of various applications. More importantly, in order to achieve the optimum power consumption, the bandwidth of the VGAs could be dynamically adjusted and some G_m cells could be cut off in the given application. The experimental results show that the reconfigurable analog baseband circuit could satisfy the requirements of WLAN, WCDMA and Bluetooth with the optimized power consumption.

2. Analog baseband circuit

Figure 1 shows a block diagram of the reconfigurable analog baseband circuit. The circuit consists of two cascaded VGAs and an elliptic LPF. The requirements for the different applications are fulfilled, which are considered as below.

The bandwidth requirements are fulfilled by changing the topology architecture and relative parameters of the LPF. The cascaded VGAs have a high DC-gain variation range (-10 to $+40$ dB) while the LPF shows a fixed DC-gain (0 dB) to reduce the complexity of the filter. Two continuous-tunable cascaded VGAs have the same topology, but with different transistor sizes, taking into account the linearity requirement and the power consumption.

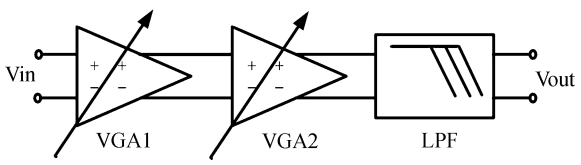

Fig. 1. Block diagram of the reconfigurable analog baseband circuit.

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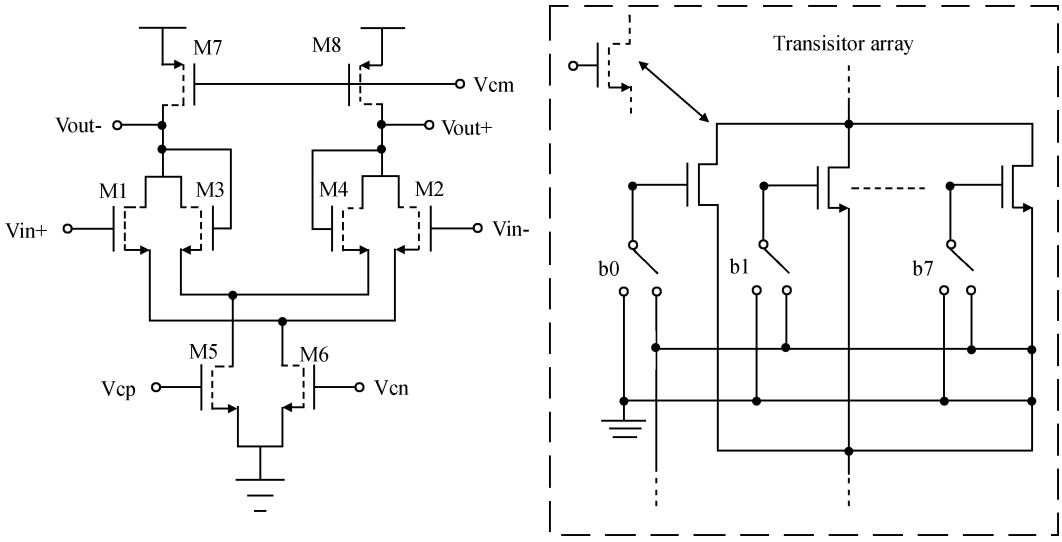

Fig. 2. Schematic of each VGA.

Both VGA1 and VGA2 are designed to provide −5 to +20 dB gain, but the −3 dB bandwidth is set to different values for the different applications: 36 MHz for WLAN, 18 MHz for WCDMA and 10 MHz for Bluetooth. The reconfigurable bandwidth could increase the out-of-band attenuation and optimize the power consumption. The frequency response of the analog baseband circuit is dominated by the LPF, which can be reconfigured to show the different filtering characteristics (the different filter orders and the cut-off frequencies) for different applications: third-order filter with 1 MHz cut-off frequency for Bluetooth, fourth-order filter with 2.2 MHz cut-off frequency for WCDMA, and fifth-order filter with 11 MHz cut-off frequency for WLAN.

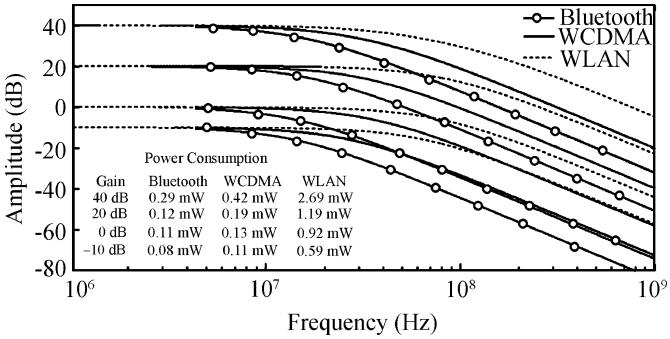

Fig. 3. Amplitude response and power consumption of the cascaded VGAs.

3. Circuit description

The presented analog baseband circuit consists of three cascaded blocks, VGA1, VGA2, and LPF, as shown in Fig. 1. The position of each block in the chain is determined based on the noise and the linearity requirements. The cascaded VGAs provide the gain to reduce the effects of LPF noise on the receiver performance. The LPF is used as the last block to guarantee better linearity performance.

3.1. Variable gain amplifier

The schematic of each VGA is shown in Fig. 2. Each of M1–M8 is implemented as one transistor array. Each transistor array consists of 8 transistors controlled by the control signals b0–b7. When some control signal bi ($i = 0, \ldots, 7$) is high, the corresponding transistor would be connected to the array; when some control signal bi ($i = 0, \ldots, 7$) is low, the gate of the corresponding transistor would be grounded and has no contribution to the array. In this way, the sizes of M1–M8 could be reconfigured to satisfy the different requirements. In order to reduce the complexity, the control signals for the different transistor arrays are the same so that the effective size ratio of the various transistor arrays in the given operation mode is kept constant.

A source coupled pair (M1 and M2) with diode-connected loads (M3 and M4) is used to realize the pseudo-exponential gain control function[6, 7]. Based on the square law, the gain of each VGA is:

$$\text{Gain} = \frac{g_{\text{m1,2}}}{g_{\text{m3,4}}} = \sqrt{\frac{\left(\frac{W}{L}\right)_{1,2}(I_{\text{bias}} + I_{\text{control}})}{\left(\frac{W}{L}\right)_{3,4}(I_{\text{bias}} - I_{\text{control}})}}, \quad (1)$$

where $I_{\text{bias}} + I_{\text{control}}$ is the current of M6 and $I_{\text{bias}} - I_{\text{control}}$ is the current of M5. These two currents are controlled by $V_{\text{cn}} - V_{\text{cp}}$ so that the gain can be adjusted continuously. The sizes of M1 (M2) and M3 (M4) are designed to achieve the required asymmetrical gain range (−5 to +20 dB for each VGA).

The bandwidth of each VGA is determined by the impedance and the capacitance in the output node and can be described as follows:

$$\omega_{-3\text{dB}} = \frac{g_{\text{m3,4}}}{C_{\text{out}}}. \quad (2)$$

The power consumption of the VGAs can be adjusted according to the different bandwidths and the gain requirements. On one hand, for the particular gain, the bandwidth can be adjusted without affecting the gain in order to support the different applications. The bandwidth adjustment is realized by changing the control signal levels (b0–b7) in Fig. 2. By doing

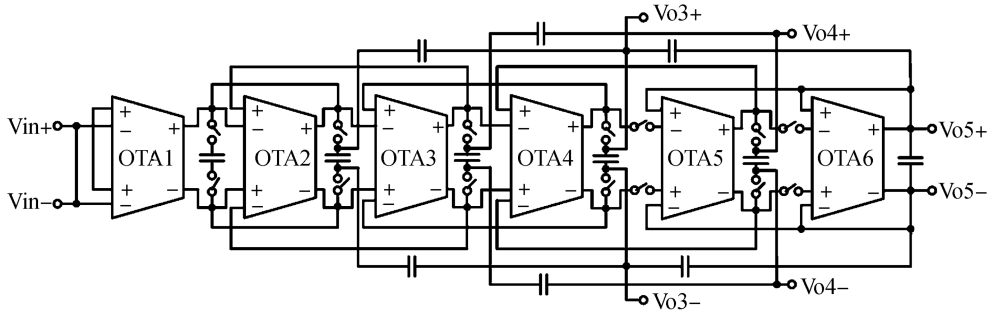

Fig. 4. Block diagram of the LPF.

so, all effective sizes of M1–M8 are adjusted in the same ratio and $g_{m3,4}$ is set to coincide with the required bandwidth. At the same time, DC-gain is not influenced by this process since the effective size ratio of M1/M2 and M3/M4 is kept unchanged. As a result, not only are out-of-band tones better suppressed, but power consumption can also be optimized for the different applications—the circuit does not take unnecessary current to achieve a higher bandwidth than the given application needs.

On the other hand, for the given application, low gain mode brings additional space for the power consumption optimization. As for the given application, $g_{m3,4}$ varies with gain. Lower gain results in higher $g_{m3,4}$ and thus higher bandwidth, which exceeds that which the given application needs. By decreasing the effective size of M1–M8 in the same ratio (changing the control signal b0–b7), we compensate the effect of the gain variation on $g_{m3,4}$ (bandwidth) and consequently minimize the current consumption to achieve the required bandwidth. At the same time, the gain adjustment is not affected by this process.

Moreover, when the required analog baseband chain gain is less than 20 dB, VGA2 could be by-passed through CMOS switches. In this case, VGA2 is completely turned off in order to further reduce the current consumption.

The cascaded VGAs are the main non-linearity sources compared with the LPF. It is necessary to ensure that VGA1 and VGA2 make similar non-linearity contributions to the whole receiver. Otherwise, the linearity performance of the complete chain may be largely limited by one particular block and it becomes not worthwhile to consume the additional current to maintain the high linearity of other blocks. Consequently, for a required chain gain more than 20 dB, VGA1 and VGA2 contribute an identical DC-gain because higher gain means worse linearity performance. Moreover, the amplified input signal by VGA1 places a higher linearity requirement on VGA2 compared to VGA1. The approach adopted here is to implement VGA2 with larger transistor sizes, so that they work in the deeply saturated region and guarantee better linearity performance.

The proposed cascaded VGAs can provide a high gain variation range of –10 to +40 dB for the three applications. Power consumption is optimized according to the bandwidth and gain requirements of each application, as shown in Fig. 3. For the fixed gain, the application with the higher bandwidth requirement calls for more power consumption. Similarly, for the given application, high gain mode consumes more power. So in the given application mode, the power consumption could be minimized based on the specific gain and bandwidth requirements.

3.2. Reconfigurable low-pass filter

The highly tunable elliptic low-pass filter is based on the leap-frog G_m–C RLC ladder topology[7, 8] . Figure 4 shows a block diagram of the LPF. The load capacitor of each OTA is a switched-capacitor array.

The performance of the LPF depends on the topology architecture. Unlike the traditional cascaded biquad implementation[3, 4], nearly all the performance of this LPF, such as cut-off frequency, filter order and transition band ratio, as well as power consumption, can be reconfigured. The LPF can be configured to three different modes for WLAN, WCDMA, and Bluetooth, respectively. Each mode exhibits different cut-off frequencies, different transition band ratios and different power consumptions. In this work, we use a third-order filter for Bluetooth, a fourth-order filter for WCDMA, and a fifth-order filter for WLAN. Finally, the different output nodes are used for different applications. The proposed structure also suffers less from the process variation.

The operational transconductance amplifier (OTA) in the LPF is presented in Fig. 5[9]. A linear cross-coupled quad input stage with an enhanced folded-cascode circuit is utilized to achieve high linearity and large output resistance, and the floating voltage source is used to adjust the transconductance of OTA so that the transconductance of OTA is reconfigured.

The reconfigurable G_m–C elliptic low-pass filter exhibits the following characteristics. (1) Highly tunable performance: not only bandwidth, but also filter order, and transition band ratio of the proposed low-pass filter can be adjusted to satisfy the requirements for the different applications. It has much more flexibility for designers to make tradeoffs between power consumption and filter selectivity than traditional programmable filters. (2) Low power consumption: as the key feature of a wireless receiver, the power consumption of the LPF is optimized in several ways. First, OTA5 and/or OTA6 are turned off to reduce filter order in the case that the filter selectivity is not a dominant factor. Also, the bias condition of each OTA is adjusted based on the different bandwidth requirements in order to reduce the current consumption. (3) High linearity: a high linear range is achieved due to the cross-coupled input stage of the presented OTA. For an input signal magnitude of less than 600 mV, the transconductance fluctuates a little, causing total harmonic distortion less than 0.1%.

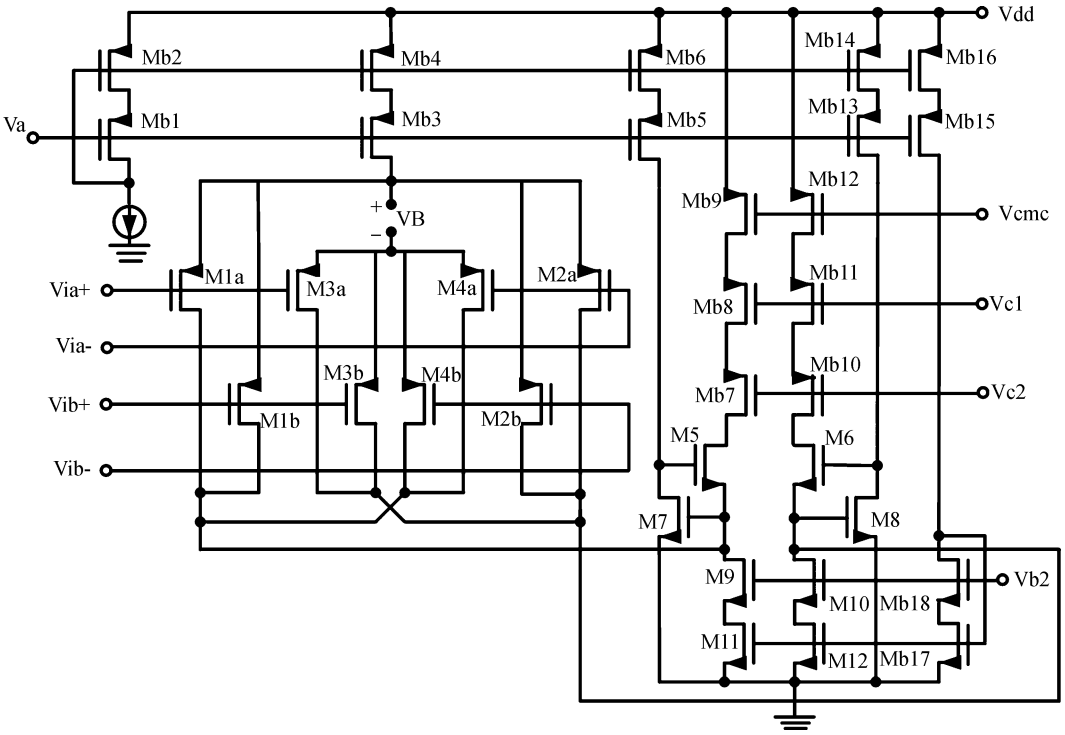

Fig. 5. OTA used in the LPF.

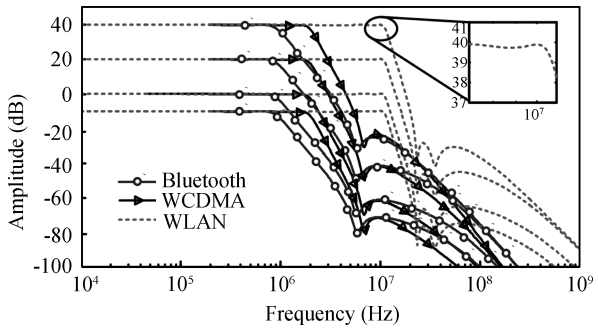

Fig. 6. Amplitude responses of the analog baseband circuit (simulation results).

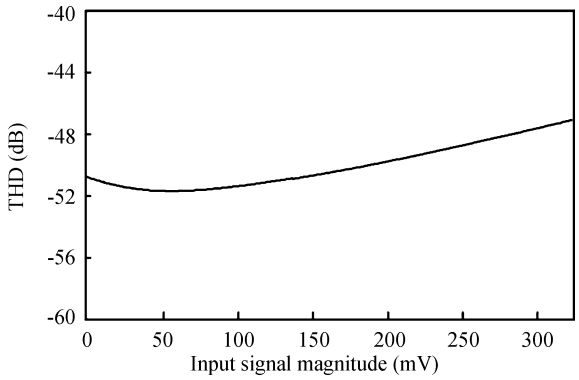

Fig. 7. THD for different input signal amplitudes.

4. Simulation results

The analog baseband circuit has been implemented in 0.35 μm CMOS. The amplitude responses for the different gain levels and bandwidth requirements are presented in Fig. 6. The DC-gain range for all three applications is -10 to $+40$ dB. The transition band ratio and the -3 dB bandwidth are different for the different applications.

Linearity performance is evaluated with a single tone test, but with different input signal frequencies and magnitudes. Figure 7 shows the total harmonic distortion in WCDMA mode for a 1.4 MHz input signal with different magnitudes. The chain gains are set to ensure that output signal magnitude is 100 mV. The simulation results show that THD does not fluctuate much while the input signal magnitudes change.

Figure 8 shows the output frequency spectrum of the analog baseband circuit in WCDMA maximum gain mode when a single tone is applied. Because of the relatively small magnitude, the second harmonic and the fourth harmonic, as well as other high harmonics, can not be observed.

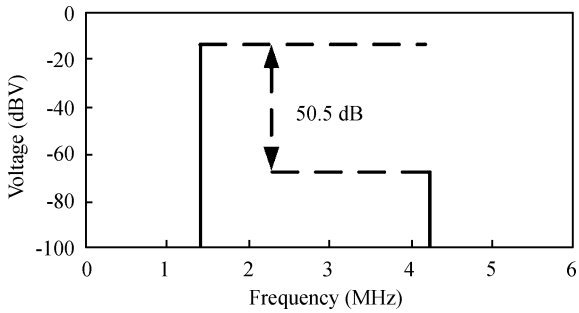

Fig. 8. Output frequency spectrum of the analog baseband circuit for 1.4 MHz single tone input (WCDMA, maximum gain).

Power consumption is optimized according to the given application. It goes from 16.8 mW for WLAN down to 6.5 mW for Bluetooth when the gain is set to the maximum value of

Table 1. Performance summary.

	Parameter	Value		
		Bluetooth	WCDMA	WLAN
This work (simulation results)	Filter order/ Bandwidth (MHz)	Third/1	Fourth/2.2	Fifth/11
Technology: 0.35 μm CMOS	Gain range (dB)	−10 to 40	−10 to 40	−10 to 40
Power supply: 3 V	Pass band ripple (dB)	0.3	0.4	0.3
	Linearity	THD = 50.12 dB (G = 40 dB, V_{in} = 0 dBm @ 0.8 MHz)	THD = 50.4 dB (G = 40 dB, V_{in} = 0 dBm @ 1.4 MHz)	THD = 59.1 dB (G = 40 dB, V_{in} = 0 dBm @ 9 MHz)
	Total power (G = 40dB) (mW)	6.5	8.94	16.8
	VGA1 power (mW)	0.12	0.19	1.19
	VGA2 power (mW)	0.17	0.23	1.5
	LPF power (mW)	6.2	8.51	14.1
Ref. [3]	Filter-order/Bandwidth (MHz)	Fourth/1	Fourth/2.2	Fourth/11
Technology: 0.13 μm CMOS	Gain range (dB)	−6 to 69	4–39	4–39
Power supply: 2.5 V	Total power (G = 40 dB) (mW)	32.5	32.5	55

*In this work, the gain and the bandwidth of the proposed VGA, the filter-order and the bandwidth of the proposed LPF can all be adjusted, while in Ref. [3], only the gain of VGA and the bandwidth of LPF can be adjusted.

40 dB.

Table 1 summarizes the performance of the complete reconfigurable baseband circuit and gives a comparison with the chip measurement results of previous work[3].

5. Conclusion

In this paper, a reconfigurable analog baseband circuit for WLAN, WCDMA and Bluetooth is presented. Bandwidth, gain, filter-order, and filter cut-off frequency can all be reconfigured, which guarantees maximum performance flexibility. Power consumption is remarkably optimized based on the different bandwidth and gain requirements of each application.

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