Design of a high-order single-loop ΣΔ ADC followed by a decimator in 0.18 μm CMOS technology

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Abstract: This work presents an oversampled high-order single-loop single-bit sigma–delta analog-to-digital converter followed by a multi-stage decimation filter. Design details and measurement results for the whole chip are presented for a TSMC 0.18 μm CMOS implementation to achieve virtually ideal 16-b performance over a baseband of 640 kHz. The modulator in this work is a fully differential circuit that operates from a single 1.8 V power supply. With an oversampling ratio of 64 and a clock rate of 81.92 MHz, the modulator achieves a 94 dB dynamic range. The decimator achieves a pass-band ripple of less than 0.01 dB, a stop-band attenuation of 80 dB and a transition band from 640 to 740 kHz. The whole chip consumes only 56 mW for a 1.28 MHz output rate and occupies a die area of 1×2 mm^2.

Key words: oversampled analog-to-digital converter; sigma–delta modulator; decimator; switched capacitor
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1. Introduction

Oversampled sigma–delta modulation has been widely used for its low-complexity analog circuitry and robustness in preference to other A/D conversion techniques[1, 2]. In the main types of oversampled sigma–delta modulation, however, high-order single-loop single-bit designs are the most attractive architecture whenever high SNDR (signal-to-noise-and-distortion ratio), simple circuit design and good idle-tone performance are important[3–6]. The major obstacle to overcome is the issue of stability, but once a methodology has been established, designing a new loop filter is a simple matter of running a few programs and checking the result with a discrete-time simulator. Although use of a multi-bit quantizer could avoid the stability problem which is caused by integrator overload, the high linearity of a single-bit quantizer is most attractive in many circumstances. The following stage—decimation filter—used for the sigma–delta analog-to-digital converter (ADC) has a special topology and flexibility in realization. Its architecture and performance should be designed in terms of the requirements of the sigma–delta modulator and, of course, the area and power should also be considered and optimized.

In this paper, the architecture and the characteristics of the high-order single-loop single-bit ΣΔ modulator are presented. The implementation of the modulator with switched-capacitor circuits is presented. Design of the multi-stage decimation filter is described. Since the chip includes analog and digital circuits, attention should be paid to the layout strategy, which is discussed in this paper.

2. Modulator architecture

All sigma–delta feedback topologies may be characterized by two transfer functions: the NTF (noise transfer function) and the STF (signal transfer function). The NTF determines to what extent the quantization noise is reduced in a given bandwidth and hence determines the overall SNDR of the converter. Depending on the chosen architecture, it may or may not be possible to independently specify the STF. From a circuit design standpoint, it is desirable to use integrators as the fundamental active building block. This allows SC (switched-capacitor) circuits to be designed in a parasitic-insensitive manner[7]. Meanwhile, by adding a small negative-feedback term around pairs of integrators in the loop filter, it is possible to move the open-loop poles, which become NTF zeros when the loop is closed, away from dc along the unit circle. From the consideration mentioned above, a CIFB (cascade-of-integrator-feedback) topology is chosen in this work.

Firstly, the fundamental theory of CIFB topology should be introduced. Figure 1 shows a second-order single-loop single-bit CIFB sigma–delta modulator topology. Coefficients a_1, a_2 are the feedback gain factors from the quantizer output to the input of the integrator; b_1, b_2 are the feed-forward gain factors from the signal input; g_1 is the small feedback term from the output of the second integrator. Note that with NTF omission coefficient b_2, the system will yield a maximally-flat STF.

An analysis of the architecture is given as follows. Nearly all single-quantizer loops can be equivalently described by

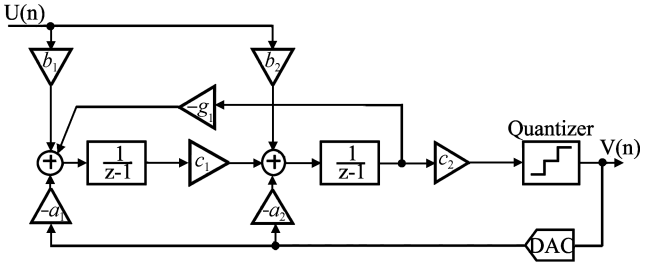

Fig. 1. Second-order CIFB sigma–delta modulator.

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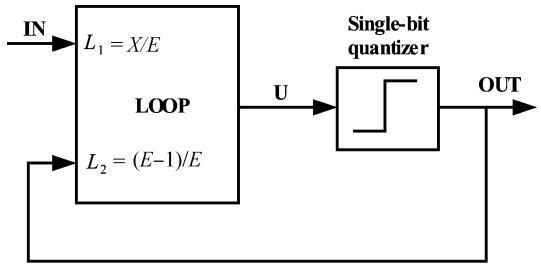

Fig. 2. Universal sigma–delta structure.

the architecture in Fig. 2.

Then the NTF and STF can be obtained respectively as

$$E(z) = \frac{1}{1 - L_2(z)} \tag{1}$$

and

$$X(z) = \frac{L_1(z)}{1 - L_2(z)}. \tag{2}$$

When the chain structure of two integrators with distributed feed-back (a_1, a_2) and distributed feed-forward (b_1, b_2) inputs is considered, the L_1, L_2, NTF and STF are given respectively by

$$L_1(z) = \frac{b_1}{(z-1)^2} + \frac{b_2}{z-1}, \tag{3}$$

$$L_2(z) = -\left[\frac{a_1}{(z-1)^2} + \frac{a_2}{z-1}\right], \tag{4}$$

$$E(z) = \frac{(z-1)^2}{D(z)}, \tag{5}$$

$$X(z) = E(z)L_1(z) = \frac{b_1 + b_2(z-1)}{D(z)}, \tag{6}$$

where $D(z)$ is the correct term to flatten the high-frequency portion of $E(z)$ and $X(z)$. In practice, $L_2(z)$ has high gain in the band of interest and is thus responsible for attenuating the quantization noise. Also, $E(z)$ and $X(z)$ share the same poles, unless pole-zero cancellation occurs by judicious choice of $L_1(z)$. Therefore, STF($X(z)$) and NTF($E(z)$) for the second-order CIFB structure shown in Fig. 1 can be given respectively by

$$X(z) = \frac{b_2c_2(z-1) + b_1c_1c_2}{(z-1)^2 + a_2c_2(z-1) + a_1c_1c_2 + g_1c_1}, \tag{7}$$

$$E(z) = \frac{(z-1)^2 + g_1c_1}{(z-1)^2 + a_2c_2(z-1) + a_1c_1c_2 + g_1c_1}. \tag{8}$$

The dynamic range of a sigma–delta modulator and the relationship of SNR (signal-to-noise ratio) and B are given respectively by

$$\mathrm{SNR} = \frac{3\pi}{2}\frac{2L+1}{\pi^{2L+1}}(2^B - 1)^2 \times \mathrm{OSR}^{2L+1}, \tag{9}$$

$$B = \frac{\mathrm{SNR} - 1.76}{6.02}, \tag{10}$$

where L is the order of the modulator, B is the number of bits of the quantizer and OSR is the oversampling ratio. Therefore, in order to achieve a resolution of about 15 bits, SNR should be at least 92 dB according to Eq. (10). Then, L and OSR can be established by Eq. (9). With these theories mentioned above and according to the required SNR and signal bandwidth, a fourth-order CIFB topology with an oversampling ratio of 64 is adopted. Then, the NTF of this work can be established by Eqs. (1)–(8) and optimized by a scaling process:

$$\mathrm{NTF}(z) = \frac{(z^2 - 1.996z + 1)(z^2 - 1.998z + 1)}{(z^2 - 1.492z + 0.5643)(z^2 - 1.701z + 0.7868)}. \tag{11}$$

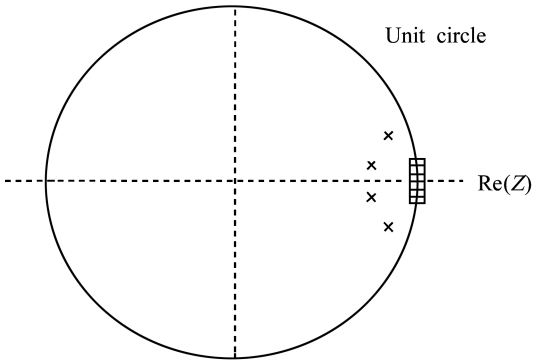

Fig. 3. Poles and zeros of the synthesized NTF.

Figure 3 shows the poles and zeros of the NTF(z) and the architecture created in the MATLAB is shown in Fig. 4.

Assisted by computer calculations and simulations, the loop filter coefficients can be established and are given in Table 1. The practical values of the coefficients make the implementation of the switch-capacitor easier. With these coefficients, the ideal SNR can reach 101.3 dB over a 640 kHz bandwidth and the effective number of bits (ENOB) is 16.53 bits. The stable dc range is –0.7 to +0.7 of the full scale.

3. Switched-capacitor implementation

Fully differential CMOS implementation of the modulator schematic is show in Fig. 5. The feedback paths are implemented by switched capacitor networks. Amplitude information is not used at all due to the use of the single-bit quantizer.

3.1. Op-amp design

Since the SNR of any given order modulator can be increased by increasing the oversampling ratio, speed is of primary interest. If the op-amp is fast enough to allow the circuit to settle completely, the exact nature of the settling is unimportant. The fully differential amplifier should have a fairly linear open-loop transfer function and possess a reasonable amount of low-frequency open-loop gain, so the distortion of the amplifier will be reduced even further when placed in a closed loop configuration[8]. The op-amp architecture used in this context is shown in Fig. 6. The gain-boost level is adopted in order to enlarge the open-loop gain which affects the SNR of the modulator. The module SC_CMFB in Fig. 6 is the switched capacitor common-mode-feedback circuit which is shown in Fig. 7. A summary of the OTA (operational transconductance amplifier) specifications is shown in Table 2. Since OTA1 and OTA2 dominate the performance of the modulator, their specifications should be much stricter than those of OTA3 and

Table 1. Loop filter coefficients.

Coefficient	a_1	a_2	a_3	a_4	b_1	b_2	b_3	b_4
Simulation value	0.1212	0.1905	0.3076	0.2010	0.1212	0	0	0
Practical value	4/33	4/21	4/13	1/5	4/33	0	0	0
Coefficient	c_1	c_2	c_3	c_4	g_1	g_2		
Simulation value	0.1739	0.3343	0.2857	1.000	0.003	0.011		
Practical value	4/23	1/3	2/7	1	3/1000	1/100		

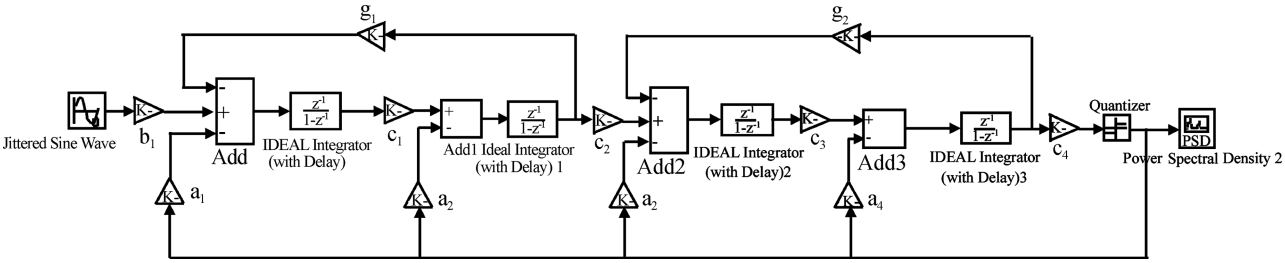

Fig. 4. A fourth-order CIFB sigma–delta modulator with two distributed feedback factors.

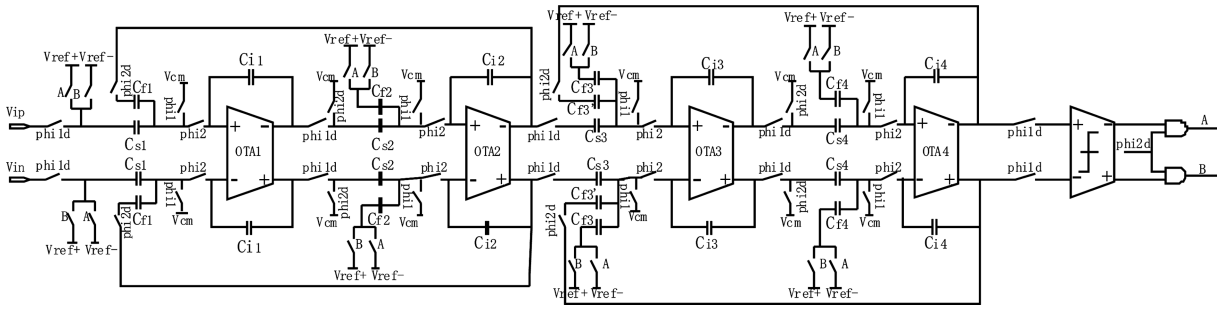

Fig. 5. Fully differential fourth-order single-bit sigma–delta modulator implemented with SC circuits.

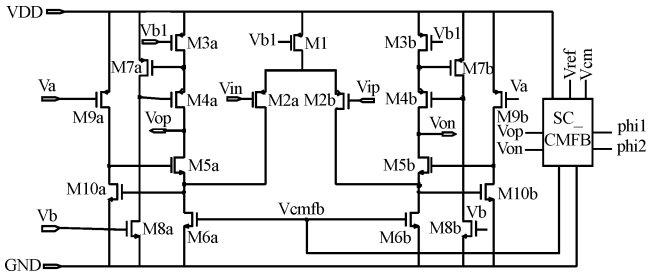

Fig. 6. Fully differential gain-boost op-amp with SC_CMFB.

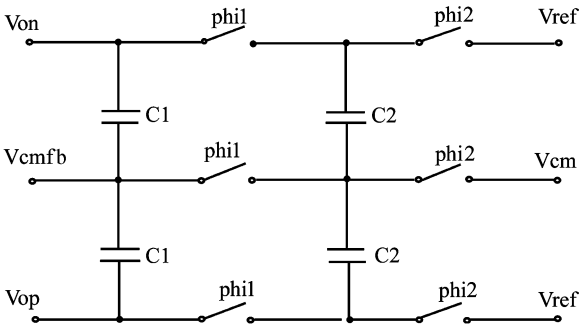

Fig. 7. SC_CMFB used for the op-amp.

OTA4. The simulation results of the first two OTAs (OTA1 and OTA2) are shown in Fig. 8.

3.2. One-bit quantizer

The quantizer is realized with a dynamic comparator and an SR latch. The comparator is very power efficient because it is a pure dynamic circuit. Offset voltage is mainly determined by matching of the input transistors, and attention should be paid to this in the layout design. However, the requirement for the quantizer is relaxed due to the mechanism of the sigma–delta modulator. Figure 9 shows the dynamic quantizer used in this work.

Table 2. Specifications of OTAs.

OTA specifications	OTA1,2	OTA3,4
Finite DC gain (dB)	99	65
Unit gain bandwidth (MHz)	350 (C_{load} = 7 pF)	100 (C_{load} = 4 pF)
Slew rate (V/μs)	224 (C_{load} = 7 pF)	140 (C_{load} = 4 pF)
Phase margin (degree)	69	65
Max I_{diss} (mA)	5.8	2.1
Max P_{diss} (mW)	10.44	3.78

3.3. Switches, capacitors and clock generator

In any switching scheme, it is desirable to minimize the number and sizes of switch devices. This will minimize parasitic parameters such as junction capacitances to the well and substrate and channel charges that degrade circuit performance. The use of minimum-gate-length N-devices as switches yields the minimum device size for a given on-resistance. Since the sampling switches must conduct over a wide range of voltages, it is necessary to use a full CMOS

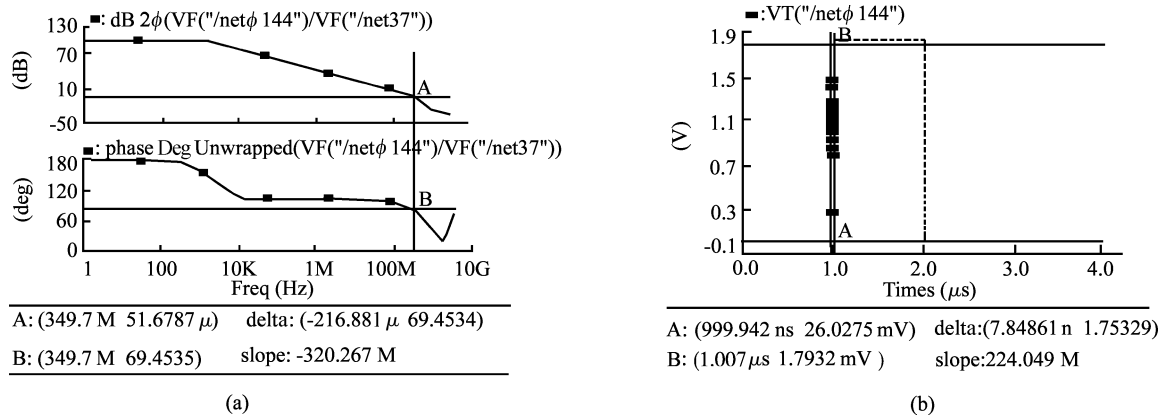

Fig. 8. Simulation results of OTA1, 2: (a) Simulation results of phase margin, open-loop gain, and unit-gain-bandwidth; (b) Simulation result of slew rate.

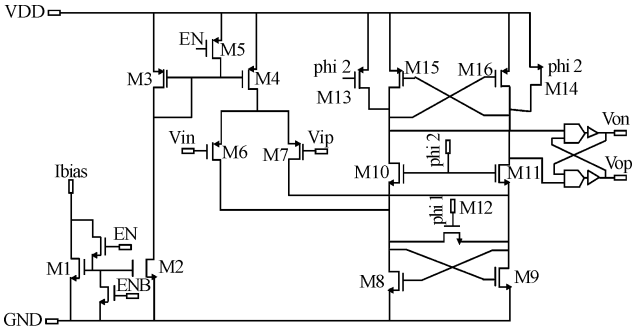

Fig. 9. Dynamic circuit of the quantizer.

transmission gate switch. However, even a full CMOS transmission gate may not be turned on over a wide range of signal voltages. So, making the device in the well a switched-tub switch may be necessary[9].

From the KT/C noise considerations, capacitors are sized by a scaling process. Since the first-stage capacitors are the dominant noise source, large capacitors should be used for the first-stage to meet the required performance of the modulator. The input referred thermal noise of first integrator can be approximated as

$$v_{\mathrm{n,in}}^2 = \frac{4}{3}\frac{kT}{C_{\mathrm{total1}}}\gamma(1+n_{\mathrm{t}}) + \frac{kT}{C_{\mathrm{s1}}}, \tag{12}$$

where k is Boltzmann's constant, T the absolute temperature, C_{total1} the total effective load capacitor at the first op-amp output in the integration phase, γ the feedback factor in the integration phase, C_{s1} the input sampling capacitor of the first stage and n_{t} a noise contribution factor that depends on the op-amp architecture. The noise requirement is relaxed due to the oversampling since only a small part of the noise falls in the signal band. Thermal noise power should be smaller than the quantization noise:

$$v_{\mathrm{n,in}}^2 < \frac{\mathrm{FS}^2}{2^{2N+2}\times 3}\times \mathrm{OSR}, \tag{13}$$

where N is the number of bits of the modulator, FS the full-scale swing of the input signal and OSR the oversampling ratio. Taking the thermal noise into account the signal-to-noise ratio of the converter can be calculated as

$$\mathrm{SNR} = 10\lg\frac{P_{\mathrm{signal}}}{P_{\mathrm{q}}+P_{\mathrm{n}}}, \tag{14}$$

where P_{signal} is the signal power, P_{q} the quantization noise power and P_{n} the thermal noise power. If the thermal noise power is equal to the quantization noise power, the SNR will decrease by 3 dB. Therefore it is necessary to make the thermal noise significantly smaller than the quantization noise to avoid decrease of the SNR. The thermal noise is reduced by increasing the capacitors in the circuit.

However, the ratios of the sampling capacitors and the integrator capacitors should be the same as the values provided in Table 1. So, if the sampling capacitors are chosen to be too large, the integrator capacitors will also be large, so that it is difficult to design the op-amps since the load capacitors limit the bandwidth of the op-amps. Therefore, there is a trade-off between the aspects mentioned above. Of course, the die area of the capacitors and the power dissipations of the op-amps are also important aspects which should be considered carefully. Assisted by the considered aspects and the simulation process, the values of the capacitors used in this paper are presented in Table 3.

A basic two-phase non-overlapping clock is used in this context. The additional clocks phi1d and phi2d are identical to phi1 and phi2, except for a delay in the falling edge. In order to reduce the nonlinearity effects of charge injection, switches connected to the signal input are clocked by phi1d and phi2d, while switches connected to the input of the op-amp are clocked by phi1 and phi2.

4. Decimation filter

Good decimator designs places the re-sampling within the filter so that sample values not needed for the output are not calculated[10]. In this context, the oversampling rate is as much as 64 times higher than the Nyquist rate. In order to reduce the sampling rate to the Nyquist rate without aliasing noise into the baseband, a digital decimation filter is used. The primary purpose of the digital filter stage of the sigma–delta modulator is to filter noise which would be aliased back into the baseband. The secondary purpose is to take the 1 bit data stream which has a high sample rate and transform it into a 16 bit data stream at the Nyquist sampling rate[11].

There are a number of factors that make it difficult to

Table 3. Capacitor values of the modulator.

Capacitor	C_{s1}	C_{i1}	C_{f1}	C_{s2}	C_{i2}	C_{f2}	C_{s3}	C_{i3}	C_{f3}	C'_{f3}	C_{s4}	C_{i4}	C_{f4}
Value (pF)	0.8	6.6	0.02	0.6	3.45	0.66	0.6	1.8	0.55	0.02	0.4	1.4	0.28

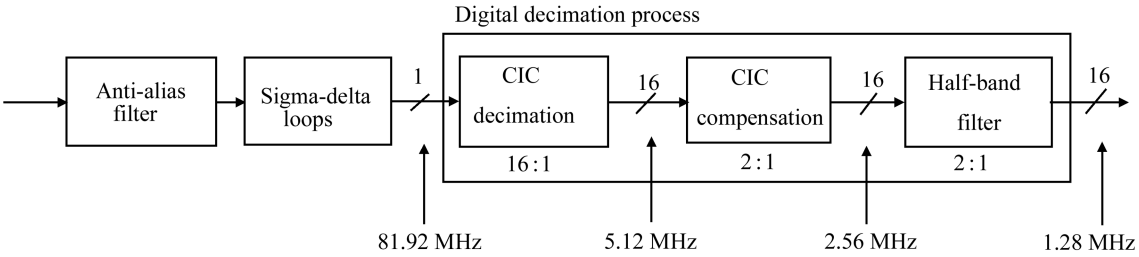

Fig. 10. Digital decimation process.

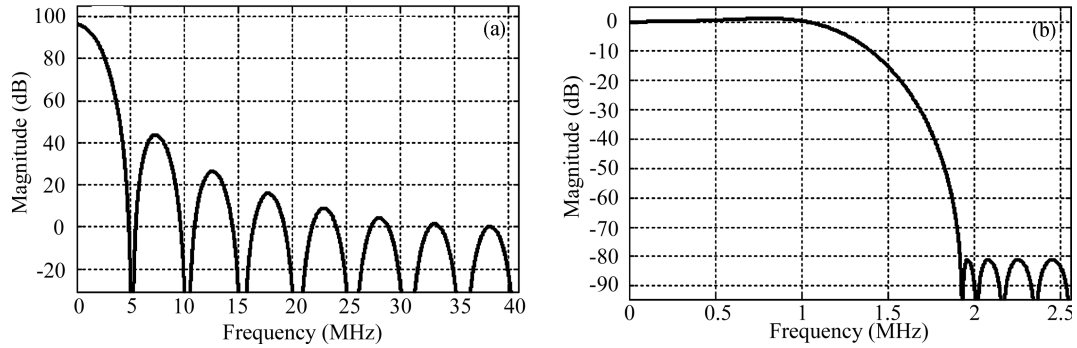

Fig. 11. Magnitude response of (a) CIC decimator and (b) CIC compensator.

implement the digital decimation filter, for example, the high input sampling rate and the intensive signal processing algorithms in real time that the digital decimation filter must perform. Figure 10 shows the architecture of the digital decimation filter adopted in this paper. The first stage is a CIC (cascaded integrator comb) filter, which is the simplest and most economical filter since it does not require a multiplier. However, the CIC filter output has a magnitude droop in the pass-band. A CIC compensation filter is used to compensate the CIC filter, and its coefficients are computed to equalize the baseband frequency response to a flat response within a required scale. In fact, the CIC compensation filter is a FIR (finite impulse response) filter. The third stage is a half-band filter, which is based on a symmetrical FIR design and approximately half of the filter coefficients are exactly zero. So, the number of multiplications in implementing the half-band filter is one-fourth of that needed for arbitrary FIR filter designs[12].

The output signal from the sigma–delta loops is sampled at 81.92 MHz and has a resolution of 1 bit. The CIC decimator has a decimation factor of 16, so the sampling rate becomes 5.12 MHz, one-sixteenth of the original sampling rate. The CIC compensation filter and the half-band filter have the same decimation factor of 2. Finally, the sampling rate is decimated to 1.28 MHz, which is the Nyquist rate and has a resolution of 16 bits. Figure 11 shows the magnitude responses of the CIC decimator and the CIC compensator. Since the coefficients of the CIC decimator are not normalized, the magnitude gain is not 0 dB. In fact, when realizing the filter, normalizing is done. The CIC compensator has an ascending trend in the pass-band to compensate the droop of the CIC filter. The transition bands

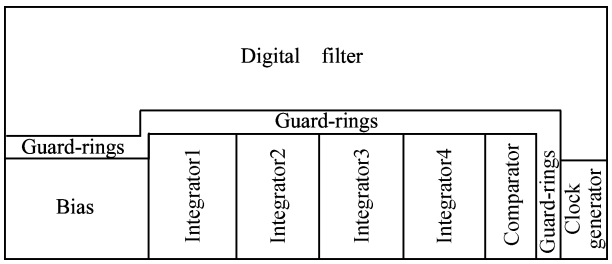

Fig. 12. Floor plan of the whole layout.

of the CIC filter and CIC compensator could be relaxed since there is a half-band filter behind to limit the cut-off frequency.

5. Layout strategy

This section presents the floor planning of the fourth-order single-loop sigma–delta modulator and the decimator. The floor plan of the whole circuit is shown in Fig. 12. The analog part is separated from the digital part by guard-rings to minimize interference from the digital part. On-chip decoupling capacitances are widely used at the power supply and bias nodes. All the analog parts are laid out symmetrically as much as possible to reach the maximum common-mode rejection ratio. In the layout, all differential signals are routed in parallel to reduce differential mode couplings. Sensitive nodes are shielded for good isolation and dummies are added to encircle the capacitor arrays in order to reduce proximity effects. Matched transistors are placed close to each other using an inter-digitated finger layout style. The analog circuits should have a different set of supplies from the noisy digital circuits. In addition, critical analog devices and signals should

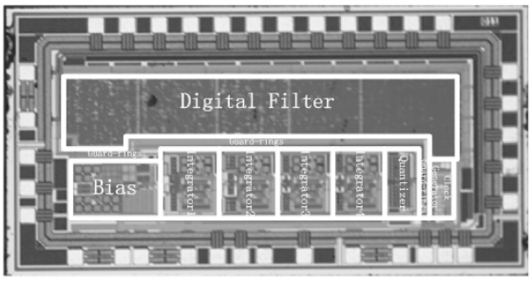

Fig. 13. Die microphotograph.

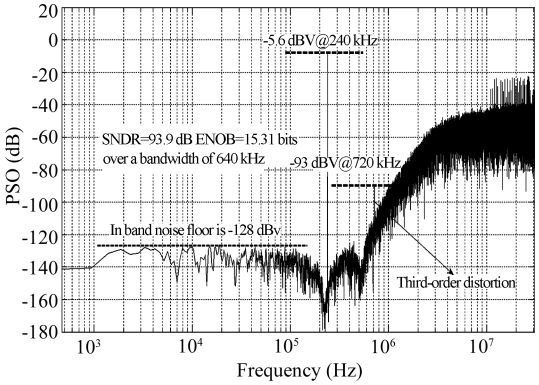

Fig. 14. Measured output spectrum of the modulator.

be placed far away from the digital circuits. Precautions have been taken in pad assignments to improve the ADC performance.

6. Experimental results

Figure 13 shows a die microphotograph of the prototype fabricated in TSMC 0.18 μm CMOS technology. The whole chip including analog modulator and decimation filter occupies 1×2 mm^2 with pads and dissipates 56 mW from a 1.8 V supply. The FFT of the modulator output for a –5.6 dBV @ 240 kHz input sine-wave sampled at 81.92 MHz is shown in Fig. 14. Third-distortion appears at 720 kHz with a value of –93 dBV, and the noise floor in the band is –128 dBV. There are two attenuated points bred by the distributed feedback factors over the nearly flat in-band and the ENOB reaches 15.31 bit for an input level of –5.6 dBV. Due to the impact of overload noise, idle channel tone noise, and switching activity, especially that in the I/O buffers which are distributed along the chip through the pad ring, the experimental peak SNR decreases by about 7 dB compared to the ideal one. Figure 15 presents the ideal and experimental SNR versus the input level for a 64 over-sampling-rate.

7. Conclusions

This design exploits a high-order single-loop single-bit structure to implement a high performance sigma–delta ADC.

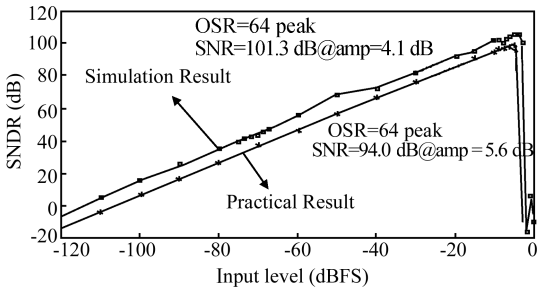

Fig. 15. Measured peak SNR versus input amplitude.

Following the modulator, a digital filter consisting of a CIC decimator, a CIC compensator and a half-band filter has been designed and optimized in this paper. Filtered by the digital filter, the one-bit data streams are transformed to a 16 bits digital signal. Measurement results of the test chip designed in 0.18 μm CMOS technology have proved this.

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