Thermal characteristics investigation of high voltage grounded gate-LDMOS under ESD stress conditions*

Sun Weifeng(孙伟锋)†, Qian Qinsong(钱钦松), Wang Wen(王雯), and Yi Yangbo(易扬波)

(National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China)

Abstract: The thermal characteristics of high voltage gg-LDMOS under ESD stress conditions are investigated in detail based on the Sentaurus process and device simulators. The total heat and lattice temperature distributions along the Si–SiO_2 interface under different stress conditions are presented and the physical mechanisms are discussed in detail. The influence of structure parameters on peak lattice temperature is also discussed, which is useful for designers to optimize the parameters of LDMSO for better ESD performance.

Key words: thermal characteristic; gg-LDMOS; ESD stress condition
DOI: 10.1088/1674-4926/30/10/104004 **EEACC:** 2500

1. Introduction

LDMOS is widely used in smart power ICs and driver ICs for its compatibility with standard CMOS technology[1, 2]. In these applications, in order to improve the reliability, ESD (electrostatic discharge) characteristics of LDMOS must be considered. ESD is an electrical overstress event that transfers a finite amount of charge between two objects at different potentials[3]. Such an event accounts for more than 25% of the failures throughout integrated circuit life[4]. In recent years, a great deal of literature on the ESD characteristics of LDMOS has been published. Reference [5] analyzed the triggering voltage, drain bulk breakdown voltage, holding voltage, snapback voltage, triggering current and hole triggering current of 40 V-LDMOS under ESD stress by means of TLP measurements/HBM testing. Reference [6] studied the influence of structure and process parameters on the ESD characteristics of LDMOS. Reference [7] addressed several new embedded SCR approaches which provided extreme ESD robustness based on the LDMOS/CMOS process. In these papers, the electric characteristics have been discussed in detail. However, the thermal characteristics of LDMOS under ESD zap conditions have not been analyzed in detail, although they are very important for understanding the ESD characteristics of LDMOS.

The purpose of this paper is to investigate the thermal characteristics of high voltage gg (grounded gate)-LDMOS under ESD stress conditions, including the first breakdown region, triggering point, snapback regime and the second breakdown point. After that, the influence of structure parameters on peak lattice temperature is also discussed in terms of the Sentaurus device simulation results.

2. Device structure and simulation conditions

Figure 1 shows an LDMOS structure generated from the Synopsys Sentaurus process. The concentration of the N-drift is 2.5×10^{16} cm^{-3}. The N-drift length and poly field-plate are 10 μm and 5 μm, respectively. L is the gate length of the LDMOS. GSCS is the distance between gate and source contact. GDCS is the distance between field oxide edge and drain contact. The breakdown voltage is 108 V. In the Sentaurus device simulation, the source, gate and substrate are all grounded. We suppose that every contact zone is a thermal electrode and the thermal resistance is zero. HBM ESD stress is added at the drain contact.

3. Thermal characteristic discussion

Figure 2 defines the characteristic quantities of the high

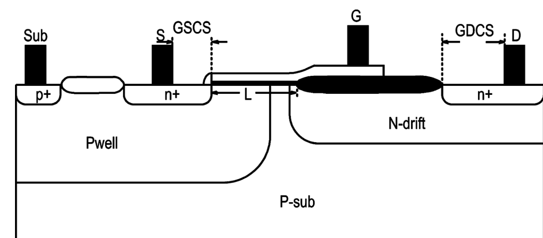

Fig.1. Cross-section view of the LDMOS.

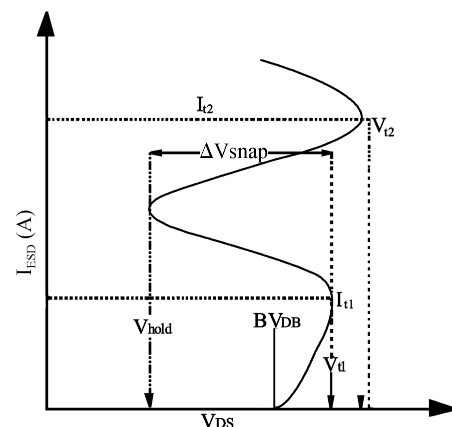

Fig. 2. Snapback I–V curve of gg-LDMOS.

* Project supported by the Natural Science Foundation of the Jiangsu Province (No. BK2008287) and the Advanced Research of National Natural Science Foundation of Southeast University (No. XJ2008312).

† Corresponding author. Email: swffrog@seu.edu.cn

Received 3 April 2009, revised manuscript received 29 April 2009 © 2009 Chinese Institute of Electronics

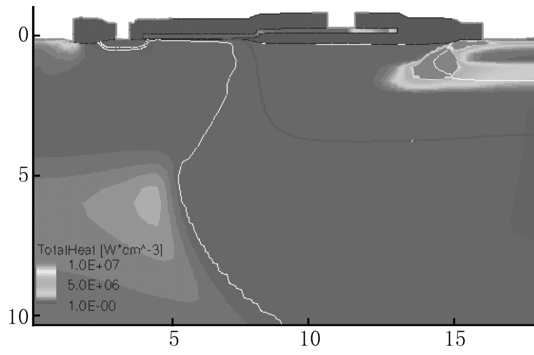

Fig. 3. Total heat distribution of gg-LDMOS at the first breakdown point.

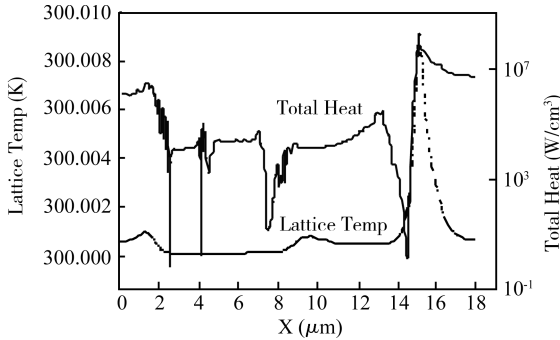

Fig. 4. Total heat and lattice temperature distribution along the Si–SiO_2 interface at the first breakdown point.

current *I–V* curves: the first breakdown voltage BV_{DB}, triggering voltage V_{t1}, holding voltage V_{hold}, snapback voltage ΔV_{snap}, the second breakdown voltage V_{t2}, triggering current I_{t1}, and the second breakdown current I_{t2}. In the following discussion, the LDMOS will be divided into the four work points.

3.1. First breakdown point

At the first breakdown point, the total heat distribution of high voltage gg-LDMOS at the first breakdown point can be seen in Fig. 3. The heat peak is near the n^+/n^- region. The total heat includes Joule heat and Thomson heat. The Thomson heat can be expressed by

$$H_T = -\boldsymbol{J}_n \cdot T\nabla P_n - \boldsymbol{J}_p \cdot T\nabla P_p. \quad (1)$$

At the beginning of the ESD current stress, the injection current is converted to electron current through the n^+ drain. According to the first term of Eq. (1), the electron current will result in a Thomson heat increase near the n^+ drain, which is in agreement with the simulation results. Figure 4 is the total heat and lattice temperature distribution along the Si–SiO_2 interface at the first breakdown point. We can see the lattice temperature peak is also near the n^+/n^- region. The lattice temperature is decided by the current and electric field. At the beginning of ESD current stress, the current is small and mainly near the n^+ drain, so the lattice temperature peak is near the n^+ drain.

3.2. Triggering point

The stress current increases as ESD stress time increases and the parasitical BJT turns on. The positions of the total heat peak and lattice temperature peak change compared with

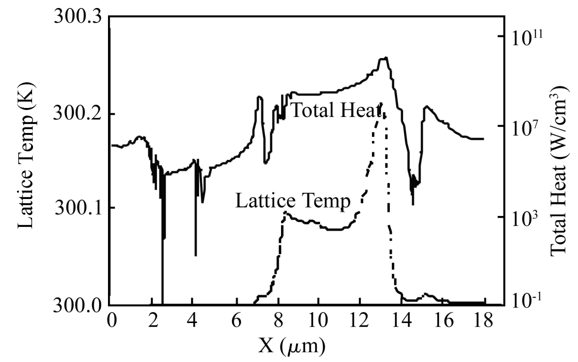

Fig. 5. Total heat and lattice temperature distribution along the Si–SiO_2 interface at the triggering point.

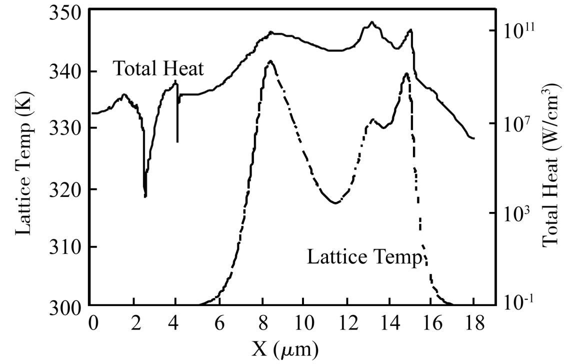

Fig. 6. Total heat and lattice temperature distribution along the Si–SiO_2 interface at the snapback regime.

Fig. 4. At this moment, the impact ionization rate is more than 1 and the current accumulates near the depletion region and the end of the poly field-plate. So the peaks appear at the end of the poly field-plate, as shown in Fig. 5.

3.3. Snapback regime

From Fig. 6, one can see there are three total heat peaks at the n^+ drain, the end of the poly field-plate and the bird's beak, respectively. There are two lattice temperature peaks at the n^+ drain and the bird's beak, respectively. During the snapback regime, the parasitical BJT drastically turns on and the impact ionization at the bird's beak increases greatly for the conductivity modulation. So there are both lattice temperature and total heat peaks at the bird's beak.

3.4. Second breakdown point

With the increase of the stress current, the LDMOS is under high current injection. The concentrations of electron and hole are nearly uniform. A filament zone will form at the n^+ drain when the second breakdown happens. The resistance of the filament zone will decrease greatly as the electron and hole current increase and there will be more current through this region, which will result in a higher Joule heat. If the heat is higher than the critical value, thermal breakdown will happen. So we can see from Fig. 7 that the total heat peak and lattice temperature peak are near the n^+ drain (i.e., the filament zone). From Fig. 7, we also can see that the peak total heat decreases and the peak lattice temperature increases compared with the snapback regime. This is because the lattice absorbs some of

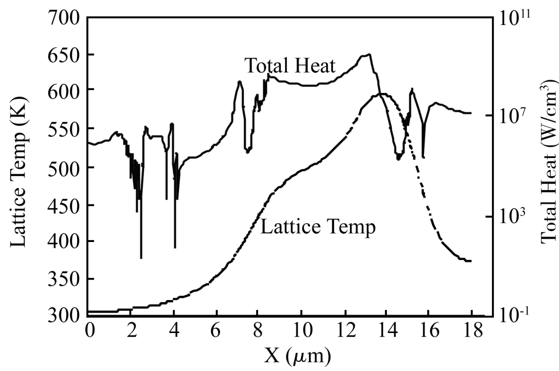

Fig. 7. Total heat and lattice temperature distribution along the Si–SiO_2 interface at the second breakdown point.

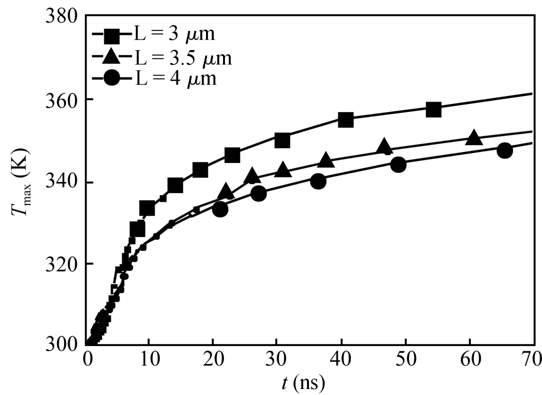

Fig. 8. Peak lattice temperatures with three different gate lengths during HBM ESD transient (GDCS = 1 μm, GSCS = 0.5 μm).

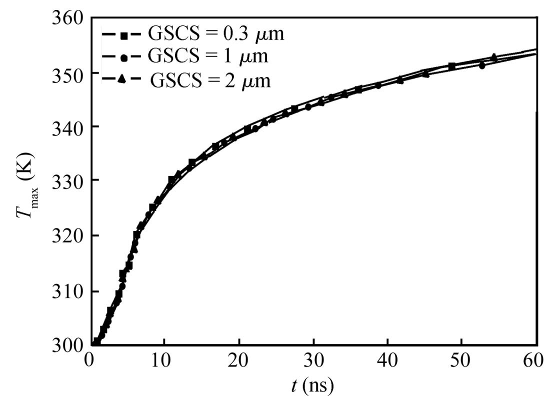

Fig. 9. Peak lattice temperatures with three different GSCS during HBM ESD transient (L = 4 μm, GDCS = 1 μm).

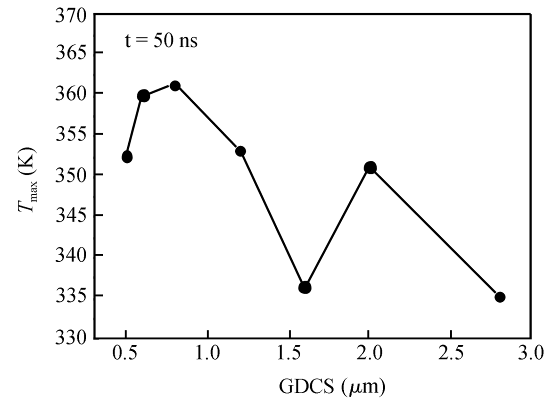

Fig. 10. Peak lattice temperatures with different GDCS at ESD stress time t = 50 ns (L = 4 μm, GSCS = 0.5 μm).

the total heat.

4. Influence of structure parameters on the peak lattice temperature

In the following simulation, the device width is 10 μm, the ESD stress current I_{ESD} is 10 mA and the rise time of the ESD stress current pulse is 6 ns. With the increase of the gate length, the effective heat diffusion distance improves, so the lattice temperature distribution becomes more uniform. In this way, the peak lattice temperature decreases as the gate length increases, as shown in Fig. 8. From Fig. 9, one can see that the GSCS distance hardly affects the peak lattice temperature. Under these conditions, the peak electrical field is near the drain, so as to form the lattice temperature peak near the drain, but the change in GSCS hardly affects the drain region. Figure 10 shows peak lattice temperatures with different GDCS. We can see that the change is irregular. So increasing the GDCS will not always improve ESD performance. From the above discussion, in order to improve the ESD performance of high voltage LDMOS, we can improve the gate length properly and the GDCS could be about 1.5 μm.

5. Conclusion

In order to investigate the thermal characteristics of high voltage gg-LDMOS under ESD stress conditions, the four work states (i.e., the first breakdown region, the triggering point, the snapback regime and the second breakdown point) have been divided in terms of different stress conditions. In the four states, there are different total heat and lattice temperature distributions along the Si–SiO_2 interface, which is important to understand the ESD characteristics of LDMOS. Finally, the influence of structure parameters on peak lattice temperature is also discussed, which is useful for designers to optimize the parameters of LDMSO for better ESD performance.

References

[1] Murari B, Bertotti F, Vignola G A. Smart power IC's. Berlin: Springer, 1996

[2] Sun Weifeng, Shi Longxing, Sun Zhilin, et al. High voltage power integrated circuit technology with N-VDMOS, RESURF P-LDMOS and novel level shift circuit for PDP scan driver IC. IEEE Trans Electron Devices, 2006, 4: 891

[3] Vinson J, Liou J J. Electrostatic discharge in semiconductor devices: an overview. IEEE Proc 1998, 86: 399

[4] Duvvury C, Amerasekera A. ESD: a pervasive reliability concern for IC technologies. IEEE Proc, 1993, 81: 690

[5] Mergens M, Wilkening W, Mettler S, et al. Analysis and compact modeling of lateral DMOS power devices under ESD stress conditions. Electrical Overstress/Electrostatic Discharge Symposium Proceedings, Orlando, FL, USA, 1999: 1

[6] Boselli G, Meeuwse S, Mouthaan T, et al. Investigations on double-diffused MOS transistors under ESD zap conditions. Microelectronics Reliability, 2001, 41: 395

[7] Walker A J, Ward S T, Puchner H. Novel robust high voltage ESD clamps for LDMOS protection. IEEE 45th Annual International Reliability Physics Symposium, Phoenix, 2007: 596