Lithography-independent and large scale fabrication of a metal electrode nanogap*

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Abstract: A lithography-independent and wafer scale method to fabricate a metal nanogap structure is demonstrated. Polysilicon was first dry etched using photoresist (PR) as the etch mask patterned by photolithography. Then, by depositing conformal SiO_2 on the polysilicon pattern, etching back SiO_2 anisotropically in the perpendicular direction and removing the polysilicon with KOH, a sacrificial SiO_2 spacer was obtained. Finally, after metal evaporation and lifting-off of the SiO_2 spacer, an 82 nm metal-gap structure was achieved. The size of the nanogap is not determined by the photolithography, but by the thickness of the SiO_2. The method reported in this paper is compatible with modern semiconductor technology and can be used in mass production.

Key words: lithography-independent; nanogap; conformal deposition; anisotropic etching
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1. Introduction

Nanoelectronic devices in which nanoscale material, such as nanowires, nanotubes, DNA chains, and graphemes serve as functional elements, have received great attention since the end of the last century owing to their potential in overcoming the physical limitations of Si-based microelectronics. Much research has been done to synthesize nanomaterials and understand their electrical characteristics. For this purpose it is necessary to define the nanomaterials between two metal electrodes. However, because of the nanometer scale of these materials, the space between metal electrodes must be very small, at least to several tens of nm. A great deal of effort has been devoted to realizing such a structure (the nanogap), including electron-beam lithography (EBL), focused ion beam (FIB), shallow evaporation, electromigration, electrochemical deposition, mechanical break junction, and so on. Unfortunately, all the reported methods have some drawbacks arising from lack of reliability, repeatability or controllability. For instance, EBL and FIB can exactly produce the metal nanogap down to several nanometers and control its position, but these two methods are time-consuming and unsuitable for large scale fabrication[1, 2]. The shallow evaporation method with nanomaterial serving as the mask is capable of large scale synthesis of a metal nanogap, but the position of the nanomaterial cannot be precisely controlled, thus the nanogap distribution is random, which leads to low yield and repeatability[3]. Gupta reported the fabrication of a metal nanogap using shallow evaporation without nanomaterial mask[4], but this method also suffers from poor controllability and reliability due to the existence of metal at the bottom of the trench. Electromigration can realize a nanogap only on small substrates, where the gap size and position cannot be controlled[5, 6]. Other methods, including electrochemical deposition and mechanical break junction, have similar problems[7, 8].

In this paper, we demonstrate a method to realize a metal nanogap on a 4-inch silicon wafer, which is based on modern mature semiconductor technology. Although the nanogap position is determined by photolithography, the nanogap width is defined by the thickness of the sacrificial SiO_2 spacer, not by the resolution of the photolithography.

In order to obtain the best process result, etch rates of different materials (silicon nitride, SiO_2, polysilicon) with different etch facilities (Si-ICP, SiO_2-ICP, KOH, BHF), polysilicon thickness, polysilicon step profile and SiO_2 deposition conditions are also investigated in this paper. Our method is promising for the fabrication of a nanogap with high reliability, repeatability and controllability and will greatly improve the speed and efficiency of electrical characterization of nanomaterials.

2. Experiment

Silicon nitride (SiN_xH_y) and silicon oxide (SiO_2) films were deposited by STS corp. Mulitiplex plasma-enhanced chemical vapor deposition (PECVD), configured with dual frequency of 13.56 MHz (HF) and 380 kHz (LF). Polysilicon was deposited by LP4612-2F low pressure chemical vapor deposition (LPCVD) and etched in an Alcatel corp. 601E inductively coupled plasma etcher (ICP). STS AOE (advanced oxide etcher) ICP equipment was used to remove the SiO_2 films. Hitachi S-4800 scanning electron microscopy (SEM) was used to characterize the morphology of the structures. The process

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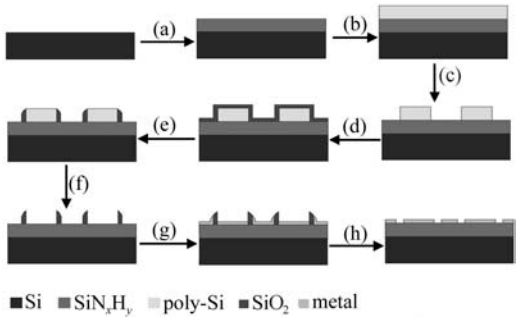

Fig. 1. Schematic diagram of nanoscale metal-gap fabrication.

scheme is shown in Fig. 1.

(a) A SiN_xH_y dielectric layer is deposited by PECVD on a 4-inch silicon (100) wafer.

(b) A polysilicon film is then deposited as the sacrificial layer by LPCVD.

(c) A PR pattern is provided as etch mask by photolithography. Then the pattern is transferred to the polysilicon by ICP etching with SF_6 and C_4F_8.

(d) A SiO_2 film is deposited as sidewall material by PECVD at low temperature (300 °C) on the polysilicon pattern with good step coverage.

(e) The SiO_2 film is vertically etched without etch mask using C_4F_8 ICP etching until the polysilicon and SiN_xH_y layer is exposed. The sidewall SiO_2 is reserved.

(f) The polysilicon sacrificial layer is removed using 30% KOH solution at 85 °C, leaving the nanoscale SiO_2 spacer.

(g) A thin metal (Au in this paper) film is evaporated by electron beam (EB) evaporation.

(h) The SiO_2 spacer is etched by BHF (HF : NH_4F : DI water = 1 : 2 : 3); simultaneously the metal on the SiO_2 is removed. The desired nanoscale metal-gap structure is obtained.

There are several key steps in this process. The first is the good conformal step coverage of PECVD SiO_2 on polysilicon, where the thickness of the SiO_2 is nearly uniform at the top, top corner, bottom corner and other areas. The second is the highly anisotropic plasma etching, in which the etch rate of the film in the direction perpendicular to the surface is much quicker than in other directions. The vertical height of SiO_2 on the step sidewall is larger than in other regions. Therefore, if the SiO_2 is etched vertically and the polysilicon is removed selectively, the nanoscale SiO_2 wire can be exposed in this process; the feature size of the SiO_2 sidewall is determined by the thickness of the deposited SiO_2 film, not by the photolithography. The thickness of the SiO_2 can be precisely controlled to less than 20 nm, and consequently a metal-gap of sub-20 nm can be expected.

3. Results and discussion

3.1. Deposition of the silicon nitride layer

There are two reasons for choosing silicon nitride as the substrate dielectric layer. First, wet etch selectivity between SiN_xH_y with SiO_2 and polysilicon is quite high (Table 1). Second, dry etch selectivity between SiN_xH_y and SiO_2 is also acceptable during SiO_2 spacer formation. In our experiment, 150–230 nm SiN_xH_y films were deposited by PECVD at low temperature (300 °C), using 5% SiH_4 (in Ar) 600 sccm/NH_3 20 sccm/N_2 1960 sccm, a gas pressure of 70 Pa, power of 150 W and low frequency of 380 kHz. It should be pointed out that if LPCVD SiN_xH_y is used, the related etch selectivity can be further improved.

Table 1. Etching rate (Å/s).

Material	SiN_xH_y	Poly-Si	HF-SiO_2	LF-SiO_2
Si-ICP	6.67	40	N/A	N/A
SiO_2-ICP	9.83	N/A	66.7	60
BHF	5.75	N/A	110	42
KOH	0.05	150	5.98	3.33

As shown in Table 1, silicon nitride films have excellent etching resistance in different etch facilities. The selectivity of SiN_xH_y to polysilicon was larger than 6 : 1 in plasma etching and 3000 : 1 in 30% KOH solution at 85 °C. Meanwhile, the selectivity of SiN_xH_y to SiO_2 was larger than 6 : 1 in plasma etching and 7 : 1 in BHF (HF : NH_4F : DI water = 1 : 2 : 3) solution at room temperature.

3.2. Deposition and etching of the polysilicon layer

The 200–500 nm polysilicon layer was deposited by LPCVD as a sacrificial layer. The gas flow for SiH_4 (20% in Ar)/B_2H_6 was 130 sccm/35 sccm, with a gas pressure of 46 Pa and temperature of 640 °C. PR was spin-coated on the polysilicon layer and then patterned by photolithography. After that, the pattern was transferred to the polysilicon using PR as the etch mask by ICP etching.

A perpendicular and smooth profile of the polysilicon step is crucial for better step coverage of SiO_2 on the polysilicon. A sloped polysilicon profile can lead to a sloped SiO_2 sidewall and increase the final gap widths. On the other hand, the occurrence of non-ideal etching 'foot' and 'trenching' , as shown in Figs. 2(a) and 2(b), respectively, on the bottom of the step would lead to the failure of the vertical SiO_2 nanowire.

An optimal ICP process was used under conditions of 50 sccm SF_6, 85 sccm C_4F_8, 1200 W top electrode power, 65 W bottom electrode power and 1.8 Pa gas pressure. The cross section scanning electron microscopy (SEM) images are shown in Fig. 2(c). The desired vertical sidewall profile with angle > 85° was obtained without 'foot' and 'trenching'.

3.3. Deposition and etching of the SiO_2 sidewalls

Compared with physical vapor deposition (PVD), chemical vapor deposition (CVD) of SiO_2 is a conformal deposition process. During the various CVD deposition processes, the step coverage quality of borophosphosilicate glass (BPSG) films and SiO_2 films deposited by tetraethoxysilane (TEOS) is better than that of undoped PECVD silane-SiO_2[9, 10]. However, BPSG glass reflow is necessary at high temperature (> 800 °C) in order to obtain good step coverage. Boron and phosphorus diffusion may deteriorate the device performance.

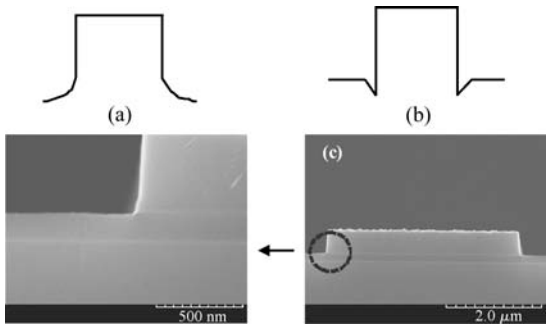

Fig. 2. (a) Etching non-ideally: foot; (b) Etching non-ideally: trenching; (c) Cross section SEM images of the 500 nm polysilicon step after ICP etching.

TEOS is liquid at room temperature, so the liquid line is prone to obstruction. Hence, reasonable deposition processes can only be obtained at higher temperature (> 600 °C). Therefore, the undoped silane-SiO_2 deposited by PECVD is more widely used because of its simplicity, expeditiousness and low temperature (< 400 °C).

Low temperature undoped SiO_2 200–250 nm was deposited by PECVD at 300 °C. The process conditions were varied in order to improve the step coverage, using 150–600 sccm 5% SiH_4 (in Ar)/1400–2000 sccm N_2O, 73–120 Pa gas pressure and the dual frequency of 13.56 MHz and 380 kHz. It was found that the quality of the step coverage is slightly dependent on the deposition conditions and the SiO_2 profile is strongly dependent on the profile of the substrate.

ICP etching was applied to remove the surface oxide films until the polysilicon and silicon nitride layers were exposed. The STS ICP etcher was configured with a 3000 W coil generator and a 600 W RF generator both at 13.56 MHz. In our experiment, the top electrode power is 1200 W and bottom electrode power is 220 W. The flow rate of $C_4F_8/H_2/He$ chemical gases is 15 sccm/12 sccm/174 sccm at a pressure of 0.5 Pa. The process gases C_4F_8 and H_2 were used to obtain good etch selectivity of SiO_2 to SiN_xH_y, because a fluorocarbon gas containing a high carbon to fluorine (C/F) ratio and a modest amount of H_2 are useful in improving SiO_2 to SiN_xH_y etch selectivity[11, 12].

The SiO_2 film on top of the polysilicon step should be removed completely, so precise control of the SiO_2 etch time was important. If the etch time is long, the width and height of SiO_2 spacer will be relatively small, and the SiO_2 spacer may also be removed during the polysilicon etch.

500 nm and 200 nm polysilicon steps were fabricated to investigate the difference of the step coverage and plasma etching back. As shown in Figs. 3(a) and 3(b), after the same 200 nm SiO_2 films were deposited, the width of the SiO_2 sidewalls of 500 nm and 200 nm steps are 110 nm and 120 nm, respectively. The step coverage is 55%–60%.

The profile SEMs of the SiO_2 spacer are shown in Figs. 3(c) and 3(d) after ICP etching back. It was found that the widths of the residual SiO_2 sidewalls of the 500 nm step were ~96 nm and of the 200 nm step were ~106 nm. Owing to the same SiO_2 etch time, the etched widths of the SiO_2 sidewalls

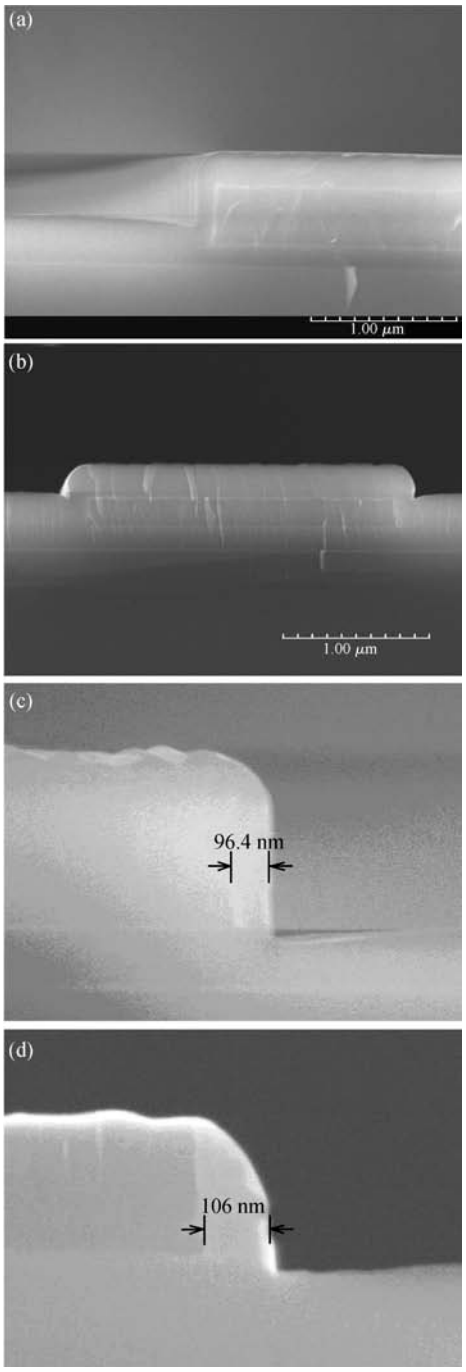

Fig. 3. Cross section SEM images: (a) 200 nm SiO_2 on the 500 nm polysilicon step; (b) 200 nm SiO_2 on the 200 nm polysilicon step; (c) SiO_2 sidewalls of the 500 nm polysilicon step after ICP etching back; (d) SiO_2 sidewalls of the 200 nm polysilicon step after ICP etching back.

for the two steps are both approximately 14 nm.

3.4. Formation of the SiO_2 nanowire and metal-gap

The polysilicon sacrificial layer was removed in KOH solution at 85 °C, after the SiO_2 film on top was dry etched. The KOH etch rates of the SiO_2 films were dependent on the deposition process conditions. It was found that a 380 kHz LF generator and higher power can clearly improve the etching resistance of SiO_2 films in KOH solution and avoid damaging the SiO_2 spacer. As shown in Table 1, the etching rate of the

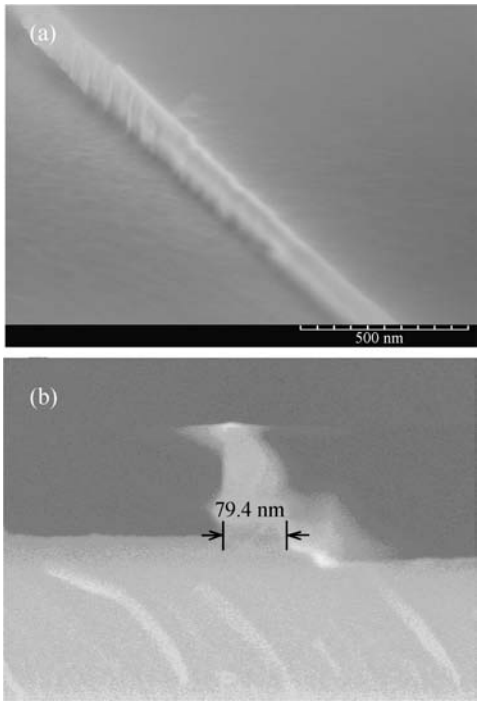

Fig. 4. (a) Top view SEM images and (b) cross section SEM images of the SiO_2 nanowire fabricated by the 200 nm polysilicon step.

LF 700 W SiO_2 film was 3.3 Å/s compared with the HF 30 W SiO_2 film value of 6 Å/s. Thus the selectivity of SiO_2 to polysilicon can be improved from 25 : 1 to 45 : 1.

Figures 3(c) and 3(d) show that the widths of the SiO_2 sidewalls of the 500 nm and 200 nm polysilicon steps were slightly different. The SiO_2 nanowires fabricated in two steps were investigated after the polysilicon films were removed completely. Because the etching time in KOH solution for the 500 nm polysilicon sample was longer than that of the 200 nm sample, part of SiO_2 sidewall of the 500 nm sample was damaged. For the 200 nm polysilicon sample, the desired SiO_2 nanowire was obtained with a width of 79 nm and a height of 110 nm, as shown in Fig. 4.

A thin Au film was evaporated on the top of the SiO_2 nanowire by E-beam evaporation. BHF ($HF : NH_4F$: DI water = 1 : 2 : 3) solution was used to remove the SiO_2 nanowire while the metal on top was simultaneously removed. As a result, an 82 nm metal-gap structure was successfully obtained (see Fig. 5). Splits were found on the surface of the Au film, which could be due to the Au film being too thin and process rate too rapid.

4. Conclusion

A simple, fast, cost-effective and lithography-independent method has been developed to fabricate a sub-100 nm metal-gap structure on a 4-inch wafer. After a 200 nm polysilicon layer was patterned by photolithography, a 200 nm SiO_2 film was deposited conformally on the polysilicon step and then etched back anisotropically by ICP. A 79 nm SiO_2 nanowire was obtained after removing the polysilicon sacrificial film. After the metal deposition and removal of SiO_2 with BHF, an 82 nm metal-gap structure was obtained.

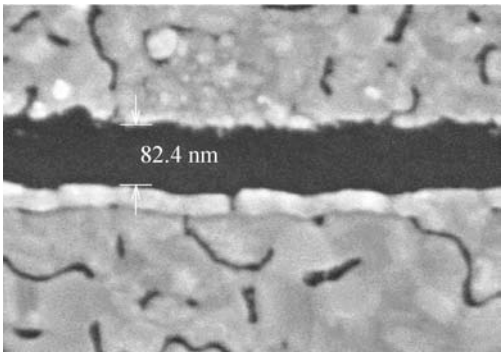

Fig. 5. Top view SEM images of the 82 nm metal-gap.

The influence of different conditions, such as etch rates of different materials (silicon nitride, SiO_2, polysilicon) with different etch facilities (Si-ICP, SiO_2-ICP, KOH, BHF), polysilicon thickness, SiO_2 deposition conditions was also investigated. Our method is promising for achieving a sub-20 nm nanogap and can be applied to the electrical characterization of nanomaterials and device fabrication.

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