Design and noise analysis of a fully-differential charge pump for phase-locked loops*

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Abstract: A fully-differential charge pump (FDCP) with perfect current matching and low output current noise is realized for phase-locked loops (PLLs). An easily stable common-mode feedback (CMFB) circuit which can handle high input voltage swing is proposed. Current mismatch and current noise contribution from the CMFB circuit is minimized. In order to optimize PLL phase noise, the output current noise of the FDCP is analyzed in detail and calculated with the sampling principle. The calculation result agrees well with the simulation. Based on the noise analysis, many methods to lower output current noise of the FDCP are discussed. The fully-differential charge pump is integrated into a 1–2 GHz frequency synthesizer and fabricated in an SMIC CMOS 0.18 μm process. The measured output reference spur is –64 dBc to –69 dBc. The in-band and out-band phase noise is –95 dBc/Hz at 3 kHz frequency offset and –123 dBc/Hz at 1 MHz frequency offset respectively.

Key words: fully-differential charge pump; mismatch; noise; common-mode feedback; phase-locked loop
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1. Introduction

Charge-pump (CP) based phase-lock loops (PLLs) are commonly used in modern communication systems. They have a wide frequency capture range and zero static phase error. In practice, PLL performance deteriorates due to non-ideal CP effects. Mismatch between charging and discharging currents introduces a steady state phase error as well as reference spurs[1−3]. Spurs may cause other channels to interfere with the desired channel in a wide-band system. Also, CP current noise contributes to PLL phase noise which directly affects transceiver performance. Thus, current mismatch and current noise are two major considerations in CP design.

Current mismatch comes from device mismatch, channel-length modulation, and parasitic capacitors. Many techniques have been employed to deal with these non-ideal effects. A replica technique in Ref. [4] can suppress channel-length modulation. Compensation techniques are employed to deal with clock feed-through and charge injection in Refs. [5, 6]. Little attention has been paid to CP current noise in previous papers. However, CP noise is an important contribution to PLL phase noise, which is a significant design specification in PLL design. Thus, it should be analyzed and simulated carefully. Furthermore, a fully-differential structure is immune to environmental noise and the power supply ripple so that a fully-differential CP is preferred in a PLL. However, a fully-differential change pump (FDCP) needs a stable common-mode feedback (CMFB) circuit which should contribute as little current noise and current mismatch as possible. In this paper, a perfect current matching FDCP with a proposed CMFB circuit is presented. The PLL architecture and FDCP circuit are described. A noise analysis for the charge pump is presented.

2. PLL architecture and FDCP circuit

Figure 1 shows the fourth-order PLL architecture and the

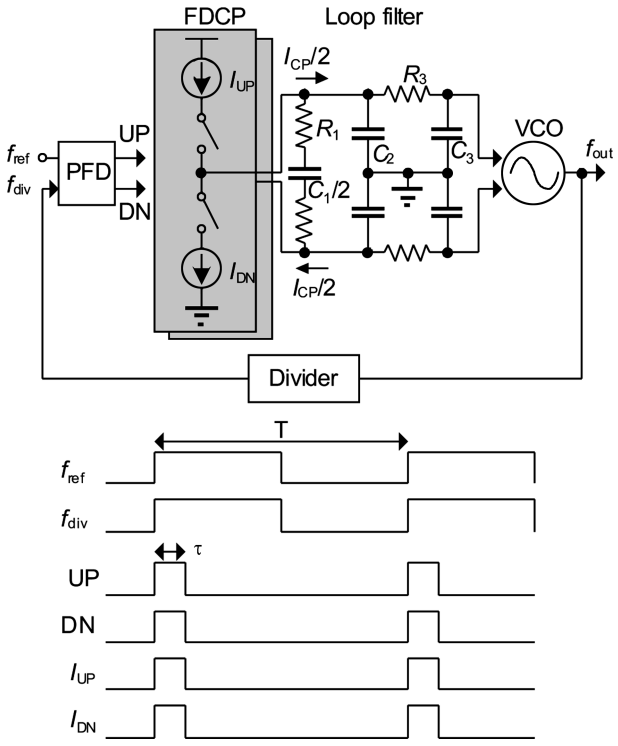

Fig. 1. Fourth-order PLL and timing diagram when locked.

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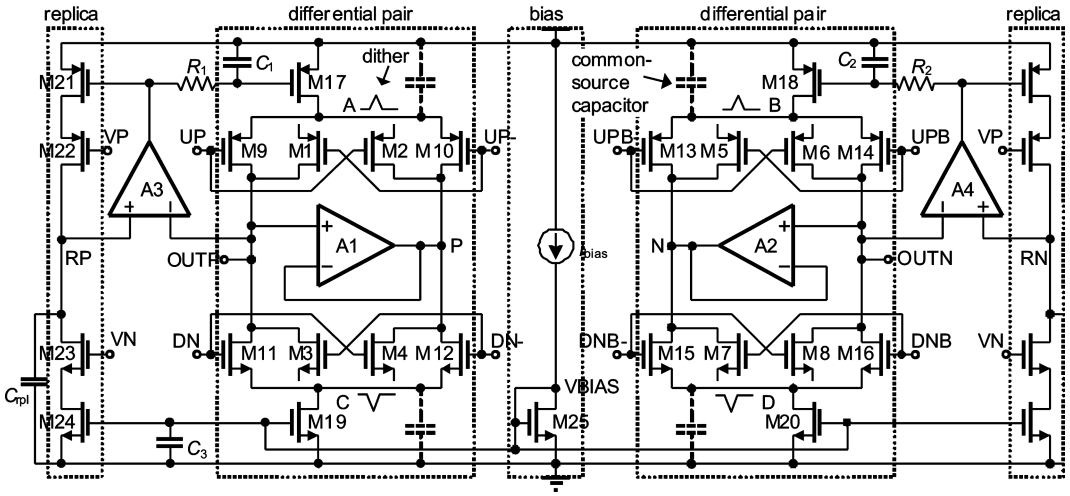

Fig. 2. Differential CP circuit.

timing diagram when the PLL is locked. The PLL employs a third-order passive filter which is configured differentially. I_{UP}, I_{DN} are the charging and discharging currents of the FDCP respectively. τ is the phase-frequency detector (PFD) reset delay which is designed to avoid the dead zone[7]. T is the period of the reference clock. The simplified open-loop transfer function of the fourth-order PLL is

$$H_0(s) = \frac{I_{\mathrm{CP}} K_{\mathrm{VCO}}}{2\pi N (C_1 + C_2 + C_3)} \frac{1 + s/\omega_{\mathrm{z}}}{s^2 \left(1 + s\big/\omega_{\mathrm{p2}}\right)\left(1 + s\big/\omega_{\mathrm{p3}}\right)}, \tag{1}$$

where

$$\omega_{\mathrm{z}} = \frac{1}{R_1 C_1}, \quad \omega_{\mathrm{p2}} \approx \frac{1}{R_1 (C_2 + C_3)}, \quad \omega_{\mathrm{p3}} \approx \frac{1}{R_3 C_2 C_3 / (C_2 + C_3)}. \tag{2}$$

The FDCP comprises a differential CP circuit, a control signal generating circuit, and a CMFB circuit. The differential CP circuit in Fig. 2 consists of two differential pairs, two replicas and a current bias. Since charging and discharging currents are switched in the differential pairs and do not need to be turned off, the working speed can be very high. Operational amplifiers A1 and A2 ensure equal voltages in nodes OUTP and P, OUTN and N respectively. Thus, voltages at common-source nodes A, B, C and D will remain unchanged before and after current switching. Two replicas and amplifiers A3 and A4 are used to compensate channel-length modulation, which makes the charging current perfectly match the discharging current[4]. The simulated DC current mismatch is shown in Fig. 3. The DC mismatch current is less than 50 nA from 0.216 to 1.512 V when charging and discharging currents are 50 μA. Resistors R_1 and R_2 as well as capacitors C_1 and C_2 are added to filter out the high frequency noise of amplifiers A3 and A4.

If the switching transistors M9–M16 work in the deep triode region when turned on, half the charge in the MOS capacitance injects to output nodes, which can cause large current glitches and results in serious mismatch. If they work in the saturation region when turned on, only the charge in the gate-drain overlap capacitance injects to output nodes. Thus, transistors M9–M16 are in the saturation region when turned

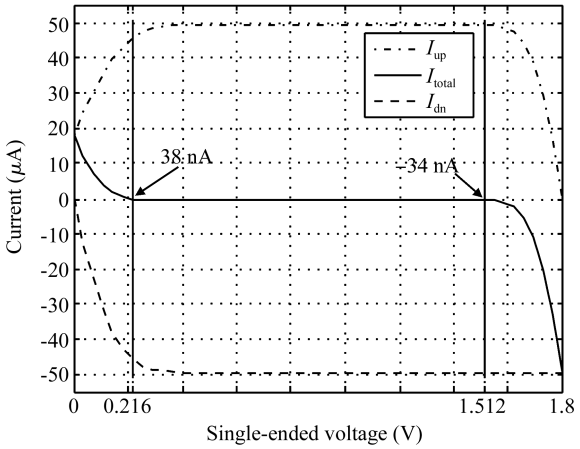

Fig. 3. Simulated DC current mismatch.

on. Transistors M1–M8 are added to compensate the gate–drain overlap capacitance of transistors M9–M16[5]. Their sources are floating, avoiding the extra DC current. When currents are being switched, voltages at common-source nodes A, B, C and D dither, which will cause a low speed glitch in charging and discharging currents. If a large common-source capacitor is added between A, B, C or D and ground or power, the low speed glitch can be suppressed[5]. However, common-source capacitors are not necessary in a fully-differential structure. Low speed glitches of charging and discharging currents cancel each other if the time τ is longer than the low speed glitch lasting time. Thus, low speed glitches cannot affect the PLL settling or introduce spurs. The differential output current with or without common-source capacitors is shown in Fig. 4. Low speed glitches in common-source nodes cannot affect the differential output current. Current glitches are caused by the gate-drain overlap capacitance of transistors M1–M16 when charging or discharging current is switching. Furthermore, common-source capacitors may increase the noise contribution from transistors M9–M16.

The control signal of transistors M9–M16 should be carefully designed to ensure working in the saturation region when turned on. The control signal generating circuit in Fig. 5 consists of two buffers, two switching arrays, and two capacitors.

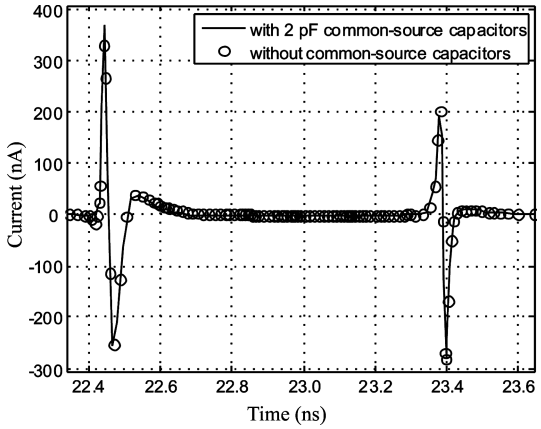

Fig. 4. Differential output current with or without common-source capacitors.

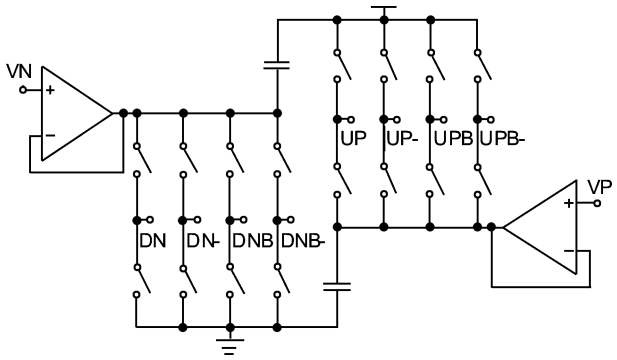

Fig. 5. Control signal generating circuit.

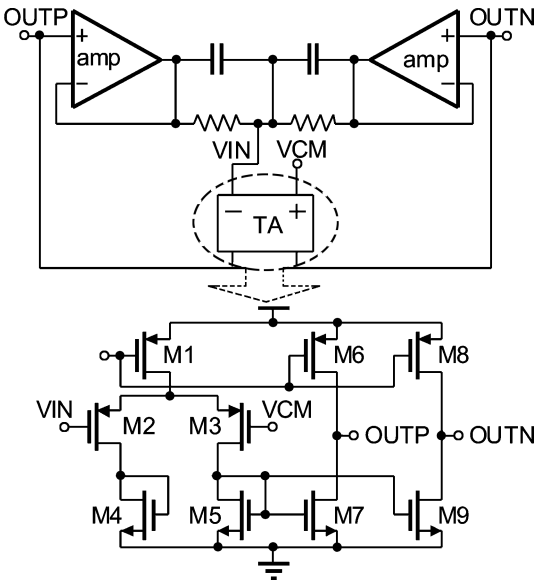

Fig. 6. CMFB circuit.

The buffers are simple one-stage amplifiers consuming 50 μA each. The switches are made of complementary MOS transistors which can suppress clock feed-through and charge injection so that control signals can change smoothly. Complementary switches can also ensure equal rising and falling times. The switching arrays are controlled by the PFD.

The easily stable CMFB circuit shown in Fig. 6 is proposed. It has characteristics of low noise and introducing ultra-small DC current mismatch. It employs two rail-to-rail amplifiers whose bandwidths are much larger than that of CMFB

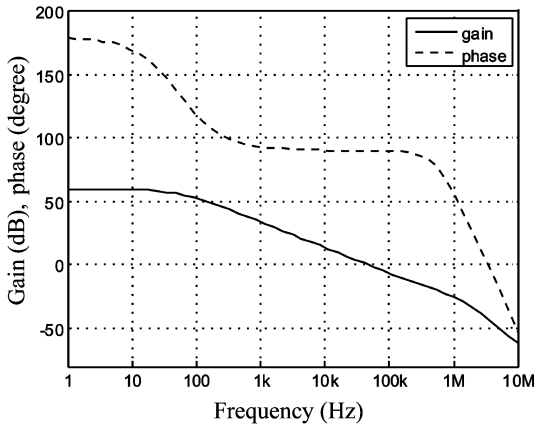

Fig. 7. Simulated CMFB loop bode diagram.

loop, two resistors and two capacitors to detect the common-mode voltage. Thus, the CMFB circuit will not affect the loop filter and can handle input voltage swing from ground to power[6]. The operation principle of the CMFB circuit is that the output common-mode voltage is detected and compared with a reference voltage VCM. The voltage difference is converted into an error current by a transconductance amplifier (TA). The error current is fed back into output nodes OUTP and OUTN to adjust the common-mode voltage. The TA uses only 1 μA static current in each output branch. Furthermore, output-stage transistors have a large length, so the DC current mismatch introduced by the CMFB circuit can be minimized. The dominant pole of the CMFB loop at nodes OUTP and OUTN is determined by the loop filter. Thus, the frequency characteristic of the CMFB circuit is like that of a single-stage amplifier. A simulated bode diagram of the CMFB circuit is shown in Fig. 7. The loop bandwidth is about 70 kHz, the phase margin is about 90 °.

The FDCP is divided into twenty-five sub-FDCPs. Each sub-FDCP is composed of two 2 μA differential pairs and two 2 μA replicas. Thus, device matching between differential pairs and replicas can be improved. Another advantage of this arrangement is that it is easy to adjust the CP current.

3. Noise analysis

A charge pump is a linear time-varying system. The output current noise of the FDCP comes from the differential CP circuit and the CMFB circuit. The output current noise of the differential CP circuit can be deduced with the sampling principle.

Firstly, the continuous output current noise must be calculated. The noise from current bias is common-mode noise which can be neglected. The differential noise power equals twice the noise power of a single-ended circuit. For simplicity, only the left-hand side of the differential CP circuit is considered. The replica can be modeled as an amplifier. In the differential pairs, the NMOS transistors work the same as PMOS transistors. Thus, for brevity of analysis, only PMOS transistors are considered. The noise contribution from switching transistors M9–M16 is ultra-small and can be neglected

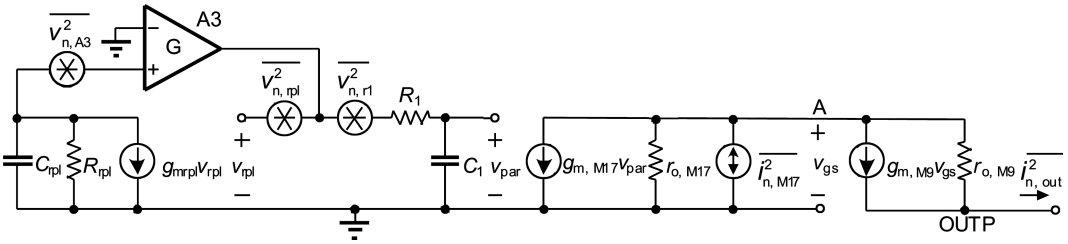

Fig. 8. Small-signal noise equivalent circuit for noise analysis.

because M9–M16 are cascode transistors. The small-signal circuit for noise analysis is shown in Fig. 8. R_{rpl}, g_{mrpl}, $\overline{v^2_{n,rpl}}$ are the equivalent resistance, transconductance and noise of the replica circuit, respectively. G and $\overline{v^2_{n,A3}}$ are the gain and input equivalent noise of amplifier A3. $\overline{v^2_{n,r1}}$, $\overline{i^2_{n,M17}}$ are the noise of resister R_1 and transistor M17.

The continuous output current noise can be obtained from Fig. 8 and simplified as

$$\overline{i^2_{nc,out}} \approx \left[\left(\overline{v^2_{n,rpl}} + \frac{\overline{v^2_{n,A3}}}{\left|g_{mrpl}\left[R_{rpl}\|\left(1/sC_{rpl}\right)\right]\right|^2} + \overline{v^2_{n,r1}}\right)\times \left|\frac{1/sC_1}{R_1+1/sC_1}\right|^2 g^2_{m,m17} + \overline{i^2_{n,M17}}\right]\left|\frac{g_{m,M9}}{g_{m,M9}+g_{ds,M9}+g_{ds,M17}}\right|^2. \quad (3)$$

After the PLL is locked, $\overline{i^2_{nc,out}}$ is sampled out every T seconds. Each sample lasts for a period of τ. The spectrum of the sampling function is

$$S\left(f=\frac{n}{T}\right)=\frac{\sin(\pi\tau n/T)}{\pi n}, \quad n=0,\pm1,\pm2,\ \ldots \quad (4)$$

So,

$$S(0)=\frac{\tau}{T}, \quad S\left(\frac{\pm1}{T}\right)=\frac{\sin(\pi\tau/T)}{\pi},\ \ldots \quad (5)$$

Sampled output current noise can be calculated through convolution between $\overline{i^2_{nc,out}}$ and $S(f)$. In the convolution, the number of sampling function harmonics which should be considered is related to the bandwidth of the noise. The bandwidth of the noise contribution from the replica, resister R_1 and flicker noise of transistor M17 is much smaller than $1/T$, so only the DC component of the sampling function needs to be considered. The bandwidth of the noise contribution from the thermal noise of transistor M17 is almost unlimited, so all sampling function harmonics need to be considered. Thus, the sampled output current noise can be obtained as

$$\overline{i^2_{n,out}} = S(0)^2\left(\overline{i^2_{n,rpl}}+\overline{i^2_{n,r1}}+\overline{i_{1/f,M17^2}}\right)+e^2\overline{i^2_{th,M17}}, \quad (6)$$

where

$$e^2=\sum_{n=-\infty}^{\infty} S\left(f=\frac{n}{T}\right)^2, \quad (7)$$

$\overline{i^2_{n,rpl}}$ and $\overline{i^2_{n,r1}}$ are the noise contribution to the continuous output current noise from the replica and resister R_1 respectively. $\overline{i^2_{1/f,M17}}$ is the noise contribution to the continuous output current noise from the flicker noise of transistor M17. $\overline{i^2_{th,M17}}$ is the noise contribution to the continuous output current noise from the thermal noise of transistor M17.

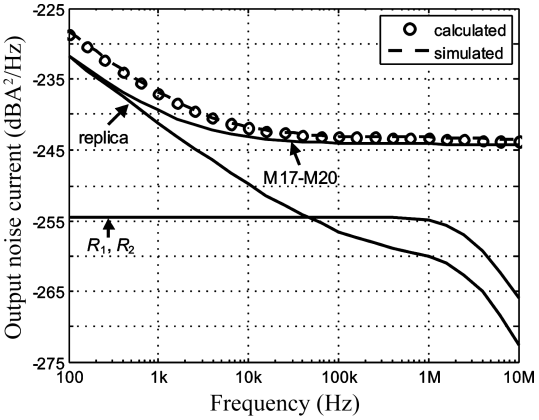

Fig. 9. Calculated and simulated output current noise of the differential CP circuit.

Figure 9 shows the calculated and simulated output current noise of the differential CP circuit and noise contribution from different circuit components. The calculation result agrees well with the simulation. In frequencies below 1 kHz the dominant noise contribution comes from both the replica and transistors M17–M20. In frequencies above 1 kHz the dominant noise contribution only comes from transistors M17–M20. The noise contribution from the replica decreases rapidly between 100 Hz and 100 kHz because the bandwidth of the replica loop with a dominant pole at node RP (or RN) is less than 1 kHz. The non-dominant pole about at 2 MHz comes from R_1 and C_1 (or R_2 and C_2).

The current noise from the CMFB circuit is not sampled. Only transistors M6–M9 in Fig. 6 contribute noise. The noise from other parts is common-mode noise. Thus, the output current noise of the CMFB circuit is

$$\overline{i^2_{n,CMFB}} = 2\left(\overline{i^2_{n,M6}}+\overline{i^2_{n,M7}}\right), \quad (8)$$

where $\overline{i^2_{n,M6}}$ and $\overline{i^2_{n,M7}}$ are current noise of transistors M6 and M7 respectively.

Figure 10 shows the simulated output current noise of the differential CP circuit with and without common-source capacitors. It can be seen that the noise contribution from the CMFB circuit can be neglected. The simulation reveals that large common-source capacitors deteriorate noise performance greatly, especially at low frequencies. The reason for this is that switching transistors M9–M16 become the main noise contribution due to the complicated time-varying characteristics of the differential CP circuit.

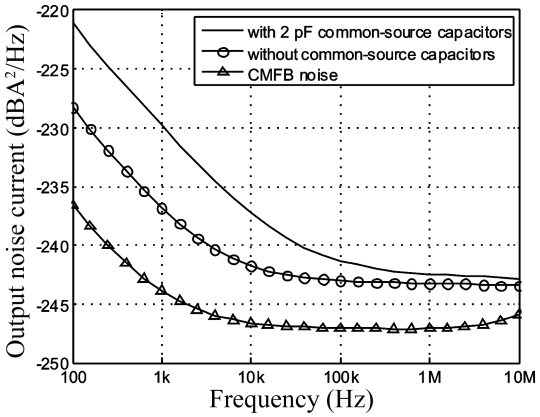

Fig. 10. Simulated output current noise of the differential CP circuit with and without common-source capacitors.

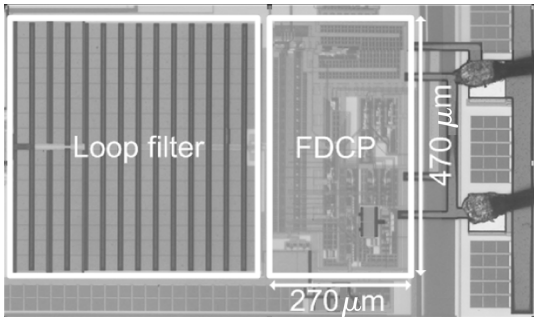

Fig. 11. Die photograph.

Based on the previous analysis, methods for improving the noise performance can be discussed. Firstly, the noise contribution from the CMFB circuit should be minimized. The size of transistors M6–M9 in Fig. 6 should be larger to decrease flicker noise. Each output branch uses only 1 μA current to decrease thermal noise. Thus, the output current noise of the CMFB circuit is much smaller than that of the differential CP circuit. Secondly, to lower the noise contribution from replicas, the bandwidth of the replica loop is decreased by increasing the size of capacitors $C_{\rm rpl}$ and $C_{\rm rpr}$. In addition, the replica current is increased to reduce its noise contribution. Thirdly, to lower the flicker noise of transistors M17–M20, their device sizes are increased. Fourthly, though noise contribution from amplifiers A3 and A4 can be neglected at low frequency, high frequency noise should be filtered out by resistor R_1 and capacitor C_1 (or R_2 and C_2). Resistors R_1 and R_2 themselves also generate noise at low frequencies, so they cannot be too large.

4. Experimental results

The fully-differential charge pump is used in a 1–2 GHz frequency synthesizer, which was fabricated in a SMIC 0.18 μm CMOS 1P6M mixed-signal process. The power supply is 1.8 V. The FDCP consumes 1.6 mW. A die photograph is shown in Fig. 11. The die area of the FDCP is about 270 × 470 μm^2. Figure 12 shows the measured PLL spectrum. The measured output reference spur is –64 to –69 dBc.

Figure 13 shows the measured PLL phase noise. It shows the measured and calculated phase noise and noise contributions from different components in the frequency synthesizer. The calculated phase noise agrees well with the measured result. Components which are the dominant contributors of phase noise in the low frequency range are the reference, the FDCP, and the VCO successively. The FDCP has a low phase noise contribution. The in-band and out-band phase noise is –95 dBc/Hz at 3 kHz offset and –123 dBc/Hz at 1 MHz frequency offset respectively. The measured PLL settling diagram is shown in Fig. 14. The PLL settling time is composed of the automatic frequency control (AFC) settling time and the analog settling time. The PLL loop is locked quickly after AFC operation.

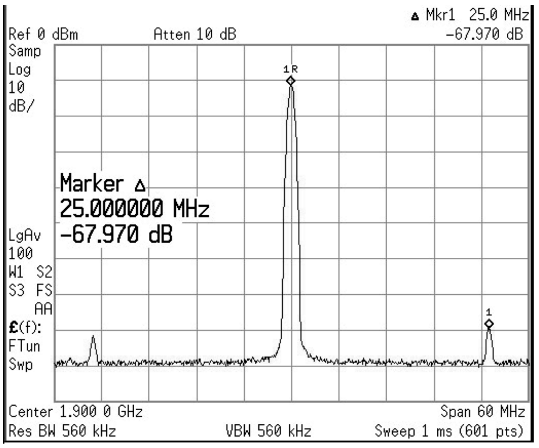

Fig. 12. Measured PLL spectrum.

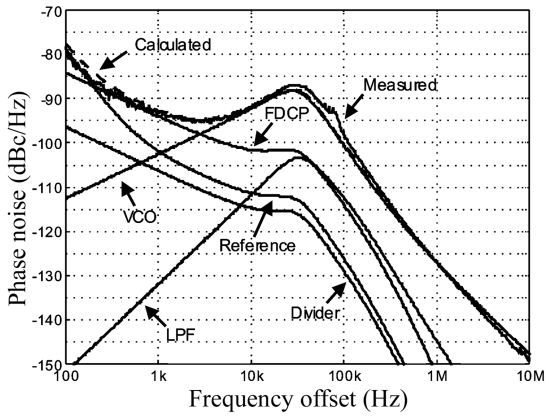

Fig. 13. Measured and calculated PLL phase noise.

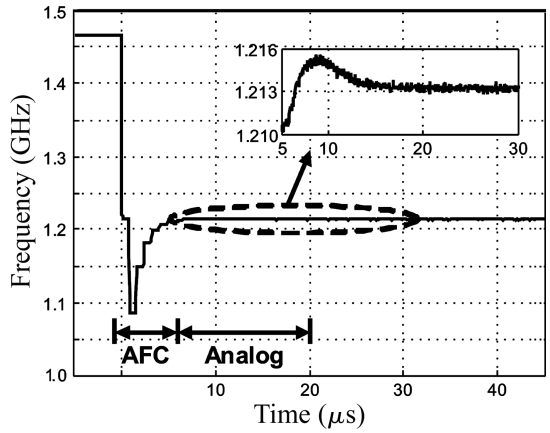

Fig. 14. Measured PLL settling time.

5. Conclusion

A perfect matching low current noise fully-differential charge pump with an easily stable CMFB circuit is presented. Mismatch and noise of the charge pump are two major factors affecting PLL performance. High DC current matching between charging and discharging currents is achieved with a replica circuit. Current glitches are suppressed with compensation transistors. The output current noise of the FDCP is analyzed in detail and the noise performance is optimized. The FDCP is realized in a PLL with SMIC 0.18 μm CMOS technology and reaches reference spur levels of –64 to –69 dBc.

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