Impacts of additive uniaxial strain on hole mobility in bulk Si and strained-Si p-MOSFETs*

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Abstract: Hole mobility changes under uniaxial and combinational stress in different directions are characterized and analyzed by applying additive mechanical uniaxial stress to bulk Si and SiGe-virtual-substrate-induced strained-Si (s-Si) p-MOSFETs (metal-oxide-semiconductor field-effect transistors) along ⟨110⟩ and ⟨100⟩ channel directions. In bulk Si, a mobility enhancement peak is found under uniaxial compressive strain in the low vertical field. The combination of ⟨100⟩ direction uniaxial tensile strain and substrate-induced biaxial tensile strain provides a higher mobility relative to the ⟨110⟩ direction, opposite to the situation in bulk Si. But the combinational strain experiences a gain loss at high field, which means that uniaxial compressive strain may still be a better choice. The mobility enhancement of SiGe-induced strained p-MOSFETs along the ⟨110⟩ direction under additive uniaxial tension is explained by the competition between biaxial and shear stress.

Key words: hole mobility enhancement; additive uniaxial strain; biaxial strain; combinational strain; channel direction

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1. Introduction

With geometric scaling of conventional MOSFETs meeting its physical limitations, strain technology has become a promising candidate, and has been incorporated into production[1]. State-of-the-art strain-Si technology includes biaxial strain caused by epitaxially growing strained-Si on relaxed SiGe virtual substrates[2], and process-induced uniaxial strain[3]. For p-MOSFETs, it is observed that biaxial tensile strain and uniaxial compressive strain can increase hole mobility. The carrier mobility is determined by

$$\mu = \frac{q\tau}{m^*},$$

where $1/\tau$ is the scattering rate, and m^* is the conductivity effective mass. So both scattering and effective mass are responsible for the mobility difference. At the present technology level, hole mobility enhancement under biaxial strain is mainly ascribed to reduced scattering[4,5], while under uniaxial strain, mass change caused by band warping plays the most important role[3,4].

Silicon MOSFETs undergoing uniaxial and biaxial stress have been investigated separately for decades experimentally and theoretically, but the effects of a combination of biaxial and uniaxial stress are rarely discussed and verified by experiments. Recently, Weber *et al.* reported work in this field[6], but they did not study the stress along the ⟨100⟩ direction. Moreover, they employed the piezoresistance theory to explain the mobility variation, which has been proved inadequate for stresses above 250 MPa[5]. Since the present production technology can introduce 900 MPa stress via the embedded SiGe source and drain method[1,3], and 2 GPa stress by the SiN cap technique[7], the piezoresistance rule should be abandoned. So, in this paper, a wafer-bending-based experiment is presented, and a qualitative analysis based on competition between interwing hole transportation and scattering rate change is developed. Longitudinal stress in the ⟨100⟩ channel is also under observation to see if ⟨110⟩ is still a better channel direction under combinational stresses compared to ⟨100⟩, as it appears under uniaxial compressions[8,9]. Further, the field dependences of strain-altered mobility in different stress conditions are compared, giving suggestions to the strain technology.

2. Experiment

The setup of the experiment includes the preparation of samples, and the construction of an additive uniaxial strain-inducing structure.

2.1. Sample preparation

The devices were bulk Si and biaxial s-Si p-MOSFETs. In fabricating the strained Si MOSFETs, 3 μm thick compositionally graded SiGe buffers were first deposited on (001) Si wafers, in which the Ge fraction increases linearly from 0 to 20% as reported in previous work[10], and then a 0.8 μm thick $Si_{0.8}Ge_{0.2}$ and 12 nm strained Si layer was grown. The Raman spectrum showed that the tensile strain in s-Si was 0.8%, which means the stress is 1.4 GPa (for an elastic modulus of 181 GPa for (001) Si[11]). Material growth was performed in

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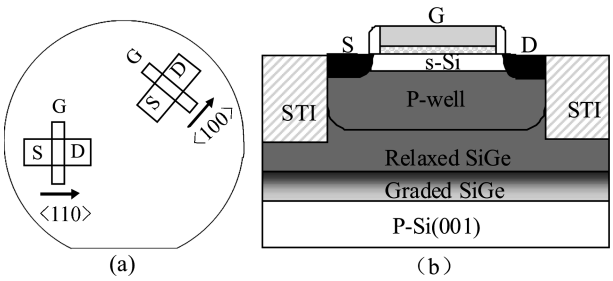

Fig. 1. (a) Schematic view of channel direction on (001) Si; (b) Cross section view of s-Si p-MOSFET.

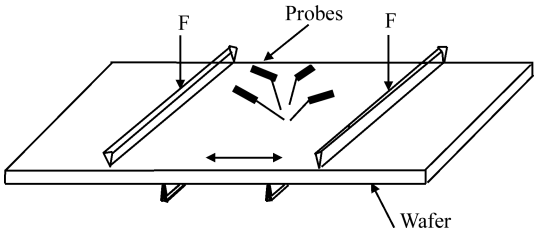

Fig. 2. Illustration of wafer bending setup.

an Applied Materials Epi Centura 200 commercial-grade epitaxy reactor, with SiH_4 and GeH_4 as precursors at a growth pressure of 100 Torr. P-MOSFETs were fabricated along the ⟨110⟩ and ⟨100⟩ direction channels, and the gate oxide thickness was 10 nm. The measured MOSFETs had a size of 20 μm/20μm. The device structure is shown in Fig. 1.

2.2. Strain-inducing structure

Uniaxial strains were introduced by a wafer bending setup (Fig. 2). As the two ridges are pressed onto the wafer, they introduce tensile or compressive uniaxial stress to the surface of the wafer, so that the MOSFETs were under uniaxial strain. Different strain directions were achieved by rotating the wafers.

The strains in the experiment were all applied along the channel, in other words, they were longitudinal strains. Since the wafer was in the elastic deformation region, due to the formula in Ref. [6], the strain (ε, in %) and stress (σ, in Pa) are decided to be approximately –0.16% to 0.16% and –215 to 215 MPa (⟨100⟩ direction) / –278 to 278 MPa (⟨110⟩ direction) respectively. All the electrical properties of MOSFETs were monitored using a Keithly 4200 semiconductor characterization system.

3. Extraction of carrier mobility

The effective vertical electric field ($E_{\rm eff}$) can be calculated by

$$E_{\rm eff} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm s}} \frac{\eta V_{\rm GS} + (1-\eta)V_{\rm T}}{t_{\rm ox}},$$

where gate oxide thickness $t_{\rm ox}$ is 100 Å in the investigated p-MOSFET, fitting parameter η is 1/3 for the hole[12], $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm s}$ are the dielectric constants of the oxide and the semiconductor, respectively. The $V_{\rm T}$ values of bulk Si and s-Si p-MOSFETs under different kinds of strains are extracted by linear extrapolation. The maximum $V_{\rm T}$ variation for the same p-MOSFET under different mechanical strain conditions is 0.01 V, and the $V_{\rm T}$ difference between s-Si and bulk Si p-MOSFETs is 0.015 V. Since the $E_{\rm eff}$ change caused by these variations is minor, the average value of −0.8 V is taken in the analysis.

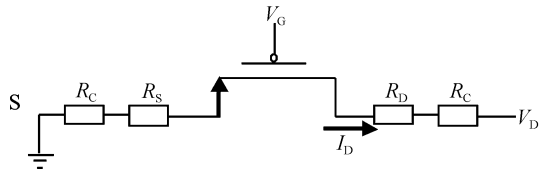

Fig. 3. Equivalent model of p-MOSFET considering parasitic resistances.

The effective hole mobility ($\mu_{\rm h}$) was extracted from the linear regime device current[12], given by

$$I_{\rm D} = \frac{W}{L}\mu_{\rm h} C_{\rm OX}(V_{\rm GS} - V_{\rm T})V_{\rm DS},$$

where W and L are both 20 μm for all the measured MOSFETs, $C_{\rm ox}$ is the oxide capacitance, and $V_{\rm DS}$ is −50 mV.

However, neglecting source/drain series resistance ($R_{\rm S}/R_{\rm D}$) and contact resistance ($R_{\rm C}$) in the p-MOSFET causes the effective mobility to be underestimated. In order to quantitatively check the impacts of these parasitic resistances, the expression of drain current in the linear regime can be revised as:

$$I_{\rm D} = \frac{W}{L}\mu_{\rm h} C_{\rm OX}\left[V_{\rm GS} - V_{\rm T} - I_{\rm D}(R_{\rm s} + R_{\rm C})\right] \times \left[V_{\rm DS} - I_{\rm D}(R_{\rm s} + R_{\rm D} + 2R_{\rm C})\right],$$

according to the equivalent model of a p-MOSFET considering $R_{\rm S}/R_{\rm D}$ and $R_{\rm C}$ (Fig. 3).

The process control monitor region in the same wafer with observed p-MOSFETs shows that BF_2 implantation (with an implant energy of 30 keV, and a dose of 3×10^{15} cm^{-2}) in the source/drain region of the p-MOSFET induces ~80 Ω sheet resistance in these regions, and the specific resistance is 4×10^{-6} Ω·cm^2 in the contact. Calculating the resistances with L/W= 0.125 of the source/drain region, and S = 8.64 μm^2 of the contact region, the $R_{\rm S}/R_{\rm D}$ value is 10 Ω, and $R_{\rm C}$ is about 46 Ω. The experiment also shows that the maximum value of $I_{\rm D}$ in the observed p-MOSFETs is less than 8×10^{-6} A. Thus, it is reasonable to neglect the product of $I_{\rm D}^2(R_{\rm S} + R_{\rm C})$ $(R_{\rm D} + R_{\rm S} + 2R_{\rm C})$, and $\mu_{\rm h}$ in this case can be extracted by:

$$\mu_{\rm h} = \left(\frac{W}{L}C_{\rm OX}\right)^{-1} \times \frac{I_{\rm D}}{(V_{\rm GS} - V_{\rm T})\,V_{\rm DS} - I_{\rm D}(R_{\rm s} + R_{\rm C})(2V_{\rm GS} - 2V_{\rm T} + V_{\rm DS})}.$$

If $\mu_{\rm h}$ and $\mu_{\rm h,0}$ represent the hole effective mobility with and without counting the source/drain and contact resistance, then

$$\frac{\mu_{\rm h,0}}{\mu_{\rm h}} = 1 - \frac{(R_{\rm s} + R_{\rm C})(2V_{\rm GS} - 2V_{\rm T} + V_{\rm DS})}{(V_{\rm GS} - V_{\rm T})\,V_{\rm DS}} I_{\rm D}.$$

The largest $\mu_{\rm h}$ variation happens under the largest $I_{\rm D}$ value. So take $I_{\rm D} = 8 \times 10^{-6}$ A to estimate the largest $\mu_{\rm h}$

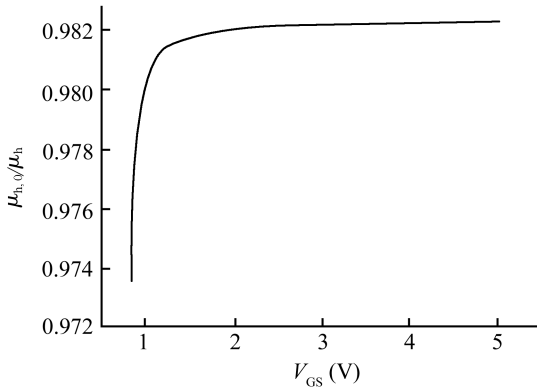

Fig. 4. $\mu_{h,0}/\mu_h$ as a function of V_{GS}.

variation, and plot the ratio of $\mu_{h,0}$ to μ_h versus V_{GS} (Fig. 4). The result shows that the μ_h variation is less than 2.6% in the entire V_{GS} range, and this variation in extraction is identical for a single I_D–V_{GS} relationship. Moreover, though I_D changes under strain, its maximum variation is less than 10^{-6} A, thus the $\mu_{h,0}/\mu_h$ variation for the same p-MOSFET under strain is about 0.2%, which will contribute little violation to the μ_h enhancement factor. In sum, neglecting parasitic resistances can still provide a relatively accurate value for hole mobility, especially the mobility enhancement factor. Therefore, the results in the following analysis are based on the extraction method without considering source/drain and contact resistance impacts for a close approximation.

Once the effective field and effective mobility are calculated, the characteristics of μ_h can be obtained and analyzed.

4. Results and discussion

4.1. Additive uniaxial strain on bulk Si p-MOSFETs

In Fig. 5, the hole mobility values are extracted using the parasitic resistance model. It shows that μ_h is reduced/increased under uniaxial tensile/compressive strains, and the mobility change is larger in the ⟨110⟩ direction than in the ⟨100⟩ direction. The mechanism of these phenomena has been explained in previous work[4, 13], in which shear-stress-induced band warping is the main factor.

The profile of the hole mobility versus effective vertical electric field in Fig. 5 can be divided into three regions: Coulomb scattering (0.25–0.35 MV/cm), phonon scattering (0.35–0.5 MV/cm), and surface roughness scattering (0.6–0.75 MV/cm) region. As stated[14], the E_{eff} dependence of carrier mobility varies in the surface roughness scattering region with different channel surface roughness values, and therefore the constant enhancement in this region (Fig. 6) indicates that the additive mechanical stress does not alter the channel surface roughness. Therefore, in the surface roughness scattering region, the ratio of hole mobility with strain to that without strain reflects changes of m^* (transport effective mass) and m_{dp} (density of states effective mass)[8]:

$$\frac{\mu_{sr}}{\mu_{sr,0}} \propto \left(\frac{m_{dp}m^*}{m_{dp,0}m_0^*}\right)^{-1}.$$

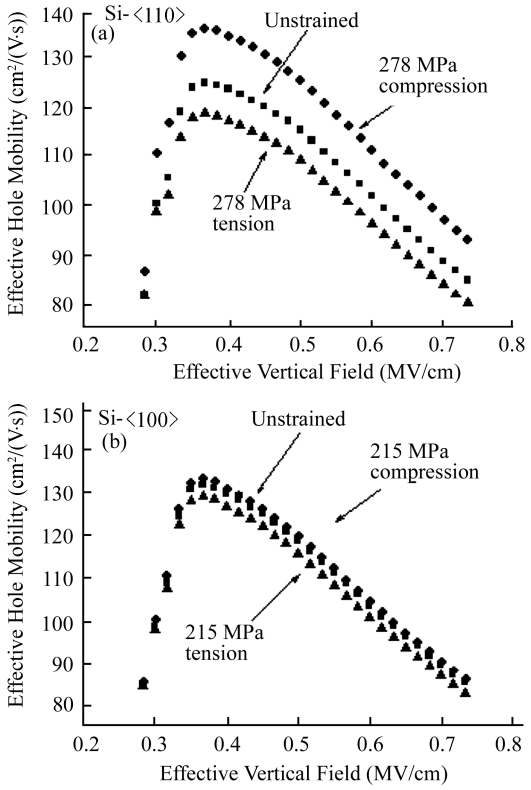

Fig. 5. Hole mobility versus E_{eff} in bulk Si p-MOSFET under additive uniaxial longitudinal compressive and tensile strains in (a) ⟨110⟩ and (b) ⟨100⟩ directions.

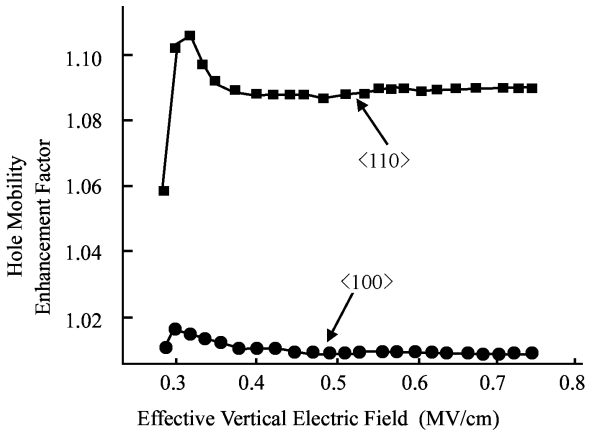

Fig. 6. Hole mobility enhancement versus E_{eff} of bulk Si p-MOSFET under 0.16% additive uniaxial compressive stresses in different directions.

Though there is an increase in m_{dp} under ⟨110⟩ compressive strain[5], it is offset by the more drastic m^* decrease.

In the Coulomb scattering region, μ_C has a dependence on N_s (hole inversion density)[15]:

$$\frac{\mu_C}{\mu_{C,0}} = \left(\frac{N_s}{N_{s,0}}\right)^{1/2},$$

where N_s is decided by:

$$N_s = 2\left(\frac{m_{dp}K_BT}{2\pi\hbar^2}\right)^{3/2} e^{-(E_f-E_{V,ch})/kT}.$$

According to Ref. [16], $E_{V,ch}$ (energy of valence band edge in the channel at the Si surface) changes little in the observed

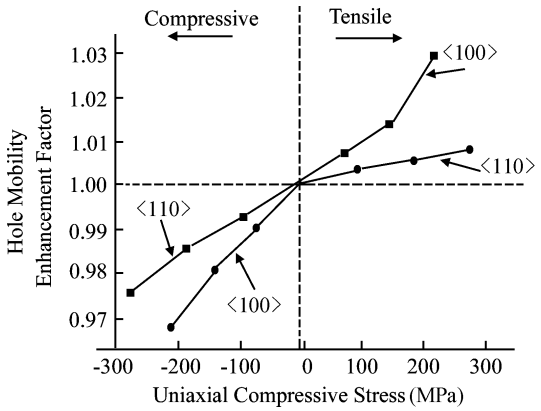

Fig. 7. Hole mobility enhancement under additive uniaxial strains on biaxial s-Si p-MOSFETs at E_{eff} = 0.7 MV/cm. μ_{h} increases and decreases under additive uniaxial tensile and compressive strain, respectively.

strain range, thus when Coulomb scattering dominates it can be concluded that:

$$\frac{\mu_{\text{C}}}{\mu_{\text{C},0}} = \left(\frac{m_{\text{dp}}}{m_{\text{dp},0}}\right)^{3/4} \left(\frac{m^*}{m_0^*}\right)^{-1},$$

in which m^* and m_{dp} remain constant in different vertical fields[13]. Since in the Coulomb scattering region, hole mobility has a positive exponential dependence on m_{dp}, in contrast with the negative dependence in the surface roughness scattering region, it can be envisioned that an m_{dp} increase will result in a higher mobility enhancement in the low field relative to that in the high field. Figure 6 shows a corresponding result in which hole mobility enhancement reaches a peak value at E_{eff} = 0.3 MV/cm. Similar results can be obtained for compressive strain along the ⟨100⟩ direction.

4.2. Additive uniaxial strain on biaxial s-Si p-MOSFETs

Figure 7 shows that the mobility gain under additive uniaxial mechanical compressive strain of the bulk Si p-MOSFET is not transportable to the biaxial s-Si p-MOSFET. On the contrary, the increase of mobility occurs under additive uniaxial tensile strain.

Since the uniaxial strain effect on μ_{h} is very different in the ⟨110⟩ and ⟨100⟩ directions[5, 9], the physics of additive uniaxial strain should be discussed separately. For ⟨110⟩ s-Si p-MOSFETs, the addition of 0.16% uniaxial tensile strain results in an additive 0.08% biaxial tensile strain and an additional 0.08% positive shear strain (shown in Fig. 8)[6]. Table 1 shows the mass change caused by inter-wing (between in-plane and out-of-plane wings, or different regions of the in-plane wings in the top band) redistribution and scattering change caused by band-splitting under biaxial tensile and shear stress, where '+' and '−' mean the increase and decrease of effective mass or scattering rate respectively.

It can be seen that under additive uniaxial tensile stress, the effective mass is increased, and scattering is suppressed/enhanced by the biaxial/shear strain component. The experimental result shows that when the s-Si on the SiGe virtual substrate has a biaxial stress of 1.4 GPa, the 278 MPa

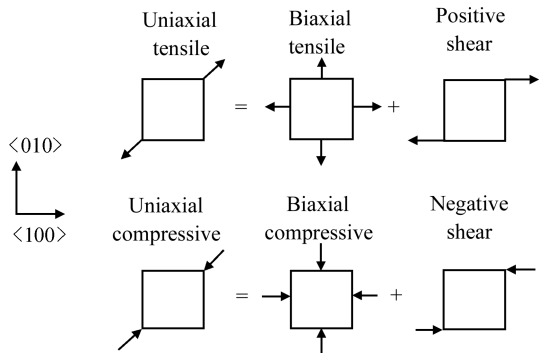

Fig. 8. Equivalent effect of uniaxial ⟨110⟩ stress.

Table 1. Biaxial tensile and shear stress effects on effective mass change of the conduction band[13].

	Inter-wing mass change	Scattering rate
Increased biaxial tension	+	−
Decreased biaxial tension	−	+
Positive shear	+	+
Negative shear	−	−

additional uniaxial tensile stress increases hole mobility, which means that the scattering suppression induced by increased biaxial tension is a dominant factor in this case. In the same way, under additional uniaxial compressive strain, counteraction between mass and scattering is also present (Table 1), and reduced mobility also shows that scattering change caused by decreased biaxial tensile strain prevails. In sum, when the biaxial strain is higher than 1 GPa, which is believed to cause enough band-splitting-induced scattering reduction, and is much larger than the uniaxial strain, the additional biaxial strain-induced scattering change is more crucial.

Further, for the SiGe-induced biaxial strained-Si, hole mobility enhancement has a linear dependence on Ge fraction in the 20%–30% Ge fraction region in the low field[17], so it is reasonable to interpolate hole mobility enhancement on $Si_{0.78}Ge_{0.22}$ over that on $Si_{0.8}Ge_{0.2}$ to be 6% at E_{eff} = 0.4 MV/cm, according to the result that the co-produced s-Si p-MOSFET with $Si_{0.7}Ge_{0.3}$ substrate has about 30% mobility enhancement over that with $Si_{0.8}Ge_{0.2}$ substrate[12]. The $Si_{0.78}Ge_{0.22}$ substrate means an addition of 0.08% biaxial tensile strain over the $Si_{0.8}Ge_{0.2}$ substrate, which is equal to the additional biaxial component in the ⟨110⟩ tensile strain on $Si_{0.8}Ge_{0.2}$-induced strained-Si. However, adding the shear strain portion, μ_{h} enhancement at E_{eff} = 0.4 MV/cm is only 1%, demonstrating that shear-strain-induced band-warping plays a significant contradictory role.

In addition, the mobility change under uniaxial strain for s-Si p-MOSFETs is larger in the ⟨100⟩ direction than in the ⟨110⟩ direction (as shown in Fig. 9), opposite to the situation in bulk Si p-MOSFETs. This is consistent with the aforementioned shear stress's role. The lack of shear component in ⟨100⟩ strain means that fewer factors are contradicting the uniaxial strain induced scattering suppression. However, in order to get a quantitative result, further calculation of band

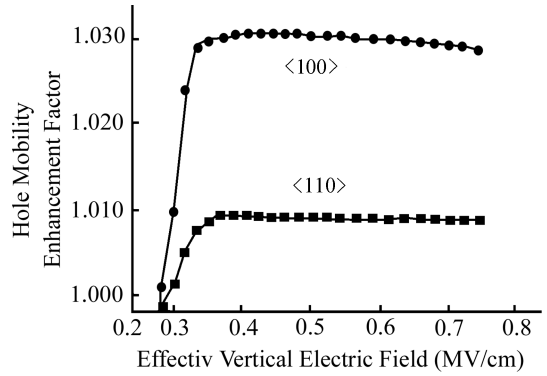

Fig. 9. Hole mobility enhancement versus $E_{\rm eff}$, for s-Si P-MOSFETs under additive 0.16% uniaxial mechanical tensile strain.

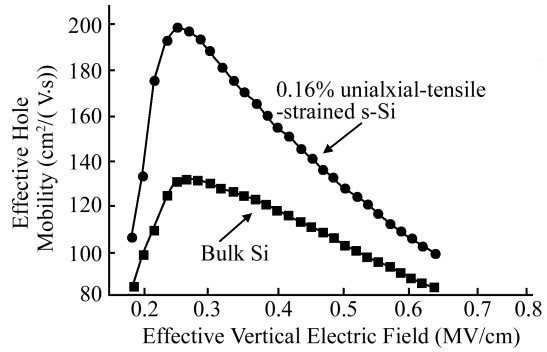

Fig. 10. Comparison of $\mu_{\rm h}$ versus $E_{\rm eff}$ between bulk Si and additive uniaxial-tensile-strained s-Si along the ⟨100⟩ direction.

shape under ⟨100⟩ strain should be carried out.

The mobility gain by additive uniaxial strain on s-Si p-MOSFETs remains rather constant in the high field region (see Fig. 9), unlike the case with biaxial tensile strain only, in which mobility enhancement decreases rapidly as $E_{\rm eff}$ increases[8]. This is an implication that the positive shear stress balances the out-of-plane mass decrease of the top band (relative to the second band) caused by additional biaxial tensile, since the larger out-of-plane mass is responsible for the enhancement loss at high vertical field. However, by comparing the s-Si p-MOSFET under external uniaxial strain to the bulk Si p-MOSFET (as shown in Fig. 10), it is found that hole mobility still experiences a gain loss at high field, which is a key drawback for the implementation of combinational strain technology in present CMOS technology.

Though strained Si technology based on a relaxed SiGe substrate has developed greatly over many years, it will be replaced by the present process-induced uniaxial strain technology, due to the hole mobility enhancement loss in the high vertical field, as well as the electron mobility enhancement saturation when Ge content exceeds 20%[18]. However, with high levels of stress (>1 GPa), hole mobility can be further increased by band-warping and band-splitting effects, especially under ⟨110⟩ direction compressive strain. Meanwhile, electron mobility also increases above 1 GPa stress under ⟨110⟩ direction tensile stress[19]. Thus, a uniaxial strain process for ⟨110⟩ channel CMOS devices is the best choice for carrier mobility enhancement. It is necessary that the stress is higher than 1 GPa, and the mobility enhancement is not degraded by other effects in the strain-inducing process. In addition, the hole mobility enhancement peak (Fig. 6) for bulk Si under uniaxial compression indicates that uniaxial strain-Si p-MOSFETs should operate in the high vertical field region, to avoid the large variation of mobility in the low field region.

5. Conclusion

For bulk Si p-MOSFETs, it is found that under longitudinal uniaxial compressive strain, there is a mobility enhancement peak in the low field, due to the band-warping-induced density of state effective mass increase.

For s-Si p-MOSFETs along the ⟨110⟩ channel, the hole mobility is enhanced under additive tensile strain, because the effects of scattering rate change exceed that of the effective mass change. Also, ⟨100⟩ direction tensile strain is more successful in enhancing hole mobility than ⟨110⟩ direction, in contrast with the result in bulk Si. Meanwhile, there exists an enhancement loss at high vertical field for combinational strain. A comparison between uniaxial and biaxial strain indicates that for p-MOSFETs uniaxial strain is a better choice to further the strain technology.

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