A high efficiency charge pump circuit for low power applications*

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Abstract: A high efficiency charge pump circuit is designed and realized. The charge transfer switch is biased by the additional capacitor and transistor to eliminate the influence of the threshold voltage. Moreover, the bulk of the switch transistor is dynamically biased so that the threshold voltage gets lower when it is turned on during charge transfer and gets higher when it is turned off. As a result, the efficiency of the charge pump circuit can be improved. A test chip has been implemented in a 0.18 μm 3.3 V standard CMOS process. The measured output voltage of the eight-pumping-stage charge pump is 9.8 V with each pumping capacitor of 0.5 pF at an output current of 0.18 μA, when the clock frequency is 780 kHz and the supply voltage is 2 V. The charge pump and the clock driver consume a total current of 2.9 μA from the power supply. This circuit is suitable for low power applications.

Key words: high efficiency; low power; charge pump circuit; high-voltage generator; standard CMOS process
DOI: 10.1088/1674-4926/31/1/015009 **EEACC:** 1210

1. Introduction

Charge pump (CP) circuits have been widely used in modern circuit systems, for example, embedded nonvolatile memories[1]. Most charge pumps are based on the circuit proposed by Dickson[2], as shown in Fig. 1. It comprises charge transfer diodes and charge pumping capacitors. Clock signals CLK and CLKB are anti-phased with an amplitude of V_{DD} to control the charge and discharge processes on the pumping capacitors. The circuit pumps charge from the power supply to the output terminal stage by stage to increase the output voltage V_{out}. In the Dickson charge pump, the diodes are implemented with diode-connected NMOS transistors. However, these diodes suffer from voltage loss because of the threshold voltage and body effect. So the efficiency of the Dickson charge pump is very low, especially at low input voltage. Several modified charge pump circuits have been reported to increase the pumping efficiency. Two auxiliary MOSFETs are used to dynamically bias the bulk of the switch transistor so that the body effect of the transistors can be eliminated and the efficiency can be improved[3]. However, the circuit is still influenced by the constant threshold voltage of the switch transistors. To solve this problem, a four-phase clock is designed to control the charge transfer process. However, the clock generation circuit consumes additional power[4].

This paper presents a new high efficiency charge pump circuit. The charge transfer switch is biased by the additional capacitor and transistor to eliminate the influence of the threshold voltage. Moreover, the bulk of the switch transistor is dynamically biased, so that the threshold voltage gets lower when it is turned on during charge transfer and gets higher when it is turned off. So the pumping gain of each stage can be improved to achieve high efficiency. Firstly, the architecture and operation principles of the charge pump are explained. Then, a comparison is made with Dickson's and Shin's charge pumps in the simulation results. Finally, the measured results and the conclusions are given.

2. A high efficiency charge pump circuit

2.1. Charge pump circuit

The architecture of the charge pump circuit is shown in Fig. 2. It comprises N pumping stages, an additional stage and an output stage. Clock signals CLK and CLKB are anti-phased with an amplitude of V_{DD}. The first pumping stage consists of a PMOS transistor M_{11} operating as the charge transfer switch, a pumping capacitor C_1 and an auxiliary PMOS transistor M_{12}. In other pumping stages, a small auxiliary capacitor C_{ia} is added between the gate of the switch transistor and the clock. The bulk of transistor M_{11} is connected to node net_3, the bulks of transistors M_{i1} and M_{i2} are connected to node net_i+2 (i = 2, 3, $\cdots$, N–1), the bulks of transistors M_{N1}, M_{N2}, M_{a1}, M_{a2}, M_{a3}, M_{o1} and M_{o2} are connected to the gate of transistor M_{a3}. The additional stage is just used to bias the bulks of the PMOS transistors in the (N–1)th stage, the Nth stage and the output stage. It should be noted that the charges are not transferred from the additional stage to the output stage. So the capacitor C_{a1} in the additional stage is smaller than the

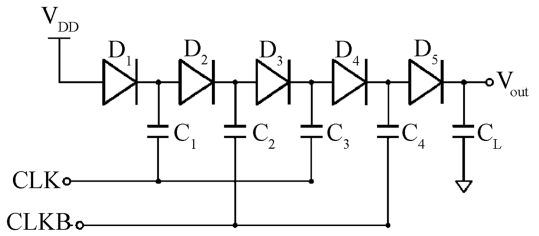

Fig. 1. Dickson charge pump circuit.

* Project supported by the Chinese National High-Tech Research and Development Program (No. 2006AA04A108) and the National Natural Science Foundation of China (No. 2008AA010703).
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Received 9 April 2009, revised manuscript received 21 September 2009

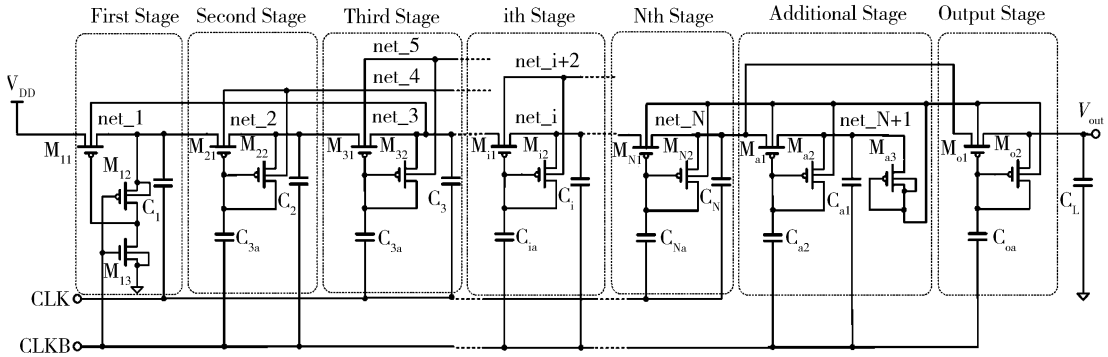

Fig. 2. High efficiency charge pump circuit.

pumping capacitors in the previous stages. The output stage is almost the same as the pumping stages except there is no pumping capacitor.

In this charge pump circuit, a diode-connected PMOS transistor M_{i2} is added between the gate and source (drain) of the PMOS charge transfer switch M_{i1} ($i > 1$). As a result, the voltage of node net_i is always a threshold voltage higher than the gate voltage of M_{i1} so the voltage loss on the switch is very small during charge transfer. Then the auxiliary capacitor C_{ia} ($i > 1$) is added between the gate of M_{i1} and clock CLK or CLKB. The function of the capacitor is to prevent charges from transferring backwards. Taking the second pumping stage for example, when the clock CLKB (CLK) changes from low (high) to high (low), the transistor M_{21} is switched off to stop charges transferring from node net_1 to node net_2. During the transition of the transistor M_{21} from switch-on state to switch-off state, the auxiliary capacitor C_{2a} can speed up the increase in the gate voltage of M_{21} and make M_{21} cut off very quickly (before M_{22} turns on to charge up the gate of M_{21}), so that the charges are prevented from transferring backwards from node net_2 to node net_1. Furthermore, the bulk of the transistor M_{i1} is connected to node net_i+2. When the transistor M_{i1} is switched off (on), the potential of the bulk is increased (decreased), so that its threshold voltage gets higher (lower) due to the body effect. The connection method can improve the efficiency of the charge pump. The detailed operation of the charge pump circuit is described below.

2.2. Operation of the charge pump circuit

For convenience of analysis, it is supposed that the parasitic capacitance and the output current are zero. When the anti-phase clock signals with an amplitude of V_{DD} are imposed on the pumping capacitors, each pumping node has a high level voltage and a low level voltage; the difference between the high and low levels is V_{DD}.

During the first half clock cycle, signal CLK (CLKB) is low (high). In the first stage, the transistor M_{13} is turned on and the transistor M_{12} is turned off. As a result, the transistor M_{11} is turned on and the charges are transferred from the power supply to node net_1 until the voltage of node net_1 equals V_{DD}. In the second stage the gate voltage of transistor M_{21} is increased by capacitor C_{2a}, so the transistor M_{21} is turned off.

During another half clock cycle, signal CLK (CLKB) becomes high (low). In the first stage, the voltage of node net_1 is increased to $2V_{DD}$ by the capacitor C_1. The transistor M_{13} is turned off and transistor M_{12} is turned on. As a result, the transistor M_{11} is turned off to cut off the leakage path from node net_1 back to the power supply. In the second stage, the gate voltage of the transistor M_{21} is decreased by the capacitor C_{2a}, so the transistor M_{21} is turned on and the charges are transferred from node net_1 to node net_2.

It can be found that in steady state when signal CLK (CLKB) becomes high (low) the voltage of net_1 is $2V_{DD}$. Because of the auxiliary PMOS transistor M_{22}, the gate voltage of transistor M_{21} is not higher than $2V_{DD} - V_{TH}$. So the lower voltage of node net_2 is almost $2V_{DD}$ and the higher voltage of node net_2 is almost $3V_{DD}$. In this way, the influence of the threshold voltage of the charge transfer switch can be almost eliminated. As a result, the gain of each pumping stage and the efficiency of the charge pump circuit are improved.

If the parasitic capacitance and the output current are taken into account, the voltage gain of each pumping stage can be expressed as[5]

$$\Delta V = V_{\mathrm{clk}} \frac{C_{\mathrm{i}}}{C_{\mathrm{i}} + C_{\mathrm{s}}} - \frac{I_{\mathrm{o}}}{f_{\mathrm{clk}}(C_{\mathrm{i}} + C_{\mathrm{s}})} - V_{\mathrm{s}}, \qquad (1)$$

where V_{clk} is the voltage amplitude of the clock signals, C_{i} is the pumping capacitance, C_{s} is the parasitic capacitance at each pumping node, I_{o} is the output current, f_{clk} is the clock frequency and V_{s} is the voltage loss on the charge transfer switch. From Eq. (1), it can be inferred that the current driving ability can be improved by increasing the clock frequency and decreasing the parasitic capacitance and the power efficiency can be improved by decreasing the parasitic capacitance and the voltage loss on the charge transfer switch. So a high current driving ability does not necessarily mean high power efficiency.

Supposing the critical current on the switch transistor is I_{c} before it is switched from the on-state to the off-state, in the ith pumping stage, V_{s} is equal to the voltage difference between the source (net_i -1) and the drain (net_i) when the current on the switch decreases to I_{c}. The relation between I_{c} and V_{DS} can be expressed as

$$I_{\mathrm{c}} = -I_{\mathrm{DS}} = \mu_{\mathrm{p}} C_{\mathrm{ox}} \frac{W}{L} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{1}{2} V_{\mathrm{DS}}^2 \right], \qquad (2)$$

where I_{DS} is the current from the drain to the source, μ_{p} is the channel mobility of the PMOS transistor, C_{ox} is the gate oxide

capacitance per unit area, W and L are the width and length of the switch transistor, V_{GS} is the voltage difference between the gate and the source, V_{TH} is the threshold voltage of the switch transistor, and V_{DS} is the voltage difference between the drain and the source. As a diode-connected PMOS transistor is added between the drain and the gate of the switch transistor, V_{GD} is approximately V_{TH}. The relation between V_{GS} and V_{DS} is

$$V_{GS} = V_{GD} + V_{DS} = V_{TH} + V_{DS}. \quad (3)$$

Substituting for V_{GS} in Eq. (2) and rearranging, V_s can be expressed as

$$V_s = -V_{DS} = \sqrt{\frac{2I_c}{\mu_p c_{ox}\frac{W}{L}}}. \quad (4)$$

In the traditional charge pump, V_s is usually larger than the threshold voltage. In this charge pump, as I_c is very small, the voltage loss on the switch V_s is much smaller than the threshold voltage. Compared with the traditional charge pump, the voltage gain in this charge pump circuit is improved significantly. Many other choices can also be found in Eq. (1) to improve the voltage gain of each pumping stage. I_o is usually determined by the output load and it is hard to cut down. The voltage amplitude and the frequency of the clock signals, or the pumping capacitance can be increased. However, these methods mean that more power and chip area are consumed.

2.3. Simulation and discussion

Three kinds of eight-pumping-stage charge pump circuits, this charge pump, Dickson's charge pump and Shin's charge pump, were designed and simulated in a 0.18 μm 3.3 V CMOS process. Figure 3 shows the simulated results of these charge pumps with only capacitive load under different power supply voltages. The pumping capacitor is 0.5 pF and the clock frequency is 780 kHz. As shown in Fig. 3, the output voltages of these circuits are degraded when the supply voltage is decreased. However, the proposed charge pump has higher output voltages under the same supply voltages. Because the proposed charge pump can output a higher voltage under the same pumping capacitor, stage number, capacitive load, supply voltage and clock frequency, it indicates that the proposed charge pump circuit has better pumping efficiency than the Dickson charge pump and Shin's charge pump.

In the proposed charge pump, the charge transfer switch plays an important role in obtaining high efficiency, and the simulated voltage waveforms on node net_1, node net_2, the gate and bulk of M_{21} with only capacitive load in steady state are shown in Fig. 4. The supply voltage is 2 V. As shown in Fig. 4, during the second half clock cycle, when the charges are transferred from node net_1 to node net_2, the lower voltage of node net_2 is very close to the higher voltage of node net_1. The voltage difference is less than 0.2 V, which is much smaller than the threshold voltage of the switch transistor. This means that the voltage loss on the charge transfer switch could be almost eliminated, i.e. V_s in Eq. (1) is much decreased. As a result, the efficiency of the charge pump is greatly improved.

Simulated voltage waveforms on node net_1, node net_2, the gate and bulk of M_{21} with a 54 MΩ resistive load in steady state are shown in Fig. 5. As the charge pump outputs a current to the load, the voltage on the pumping node changes during the half clock cycle. Although the bulk voltage of transistor M_{21} is always higher than its source voltage (the higher voltage of node net_1 and node net_2), the voltage difference between the bulk and the source is higher during the first half clock cycle when M_{21} is turned off and is lower during the second half clock cycle when M_{21} is turned on. As a result of the body effect, the threshold voltage of transistor M_{21} gets lower when it is turned on and gets higher when it is turned off. This can improve the efficiency of charge transfer and stop the charges from transferring backward. Furthermore, the gate voltage of M_{21} is always lower than the drain voltage of M_{21}, so it acts as a PMOS transfer gate, which results in only a little voltage loss. During the end of the charge transfer in the second half clock cycle, the lower voltage of node net_2 is also very close to the higher voltage of node net_1 which indicates that the charges are transferred with high efficiency.

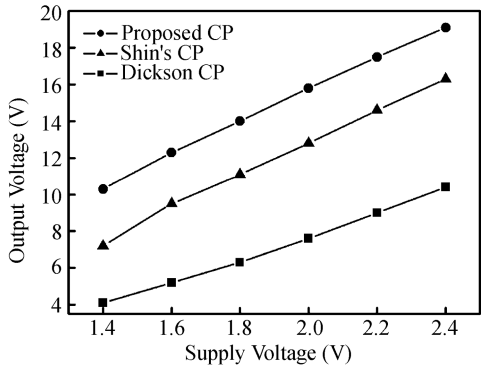

Fig. 3. Simulated results of the eight-pumping-stage charge pump circuits with only capacitive load.

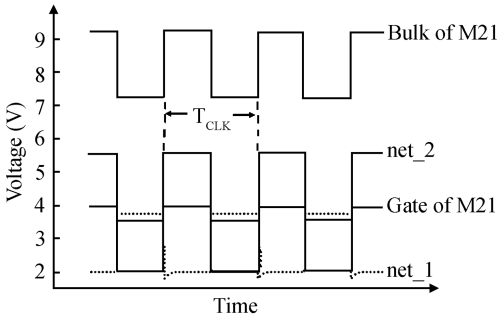

Fig. 4. Simulated voltage waveforms on net_1, net_2, the gate and bulk of M_{21} with capacitive load in steady state.

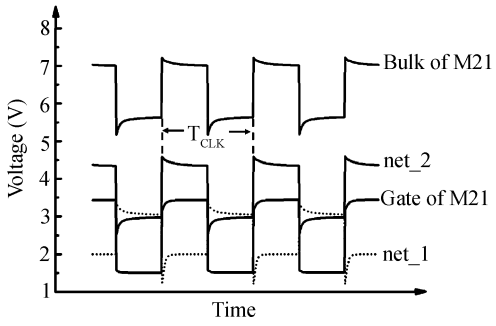

Fig. 5. Simulated voltage waveforms on net_1, net_2, the gate and bulk of M_{21} with a resistive load of 54 MΩ in steady state.

Table 1. Performance comparison.

Parameter	Ref. [4]	Ref. [6]	This work
Process	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS
Supply voltage (V)	2	2.5	2
Pumping stage number	11	8	8
Total pumping capacitor (pF)	88	80	4
Clock frequency (MHz)	30 (4 phase)	1 (2 phase)	0.78 (2 phase)
Output voltage (V)	19	20	9.8
Output current (μA)	100	2	0.18
Q (μW/(MHz · pF))	0.72	0.5	0.57

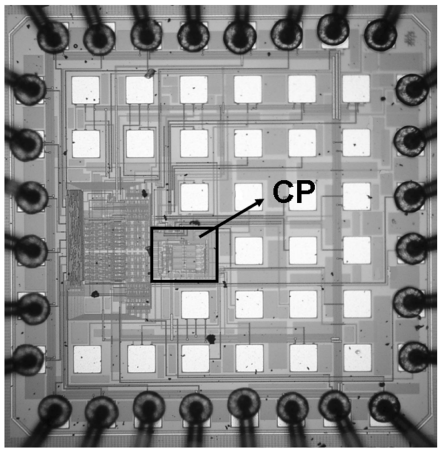

Fig. 6. Chip photograph of the charge pump circuit.

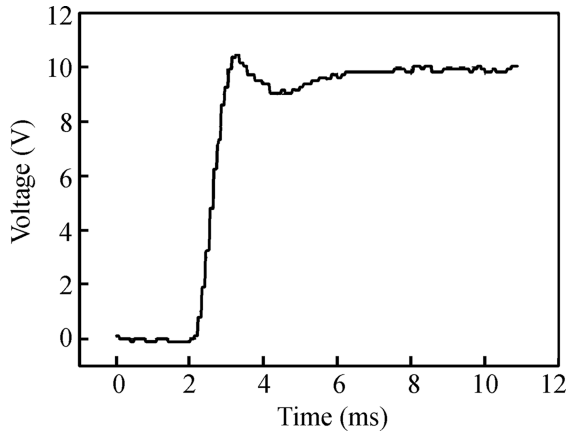

Fig. 7. Measured output waveform of the charge pump circuit with a resistive load of 54 MΩ and clock frequency of 780 kHz.

3. Implementation and result

The eight-pumping-stage charge pump circuit has been fabricated in a 0.18 μm 3.3 V standard CMOS process. A photograph of the chip is shown in Fig. 6. The charge pump area is 154×105 μm^2. Figure 7 shows the measured output waveform of the charge pump circuit with a load resistor of 54 MΩ. The pumping capacitor is 0.5 pF. The clock frequency is 780 kHz and the power supply voltage is 2 V. The charge pump and the clock driver consume a total current of 2.9 μA from the power supply. The charge pump starts to work at the time of 2 ms. The waveform indicates that the output voltage of the charge pump is 9.8 V and the output current is 0.18 μA. The measured and

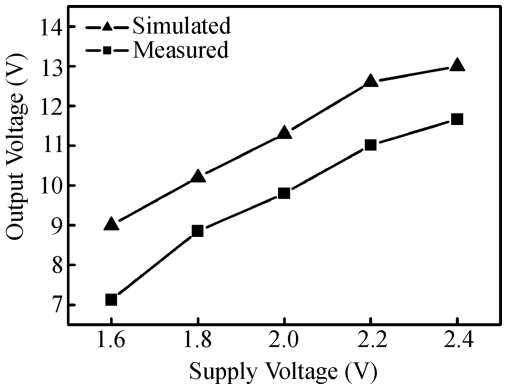

Fig. 8. Measured and simulated output voltages under different power supply voltages with a resistive load of 54 MΩ and clock frequency of 780 kHz.

simulated output voltage of the charge pump under different power supply voltages with a load resistor of 54 MΩ is shown in Fig. 8. The measured output voltage is lower than the simulated output voltage under the same supply voltage, because of the parasitic resistance and capacitance of the test chip, the bonding wires, and the packages. The parasitic resistance and capacitance may result in overlapping clock signals, which will lower the pumping efficiency[5]. Furthermore, the capacitors in the circuit are implemented with PMOS transistors to minimize the area, and the large parasitic capacitance between the n-well and p-substrate is not included in the simulation.

Finally, Table 1 compares this work with previous research. The index Q is defined to compare the performance of the circuits. It is expressed as

$$Q = \frac{P_{\text{out}}}{f_{\text{clk}} C_{\text{pump}}}, \tag{5}$$

where P_{out} is the output power of the charge pump, f_{clk} is the clock frequency and C_{pump} is the sum of the pumping capacitors. In Eq. (5), C_{pump} determines the area of the circuit, and the product of f_{clk} and C_{pump} determines the power consumption. So a larger Q means that the charge pump can supply more power with the same area and power consumption. As shown in Table 1, the performance of this charge pump circuit is much better than the one using a two-phase clock and is close to that of the charge pump controlled by a four-phase clock.

4. Conclusions

A high efficiency charge pump circuit is realized in this work. The auxiliary capacitors and transistors are used to dy-

namically bias the charge transfer switches, so that the influence of the threshold voltage of the switch transistor is almost eliminated and the pumping efficiency of the circuit is improved. A test chip was implemented in a 0.18 μm 3.3 V CMOS process. The experimental results show that the output voltage of the eight-stage charge pump circuit was 9.8 V with each pumping capacitor of 0.5 pF under a power supply voltage of 2 V and a clock frequency of 780 kHz. The output current of the charge pump was 0.18 μA. The charge pump and the clock driver consumed a total current of 2.9 μA from the power supply. This charge pump circuit is suitable for low power applications.

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