Fabrication of strained Ge film using a thin SiGe virtual substrate*

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Abstract: This paper describes a method using both reduced pressure chemical vapor deposition (RPCVD) and ultrahigh vacuum chemical vapor deposition (UHVCVD) to grow a thin compressively strained Ge film. As the first step, low temperature RPCVD was used to grow a fully relaxed SiGe virtual substrate layer at 500 °C with a thickness of 135 nm, surface roughness of 0.3 nm, and Ge content of 77%. Then, low temperature UHVCVD was used to grow a high quality strained pure Ge film on the SiGe virtual substrate at 300 °C with a thickness of 9 nm, surface roughness of 0.4 nm, and threading dislocation density of $\sim 10^5$ cm^{-2}. Finally, a very thin strained Si layer of 1.5–2 nm thickness was grown on the Ge layer at 550 °C for the purpose of passivation and protection. The whole epitaxial layer thickness is less than 150 nm. Due to the low growth temperature, the two-dimensional layer-by-layer growth mode dominates during the epitaxial process, which is a key factor for the growth of high quality strained Ge films.

Key words: strained Ge; SiGe virtual substrate; RPCVD; UHVCVD
DOI: 10.1088/1674-4926/30/9/093005 **EEACC:** 0520D; 0520F; 2520C

1. Introduction

As the feature size of of CMOS transistors scales down, the carrier mobility of silicon continually degrades and cannot meet the device performance requirements. New technologies need to be developed to improve the drive current of CMOS transistors. One way is to introduce strains to the silicon channel to increase the electron and hole mobility[1] by changing the band structures, a technology that is already adopted in state-of-the-art CMOS technology[2, 3]. Another way is to apply new channel materials with high mobility into CMOS technology, such as III–V compound semiconductor materials and germanium (Ge). The hole mobility of bulk Ge is about 1900 cm^2/(V·s), which is four times higher than that of Si. Compressively strained Ge material has exhibited the highest hole mobility among currently used semiconductor materials. There is a 4.2% lattice mismatch between Si and Ge. For Ge grown directly on a Si (001) substrate, the growth is defect-free only below the critical thickness which is about 1 nm[4]. For a layer thickness above the critical thickness, dislocations will nucleate at the interface of the two materials, with threading segments of dislocations running through the layer to the surface. The resulting threading dislocation density can be as high as 10^9 cm^{-2} [5, 6], which is too high for MOSFETs. The general rule of thumb is that the dislocation density should be below 10^4 cm^{-2} for MOS minority-carrier devices for normal operation[6]. The most widely used method to reduce the dislocation density is to employ a relaxed high Ge content SiGe buffer layer as a virtual substrate for growing Ge[7–10]. There are two popular methods for growing this SiGe virtual substrate. One is the compositionally graded buffer layer technique, where the Ge content in SiGe increases gradually as the epitaxial layer thickness grows. Dislocation nucleation is minimized by maintaining low strain rates, while elevated temperatures are used in order to maximize dislocation slip velocity and strain relaxation[11]. The drawback of this method is the thick epitaxial layer, more than several micrometers, and the surface roughness is also high. Moreover, due to the low thermal conductivity of the incorporated Ge material, device self-heating problems will be resulted in, leading to significantly elevated channel temperatures[12, 13]. Another method is the thermal condensation technique, in which a low Ge content SiGe layer is oxidized at high temperature. In this method, during thermal oxidation, Ge acts as a catalyst enhancing the Si oxidation reaction rate while remaining unchanged. Ge atoms are completely rejected from the oxide so they congregate at the SiO_2/SiGe interface and form a Ge-rich layer[14–16]. The disadvantage of this technique is the complexity of the process, and the highest achievable Ge content is limited by the Ge diffusivity in Si. Recently, a UHVCVD process has been developed to grow SiGe/Ge seed/Ge film, in which threading dislocation densities of 5×10^5 cm^{-2} and 6×10^6 cm^{-2} are achieved in 550 nm[17] and 130 nm[18] thick Ge layers, respectively. This paper describes a technique for growing low dislocation density, low surface roughness, and thin strained Ge film using reduced pressure chemical vapor deposition (RPCVD) and ultrahigh vacuum chemical vapor deposition (UHVCVD). First, RPCVD is used to grow thin relaxed SiGe layer as a virtual substrate. Then, UHVCVD is utilized to grow a strained Ge layer on the SiGe virtual substrate. Finally, an ultra-thin

* Project supported by the National Natural Science Foundation of China (Nos. 60636010, 60820106001).
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Received 11 April 2009, revised manuscript received 3 May 2009

strained Si layer is grown on top of the strained Ge layer by UHVCVD, for the purpose of passivation and protection.

2. Experiment

The silicon substrate used in the experiment is an N-type (001) wafer. As the first step, low temperature RPCVD was used to grow a high Ge content SiGe layer as a virtual substrate. The equipment is an Applied Material Centura 200 RPCVD Epi System. SiH_4 and GeH_4 were used as source gases. The Si wafers were cleaned in piranha solution (H_2SO_4 : H_2O_2 = 3 : 1) for 10 min and then dipped in the aqueous HF solution (HF : H_2O = 1 : 10) for 45 s to remove the native oxide layer before epitaxy. After being transferred into the growth chamber, the Si wafer was quickly ramped up to 1100 °C and baked for 100 s, and H_2 was introduced into the chamber at the same time to activate surface Si atoms. The temperature was then reduced to 660 °C to grow a 20 nm Si buffer layer using SiH_4 as precursor with a chamber pressure of 100 Torr. After that, the temperature was dropped to 500 °C, and a target SiGe layer with thickness of 150 nm and Ge content of 80% was grown using SiH_4 and GeH_4 as reacting gases with a chamber pressure of 100 Torr.

On completion of the growth of the SiGe virtual substrate, the wafers were transferred to a custom-built UHVCVD system to grow the strained Ge layer. Before epitaxy, the wafers were dipped in the aqueous HF solution (HF : H_2O = 1 : 10) for 30 s to remove the native oxide layer. After being transferred into the growth chamber, the wafer was baked at 750 °C for 5 min. Then, a target strained Ge layer with a thickness of 10 nm was grown at 300 °C with GeH_4 as precursor. Finally, a 2 nm thick Si layer was grown on the strained Ge layer at 550 °C using SiH_4 as precursor. The reason for growing this ultra-thin Si layer is that Ge oxide is much less stable than SiO_2 and easily dissolved in both dilute acidic and alkaline solutions, even in warm water[16]. The interface between Ge and the gate dielectric is also worse than that of Si. So an ultra-thin Si layer was used for the purpose of protection and passivation. The growth temperature was chosen not only low enough so as not to influence the strain of the Ge layer but also high enough for the decomposition of SiH_4.

Digital Instruments 3100 atomic force microscopy (AFM) was used to measure the surface roughness. JEOL 2010 cross-sectional transmission electron microscopy (XTEM) was used to determine individual film thicknesses and layer morphology. A Siemens D8 discover high resolution double-crystal X-ray diffractometer (DCXRD) was used to measure the Ge content and strain. A secondary ion mass spectrometer (SIMS) was used to accurately measure the Ge content and individual layer thickness. The surface etch-pit density (EPD) method was used to calculate the threading dislocation density. The sample surface was etched in Schimmel solution, and then Hitachi S-5500 scanning electron microscopy (SEM) was used to measure the etch-pit density.

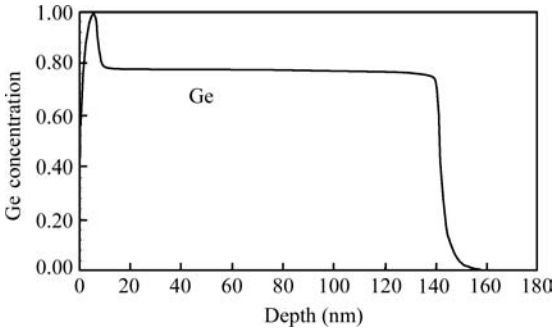

Fig. 1. SIMS curve of the strained Ge sample.

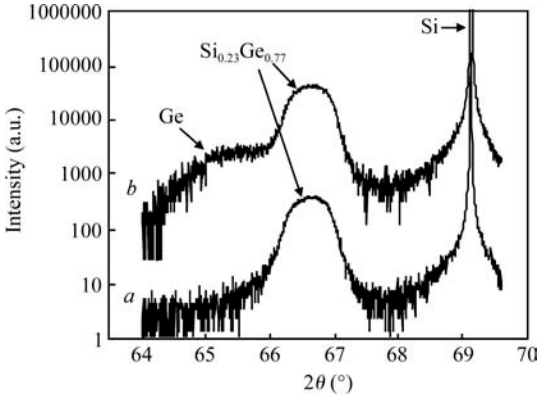

Fig. 2. DCXRD ω–2θ curves of the (004) planes of samples after (*a*) growth of the SiGe virtual substrate layer and (*b*) growth of the strained Ge layer and Si cap layer.

3. Results and discussion

The SIMS curve of the strained Ge sample (Fig. 1) shows the Ge content depth profile of the whole epitaxial layer. From the curve it can be seen that the Si cap layer is about 1.8 nm thick, the pure Ge layer is about 9 nm thick, the SiGe virtual substrate is about 135 nm, and the Ge content in the SiGe layer is about 77%. These results are close to the target values.

The DCXRD ω–2θ curves measuring the diffraction angle of the (004) planes of the samples are shown in Fig. 2. Curve *a* is after the growth of the SiGe virtual substrate using RPCVD. Based on X-ray diffraction theory[19], there is no interferential peak in curve *a*, so the SiGe layer is partially or fully relaxed. The SiGe peak in curve *a* is at 66.6° and the difference between the SiGe and Si peak $\Delta 2\theta$ = 2.512°. Assuming the SiGe layer is fully relaxed, the Ge content is determined by

$$x = \frac{a_{\mathrm{Si}}}{a_{\mathrm{Si}} - a_{\mathrm{Ge}}} \mathrm{ctg}\theta_{\mathrm{Si}} \Delta\theta = \frac{\Delta 2\theta}{3.295},$$

and x = 76% is derived. This value corresponds to the SIMS result. So the SiGe film layer as virtual substrate is almost fully relaxed. Curve *b* was measured after the growth of the strained Ge layer on the virtual substrate using UHVCVD. The SiGe peak remains in the same position, indicating that the 5 min-bake-process at 750 °C has little effect on the SiGe layer. Also, a Ge peak at the left of the SiGe peak appears after UHVCVD, but the Ge layer is so thin that the peak is weak. By data processing, it is found that the Ge peak is at about 65.5° and the

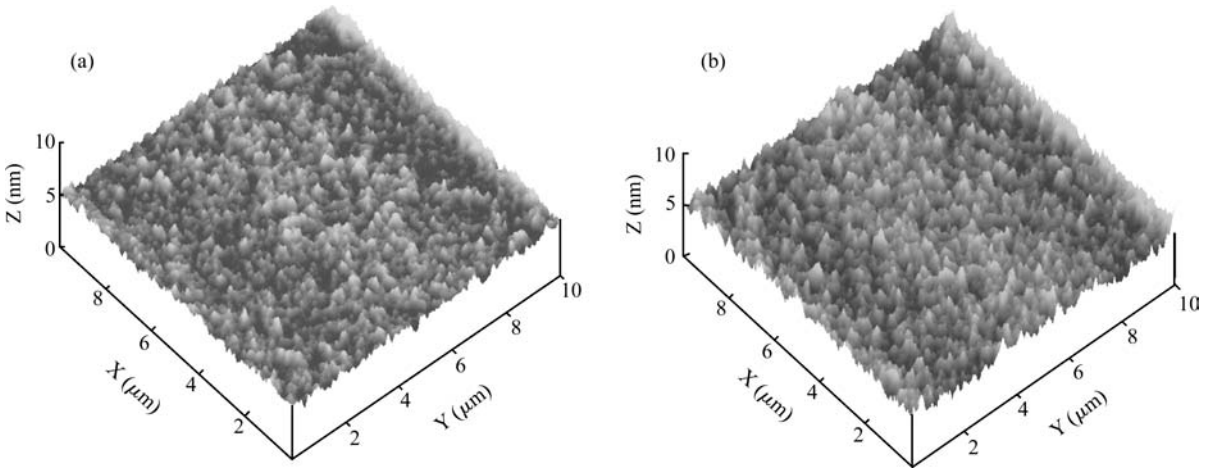

Fig. 3. AFM images of sample surfaces after (a) growth of the SiGe virtual substrate layer, RMS = 0.3 nm, (b) growth of the strained Ge layer and Si passivation layer, RMS = 0.4 nm.

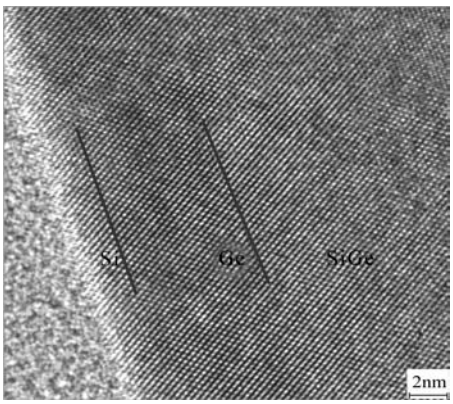

Fig. 4. High resolution XTEM image of the Si/Ge/SiGe interface of the strained Ge sample. No dislocation nucleation has been observed at the Si/Ge/SiGe interfaces.

bulk Ge material (004) diffraction peak is at 65.988°, so the Ge film layer is compressively strained. By calculation, the strain of the Ge film layer is about 0.9%, in agreement with the lattice mismatch due to the Ge content in the SiGe virtual substrate.

Figure 3 shows surface AFM images of samples for a 10 $\times$ 10 μm^2 area. Figure 3(a) denotes the surface after growing the SiGe virtual substrate. The root mean square (RMS) surface roughness of the fully relaxed SiGe layer is 0.3 nm, and there is no obvious crosshatch line appearing, as exists in some low Ge content relaxed SiGe epitaxial layers. This is due to the low growth temperature that two-dimensional layer-by-layer growth adopts during the growing process using RPCVD. Figure 3(b) shows the surface after growing the strained Ge and Si cap layers. The RMS surface roughness is 0.4 nm, which means that during UHVCVD the Ge also grows layer by layer and conforms to the SiGe substrate surface because of the very low growth temperature. The surface is flat enough for fabricating a MOS device without using chemical mechanical polishing.

High resolution cross-sectional transmission electron microscopy (XTEM) images of the Si/Ge/SiGe interface are shown in Fig. 4. The Si cap layer is about 1.8 nm, and the pure Ge layer is about 9 nm. Most of the lattice is perfect and the atom arrangement is in trim order. Because of the small Ge content difference, and the fact that this picture was taken with the <110> axis parallel to the electron beam, there appears little contrast between the strained Ge and $Si_{0.23}Ge_{0.77}$ virtual substrate layers. From the TEM images, we observe only a very small number of dislocations formed at the Si substrate/SiGe interface running through the SiGe layer to the Ge layer. No new dislocation nucleation has been observed at the Ge/SiGe interface, because the critical thickness of Ge on the relaxed $Si_{0.23}Ge_{0.77}$ layer is tens of nanometers.

Figure 5(a) is a high resolution XTEM image of the SiGe/Si substrate interface. Due to the large lattice mismatch between the Si substrate and the SiGe layer, a lot of dislocations nucleate at the interface and extend into the SiGe layer which having an angle of 60° with the interface[15]. Figure 5(b) is an XTEM image of the whole epitaxial layer including the Si cap/Ge/SiGe/Si substrate. The thickest layer is the SiGe silicon layer. In this picture it can also be seen that a great number of dislocations nucleate at the interface of the SiGe/Si substrate, but most of them interact with each other, while only a very small portion runs through the whole epitaxial layer to the surface; thus the dislocation density is greatly reduced.

To identify the threading dislocation density of the strained Ge sample, diluted Schimmel solution (CrO_3:HF:H_2O) is used to etch the sample surface. Since the sample with the whole epitaxial layer has a thickness only about 150 nm, the etching rate of conventional concentration Schimmel solution is too fast. Besides, the high Ge content material is more easily etched than Si. So greatly diluted Schimmel solution is used to reduce the etching rate, and SEM is used to observe even small pits appearing on the flat sample surface. Different etching time samples have been prepared and observed using SEM. There are pits emerging even with the least etching time. As the etching time increases, the pits' diameters grow and the number of pits changes little. When etching time exceeds 50 s, the number of pits greatly increases. The samples etched with

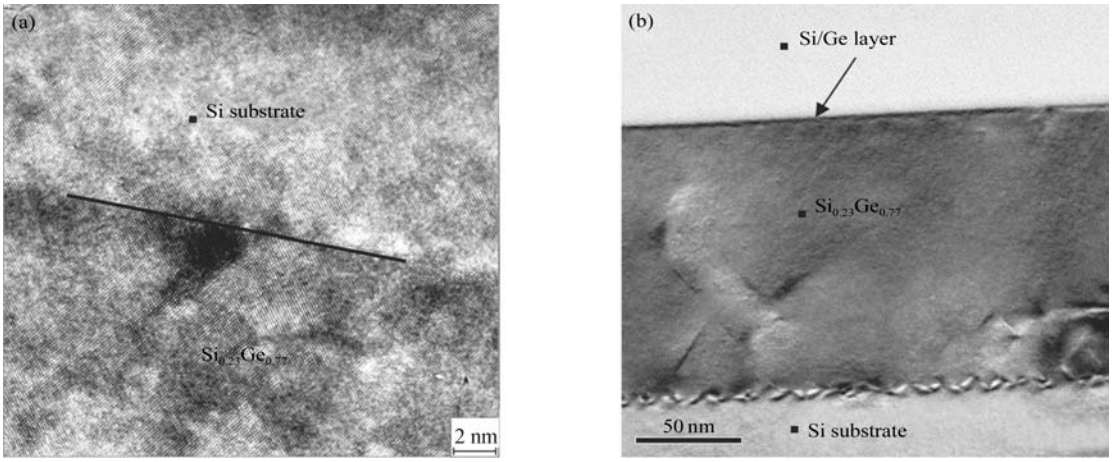

Fig. 5. (a) High resolution XTEM image of the SiGe/Si substrate interface; (b) XTEM image of the whole epitaxial layer including the Si cap/Ge/SiGe/Si substrate. Many dislocations nucleate at the SiGe/Si substrate interface and extend into the SiGe layer at an angle of 60° with the interface, but most of them are terminated in the SiGe layer by interacting with each other.

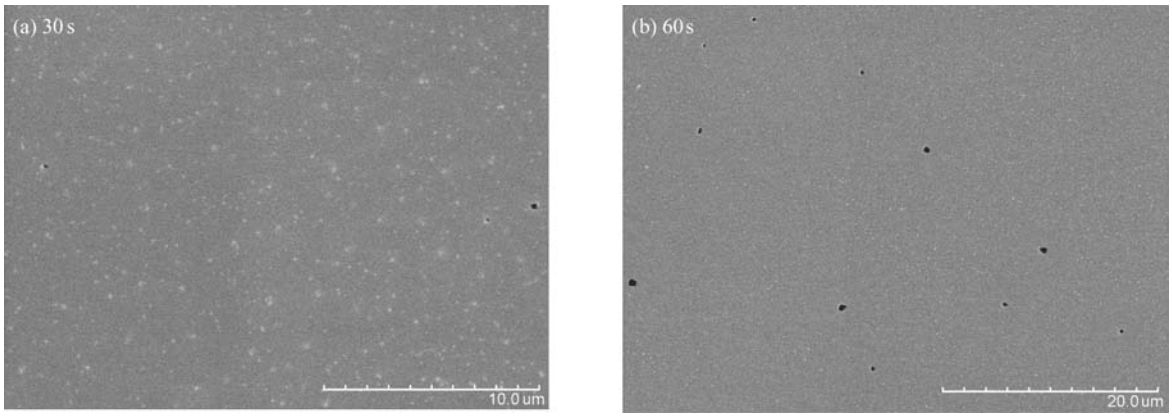

Fig. 6. Surface SEM images of the strained Ge sample etched by diluted Schimmel solution with different etching times: (a) 30 s; (b) 60 s. The black pits in the images represent the threading dislocations running through to the surface.

30 s and 60 s are used to estimate the threading dislocation density. Figures 6(a) and 6(b) are the surface SEM images of these two samples. The black pits are the threading dislocations running through to the surface. For the 30 s sample, the averaged pit density is about 2×10^4 cm^{-2}, and most of the pits' diameters are of the order of tens of nanometers. For the 60 s sample, the averaged pit density is about 6×10^5 cm^{-2}, and most of the pits' diameters are of the order of 100 nm. So, it is concluded that the threading dislocation density is $\sim 10^5$ cm^{-2}, which is considered to be low for such a thin epitaxial layer.

To sum up, a high quality thin SiGe virtual substrate was grown, with low threading dislocation density, low surface roughness, high Ge content, and fully relaxed epitaxial layer. Based on heteroepitaxy theories[20–22], the key factor to achieve this result is the layer-by-layer growth mechanism at low growth temperature. For high temperature CVD epitaxy of SiGe, three-dimensional-island growth dominates due to the high Ge surface diffusivity, and the growth rate at the dislocation defects is different from that in other areas. As the film thickness grows, the surface roughness increases rapidly and worsens the problem of threading dislocations, while dislocations piling up further roughen the surface[23, 24]. Consequently, a graded buffer technique is needed to reduce dislocation density and chemical mechanical polishing is used to reduce the surface roughness[11]. In this experiment, the growth temperature is chosen as low as possible to ensure that two-dimensional (2-D) layer-by-layer growth dominates. The Ge surface diffusivity is so low that the grown layer retains the surface profile of the Si substrate and the surface roughness does not deteriorate severely. Due to the initial high Ge content, the critical thickness of the SiGe layer is very small, and most of the threading dislocations nucleate at the interface of the SiGe/Si substrate. Meanwhile, the threading dislocations stretch in a straight line with an angle of 60° to the growth plane in the 2D growth mode[25, 26]. Most of the threading dislocations interact with each other and do not reach the surface. Only a very small portion runs through the epitaxial layer to the surface. Therefore, even with a thin epitaxial layer, a low surface roughness, low threading dislocation density and high Ge content are achieved simultaneously. The behavior of the dislocations during low temperature RPCVD growth should be further studied.

For the strained Ge layer growing on the SiGe virtual substrate using UHVCVD, the growth temperature is also the key to determining the layer morphology. Low growth temper-

ature ensures that the 2D layer-by-layer growth mode dominates to get a planar surface. Because the Ge content in the SiGe virtual substrate is as high as 77%, the critical thickness of the strained Ge layer is over 50 nm. Therefore, in the 9 nm thick strained Ge layer, there is no need to form new dislocations to relieve strains. A more elaborate description of Ge Growth using UHVCVD can be found in Refs. [21, 22].

4. Conclusions

A high quality compressively strained Ge film has been fabricated using low temperature RPCVD and UHVCVD. The thickness of the Si cap/strained Ge/SiGe virtual substrate epitaxial layers is less than 150 nm. A strained Ge film with a surface roughness of 0.4 nm and a threading dislocation density of $\sim 10^5$ cm^{-2} is achieved due to the low growth temperature that ensures the 2D layer-by-layer growth mode dominating during the epitaxial process.

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