Research and design of a novel current mode charge pump*

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Abstract: To meet the demands for a number of LEDs, a novel charge pump circuit with current mode control is proposed. Regulation is achieved by operating the current mirrors and the output current of the operational transconductance amplifier. In the steady state, the input current from power voltage retains constant, so reducing the noise induced on the input voltage source and improving the output voltage ripple. The charge pump small-signal model is used to describe the device's dynamic behavior and stability. Analytical predictions were verified by Hspice simulation and testing. Load driving is up to 800 mA with a power voltage of 3.6 V, and the output voltage ripple is less than 45 mV. The output response time is less than 8 μs, and the load current jumps from 400 to 800 mA.

Key words: charge pump; noise; output voltage ripple; operational transconductance amplifier
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1. Introduction

A charge pump DC/DC converter is a switching DC/DC converter power supply[1, 2] that uses switches to convert the input voltage to a regulated output voltage. However, one of the most common drawbacks of switching power supplies is the noise induced on the input voltage source due to fluctuations or variations in the current drawn by the converter power supply. Certain applications such as cellular telephones and precision instrumentation are sensitive to noise generated on the input voltage. Therefore, noise on the input voltage caused by the power supply must be filtered to prevent degraded electrical performance in other circuitry that is powered from the same input voltage source. However, it is necessary to use a costly filter with a large volume to filter the low frequency input noise, so application in portable devices is confined[3–5]. Therefore, methods of effective control of the power noise caused by variation of the current absorbed from the power has aroused the interest of charge pump DC/DC converter designers.

Recently, charge pumps have been used to constitute some system power supplies[6–8]. However, the reported work usually provides low driving current and cannot meet the demands of driving a number of LEDs[9]. In this paper, a novel charge pump circuit with current mode control is proposed, which uses current mirrors and inverters substituted for resistors and switches[10]. Not only are the transient response and the system stability improved, but the load ability of the charge pump is also enhanced. A current mirror amplifier with high gain and wide output swing is applied to compare the reference voltage with the output sampling voltage of the charge pump and generate the charging current of the charge pump. This charging current controlled by a feedback loop has nothing to do with the power supply, and remains constant in the charge pump boost process, so the input noise of the charge pump is reduced.

2. Structure of the current mode charge pump

As shown in Fig. 1, the current mode linear charge pump includes current mirrors, an operational transconductance amplifier (GM), a reference voltage ($V_{\rm REF}$), an oscillator (OSC), a feedback resistor (R_1, R_2), a flying capacitor (C_1) and two switches (S_1, S_2). The feedback loop regulating the output current $I_{\rm GM}$ of the operational transconductance amplifier makes the output current match the load current, and maintains the stability of the output voltage.

In Fig. 1(a), M5–M10 are the switches. M1 and M3, M2 and M4, M11 and M12 form respectively three current mirrors whose current gains are N. Clock signals CK1 and CK2 oscillate out of phase with a 50% duty cycle. Moreover, there is a very short time when they can be low simultaneously, called the dead time.

In Phase1 t_1–t_2 (the charging phase $t_{\rm A}$): CK1 is high and CK2 is low; switch S_1 turns on; switch S_2 turns off; the current mirror composed of M1 and M3 turns on, and that composed of M2 and M4 turns off; the current flows from $V_{\rm IN}$ charging up output capacitor $C_{\rm OUT}$ via C_1. The current $I_{\rm M1}$ flowing through M1 is $I_{\rm GM}$, and the current $I_{\rm M3}$ flowing through M3 is $NI_{\rm GM}$. The input current $I_{\rm IN}$ is determined by Eq. (1).

$$I_{\rm IN} = I_{\rm M1} + I_{\rm M3} = I_{\rm GM}\,(1 + N)\,. \tag{1}$$

In Phase2 t_3–t_4 (the charging phase $t_{\rm B}$): CK1 is low; CK2 is high; switch S_2 turns on; switch S_1 turns off; the current mirror composed of M1 and M3 turns off, and that composed of M2 and M4 turns on; the current is charging the flying capacitor C_1. The current $I_{\rm M2}$ flowing through M2 is $I_{\rm GM}$, and the current $I_{\rm M4}$ flowing through M4 is $NI_{\rm GM}$, $I_{\rm IN}$ is determined by

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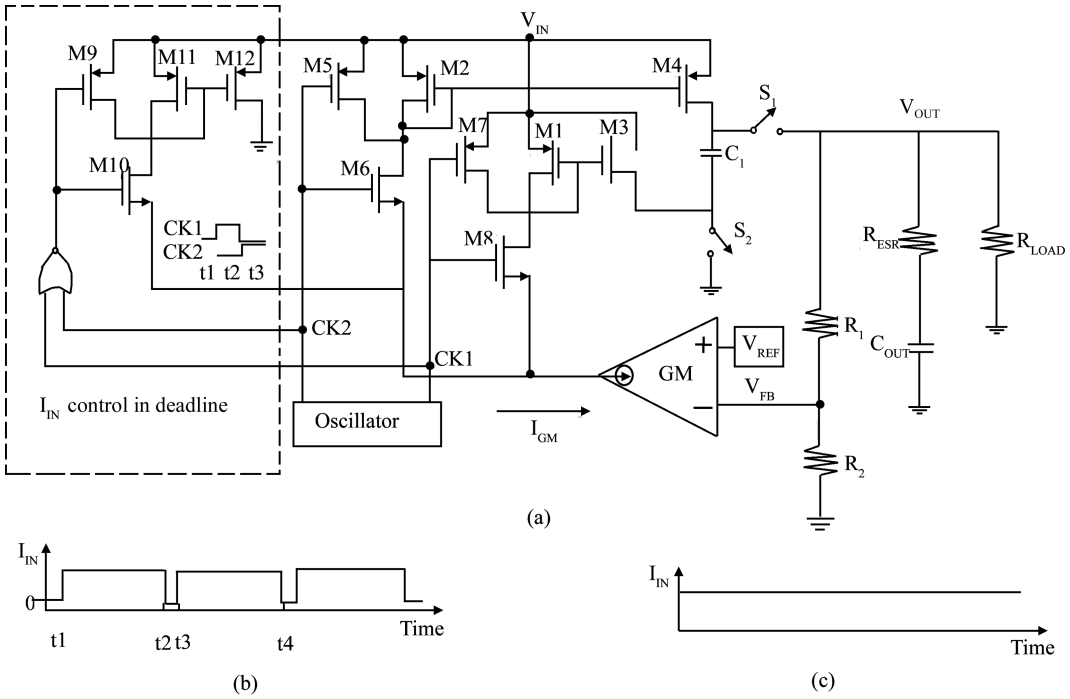

Fig. 1. Current mode charge pump: (a) Schematic; (b) Input current $I_{\rm IN}$ without the dotted circuit; (c) Input current $I_{\rm IN}$ with the dotted circuit.

Eq. (2).

$$I_{\rm IN} = I_{\rm M2} + I_{\rm M4} = I_{\rm GM}\,(1+N)\,. \tag{2}$$

In Phase3 t_2–t_3 (the dead time $t_{\rm C}$): the nor gate will not turn on until CK1 and CK2 are both low simultaneously, and switches S_1 and S_2 are open. At the same time, M10 turns on, and M9 turns off; then the current mirror composed of M11 and M12 begins to work, but the current mirrors composed of M1, M3, M2, M4 are unavailable. The current $I_{\rm M11}$ flowing through M11 is $I_{\rm GM}$. The current $I_{\rm M12}$ flowing through M12 is $NI_{\rm GM}$ The current $I_{\rm IN}$ in the dead time is determined by Eq. (3).

$$I_{\rm IN} = I_{\rm M11} + I_{\rm M12} = I_{\rm GM}\,(1+N)\,. \tag{3}$$

In the steady state, the voltage of the flying capacitor remains constant.

$$|\Delta Q_{\rm C}|\,({\rm phaseA}) = |\Delta Q_{\rm C}|\,({\rm phaseB}). \tag{4}$$

$\Delta Q_{\rm C}$ is the energy variation of capacitor C_1. When $t_{\rm A}$ is equal to $t_{\rm B}$, the average charging current of the capacitor C_1 is equal to the average discharging current.

Over one period T ($T = t_{\rm A} + t_{\rm B} + t_{\rm C}$), the load capacitor $C_{\rm OUT}$ can be charged only in stage $t_{\rm A}$ and in the rest phase (the stage $t_{\rm B}$ and $t_{\rm C}$), and $C_{\rm OUT}$ is discharged to the load. In a steady circuit system, the output voltage $V_{\rm OUT}$ is a steady value, and it requires the charging energy of the charge pump to be equal to the energy consumed by the load, so we can get the following equations.

$$I_{\rm LOAD}T = I_{\rm A}t_{\rm A}, \tag{5}$$

$$I_{\rm A} = I_{\rm B} = NI_{\rm GM} = \frac{I_{\rm LOAD}T}{t_{\rm A}} = \frac{I_{\rm LOAD}T}{t_{\rm B}}. \tag{6}$$

The dead time $t_{\rm C}$ is small, so $t_{\rm A}$ is equal to $t_{\rm B}$.

$$I_{\rm LOAD} = 2NI_{\rm GM}. \tag{7}$$

From Eq. (7), we can see that if the load current $I_{\rm LOAD}$ (the current driving LED in the steady stage) remains constant, $I_{\rm GM}$ will not change. From Eqs. (1) to (3), we know that in Phase1 and Phase2, the input currents $I_{\rm IN}$ are the same. $I_{\rm IN}$ is zero in Phase3 when CK1 and CK2 are both low. So, in the steady state, $I_{\rm IN}$ will change once between a constant and zero every half circle, as shown in Fig. 1(b). However, the dotted portion that is the control circuit with dead time $t_{\rm C}$ is designed to use the circuit loop to keep $I_{\rm IN}$ constant in Phase3, which reduces the current input noise greatly, as shown in Fig. 1(c).

If the loss of switches and the power supply is ignored, $V_{\rm OUT}$ is two times as great as $V_{\rm IN}$ when $t_{\rm A}$ is equal to $t_{\rm B}$. The output voltage noise will be reduced with the reduction of the input current noise.

2.1. Current mirror operational amplifier

The charge pump owns the capacitive load with high impedance. The operational amplifier with current mirror mode is applied, as shown in Fig. 2 (the bias circuit is neglected).

The output stage of the operational amplifier uses a fully differential fold-cascode structure and introduces common-mode negative feedback[11]. Its small-signal model can obtain the open loop gain of the differential input stage.

$$|A_{\rm O}| = g_{\rm m1}\left\{\left[\left(g_{\rm m7} + g_{\rm mb7}\right) r_{\rm o7}\left(r_{\rm o11}//r_{\rm o1}\right)\right]//r_{\rm o9}\right\}, \tag{8}$$

where $g_{\rm mb7} = \partial I_{\rm D7}/\partial V_{\rm BS7}$, $I_{\rm D7}$ is the drain current flowing M7; $V_{\rm BS7}$ is the substrate-source voltage of M7; $g_{\rm m1}$ and $g_{\rm m7}$ are respectively the transconductances of M1 and M7; $r_{\rm o5}$, $r_{\rm o7}$, $r_{\rm o9}$ and $r_{\rm o11}$ are respectively the output resistors of M5, M7, M9 and M11.

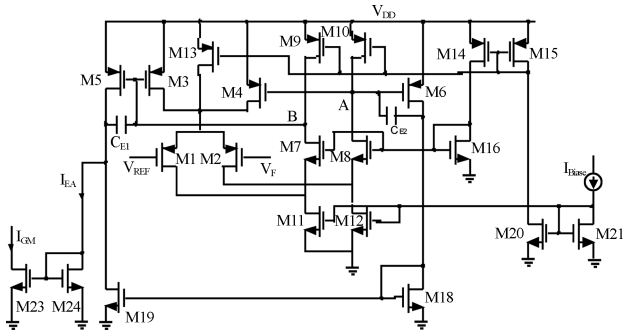

Fig. 2. Current mirror operational amplifier.

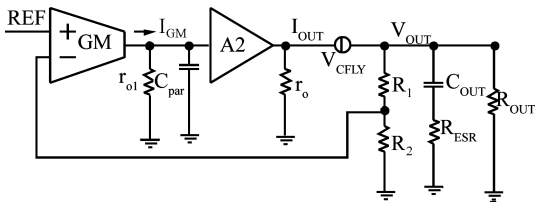

Fig. 3. Charge bump small-signal model.

The gain G_{m} of the current mirror mode amplifier is:

$$\begin{aligned} I_{\mathrm{EA}} &= I_{\mathrm{D5}} - I_{\mathrm{D6}} \\ &= g_{\mathrm{m5}}\left(V_{\mathrm{DD}} - V_{\mathrm{B}}\right) - g_{\mathrm{m6}}\left(V_{\mathrm{DD}} - V_{\mathrm{A}}\right) \\ &= g_{\mathrm{m5}}\left(V_{\mathrm{A}} - V_{\mathrm{B}}\right) \\ &= g_{\mathrm{m5}}\left|A_{\mathrm{O}}\right|\left(V_{\mathrm{REF}} - V_{\mathrm{F}}\right), \end{aligned} \tag{9}$$

where $g_{\mathrm{m5}} = g_{\mathrm{m6}}$. These are respectively the transconductances of M5 and M6; $\mathrm{I_{D5}}$ and I_{D62} are respectively drain currents flowing through M5 and M6; V_{A} and V_{B} are respectively the voltages of point A and point B in Fig. 2. V_{DD} is the power voltage.

$$\begin{aligned} \left|G_{\mathrm{m}}\right| &= \left|\frac{I_{\mathrm{EA}}}{v_{\mathrm{IN}}}\right| = g_{\mathrm{m5}}\left|A_0\right| \\ &= g_{\mathrm{m1}} g_{\mathrm{m5}}\left\{\left[\left(\mathrm{g_{m7}} + g_{\mathrm{mb7}}\right) r_{\mathrm{o7}}\left(r_{\mathrm{o11}} // r_{\mathrm{o5}}\right)\right] // r_{\mathrm{o9}}\right\}. \end{aligned} \tag{10}$$

The output impedance of the fold-cascode input stage is so big that the circuit gain can reach a high level; the structure of the output stage is simple, and we can get an output swing $V_{\mathrm{DD}} - 2V_{\mathrm{DS}}$. So compared with a common current mirror mode amplifier, there is a wider output swing.

2.2. Small-signal model

The charge pump small-signal model is shown in Fig. 3. The model includes the transconductance operational amplifier GM and the current mirror gain A_2, the sum of operational amplifier output impedance and the input impedance of the next stage r_{o1}, a parasitic capacitor C_{par}, the output impedance of the current mirror r_{o}, as well as external components like the feedback divider R_1 and R_2, C_{out} and R_{out}. The voltage V_{CFLY} represents the fly capacitor C_1[10]. When the transition frequency is far less then the system switch frequency, the capacitor is equivalent to the voltage source V_{CFLY}, and the model is effective. V_{CFLY} is:

$$V_{\mathrm{CFLY}} = V_{\mathrm{IN}} - V_{\mathrm{LOSSES}}. \tag{11}$$

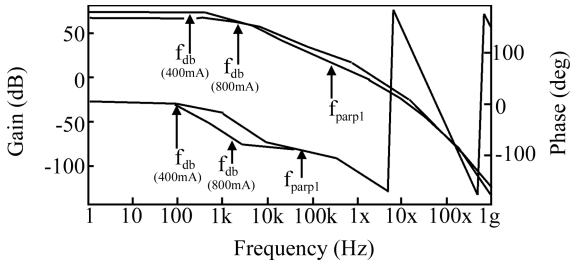

Fig. 4. Bode plot of small-signal model.

V_{LOSSES} is the loss of switches and current mirrors in the discharging stage. In the model, there is an assumption that the impedance of the fly capacitor C_1 is far less then the output impedance of the current mirrors, so the system output impedance does not include the impedance of the fly capacitor.

Based on the small-signal model, the main pole of the open loop f_{dp} is:

$$f_{\mathrm{dp}} = \frac{1}{2\pi C_{\mathrm{out}}\left(r_o // R_{\mathrm{out}}\right)}. \tag{12}$$

In order to drive a large current, the gate of the current mirror A_2 will generate a big parasitic capacitor C_{G}. The gate parasitic capacitor C_{G} and resistor R_{G} will generate a parasitic pole f_{parp1}:

$$f_{\mathrm{parp1}} = \frac{1}{2\pi C_{\mathrm{G}} R_{\mathrm{G}}}, \tag{13}$$

$$R_{\mathrm{G}} = \frac{1}{g_{\mathrm{m1}}} // r_{\mathrm{o1}} // r_{\mathrm{o3}}. \tag{14}$$

The output stage of the transconductance operational amplifier generates the second parasitic pole f_{parp2}:

$$f_{\mathrm{parp2}} = \frac{1}{2\pi C_{\mathrm{par}} r_{\mathrm{o1}}}. \tag{15}$$

The dc gain of the error amplifier is:

$$A_1 = g_{\mathrm{m1}} r_{\mathrm{o1}}. \tag{16}$$

The open loop dc gain A of the whole system is:

$$A = A_1 A_2 (r_{\mathrm{o}} // R_{\mathrm{L}}) \frac{R_{\mathrm{fl}}}{R_1 + R_2}. \tag{17}$$

The zero point is:

$$f_{\mathrm{Z}} = \frac{1}{2\pi C_{\mathrm{OUT}} R_{\mathrm{ESR}}}. \tag{18}$$

Figure 4 is a Bode and phase graph of the open loop gain when the load is 800 and 400 mA.

From Table 1, we can see that the main pole varies with variation of the load.

3. Simulation and test results

Based on the Hynix 0.6 μm CMOS process, the circuit was simulated using Hspice. Figure 5 shows the simulated transient response when the load current jumps from 400 to 800 mA. The output response time is less than 8 μs.

Figure 6 is a layout photo of the current mode charge pump with the constant current driving LEDs. The white part

Table 1. Results from Bode plot.

Parameter	Load current	
	400 mA	800 mA
Gain (dB)	74.5	67.1
Main pole f_{dp} (Hz)	665	2460
First parasitic pole f_{parp1} (MHz)	1.23	1.23
Second parasitic pole f_{parp2} (MHz)	10	10
Zero point (MHz)	27.1	27.1
Bandwidth (MHz)	1.75	2.42

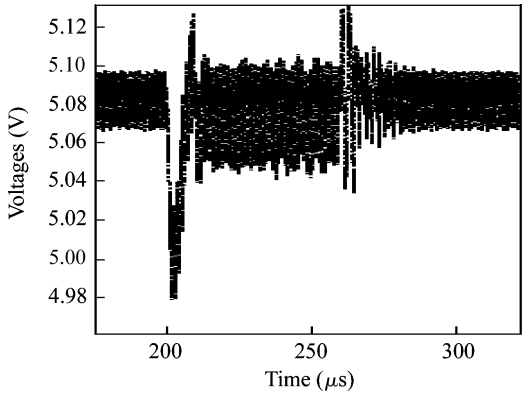

Fig. 5. Load transient response.

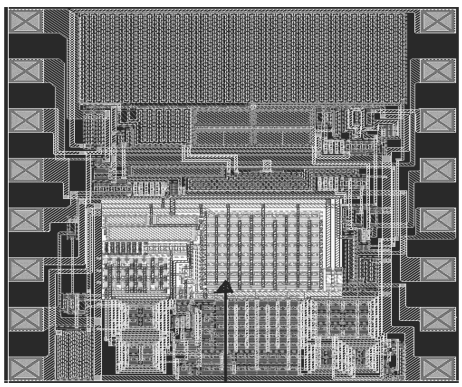

Fig. 6. Layout of current mode charge pump with constant current driving circuit.

is the current mode charge pump circuit layout of Fig. 1, and the remaining part is the layout of the constant current driving LED circuit.

Figure 7 shows that the output ripple voltage is 43.3 mV with a frequency of 900 kHz when the load current is 800 mA and the double output voltage is 5.01 V. The rise and fall times of the output voltage are equal to each other since the pumping operation is performed on every clock cycle and the clock duty cycle is 50%.

The regulated charge pump performances are summarized and compared to other recently reported designs in Table 2. According to Table 2, the proposed circuit may meet the demands of driving a number of LEDs.

4. Conclusion

A new regulated charge pump with low output ripple voltage and high load current drive capability with enhanced tolerance of output voltage variation is proposed. This proposed charge pump uses a current mirror, which replaces the conventional method of regulating the output voltage by controlling the turn-on resistor in the saturation region of the MOS transistor. In the steady stage, the input current is equal in every phase, so the power input noise is reduced. The load driving is up to 800 mA. System stability analysis is completed by small-signal analysis, which proves that a charge pump with an excellent load transient response is available without an extra compensation circuit.

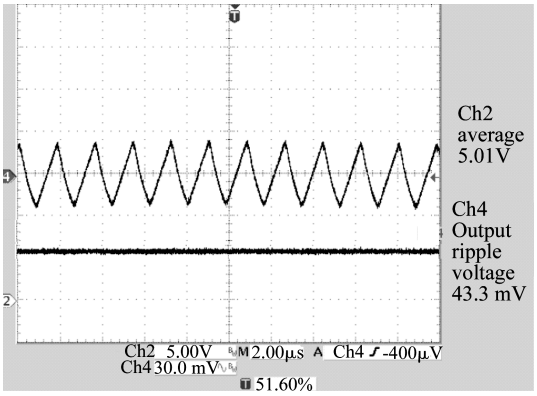

Fig. 7. Measurement results of output voltage.

Table 2. Performance summary and comparison.

Parameter	Ref. [6]	Ref. [9]	This work
Power supply (V)	3.3	10–15	3.2–4.4
Pumping frequency (kHz)	400–600	1800	900
Output voltage (V)	4.5–5	16–36	5.01
Ripple voltage (mV)	33.8	56	43.3
Load capacitor (μF)	2	4.7	4.7
Driving current (mA)	30	300	800

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