Research into charge pumping method technique for hot-carrier degradation measurement of LDMOS*

Qian Qinsong(钱钦松)†, Liu Siyang(刘斯扬), Sun Weifeng(孙伟锋), and Shi Longxing(时龙兴)

(National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China)

Abstract: A measuring technique based on the CP (charge pumping) method for hot-carrier degradation measurement of high voltage N-LDMOS is researched in depth. The impact of the special configuration on the CP spectrum and the gate voltage pulse frequency range which is suitable for high voltage N-LDMOS in CP measurements is investigated in detail. At the same time, the impacts of different reverse voltage applied on the source and drain electrodes and of the gate pulse shape on the CP curve change in N-LDMOS are also proposed and analyzed. The conclusions give guidance on measuring the density of interface states with experimental instructions and offer theoretic instructions for analyzing CP curves in high voltage N-LDMOS more accurately.

Key words: CP measurements; N-LDMOS; hot-carrier; interface states
DOI: 10.1088/1674-4926/30/10/104005 **EEACC:** 2500

1. Introduction

Among the large variety of semiconductor devices addressed to power applications, lateral double diffused MOS (LDMOS) transistors have been widely used as power switches in the monolithic integration arena. Nevertheless, LDMOS devices usually work under high temperature, high voltage and high power conditions; consequently, they suffer considerably from hot-carrier effects (HCE), and hot-carrier degradation of LDMOS devices has become an important reliability issue in power integrated circuits[1−4]. In order to improve the understanding of the physical mechanism resulting in hot-carrier degradation, there is a great need for experimental results of variations in Si–SiO_2 interface state density and distribution under the gate of the device.

CP (charge pumping) technology is currently the most reliable and effective method in numerous technologies for measuring the degradation caused by hot-carrier effects. Groeseneken *et al.* successfully gave a charge pumping current expression for MOS devices, which can reflect the average Si–SiO_2 interface state density indirectly[5]. Zhang *et al.* introduced three measuring modes for the CP technique[6], which will be illustrated in the following section. Chen *et al.* presented a new CP method to measure lateral profiling of oxide charge and interface traps near MOSFET junctions[7]. It is obvious that the CP method has been used in a great deal of work on hot-carrier effect investigation in MOS devices; nevertheless, detailed research into the application of the CP method in high voltage LDMOS devices has not been reported.

In this paper, the differences between the CP curves of N-LDMOS and LV-MOS and the special configuration influences on the CP spectrum are discussed. After that, the gate voltage pulse frequency range which is suitable for high voltage N-LDMOS in CP measurements is presented, and the influence of gate pulse shape on CP spectra is also discussed. Finally, the relationships between the CP measuring results of N-LDMOS and the reverse voltage stresses on source and drain are revealed. These conclusions give guidance on measuring the density of interface states with experimental instructions and offer theoretic instructions for analyzing CP curves in high voltage N-LDMOS more precisely.

2. Device and measurement description

A cross-section of the device which is used to undertake CP measurement is illustrated in Fig. 1. Two kinds of devices (types A and B) with different configurations are adopted in the experiments. The main geometrical and technological parameters are listed in Table 1.

In this paper, related measurements are operated by a Keithley 4200. Figure 2 shows the experimental facilities of CP measurement for an investigated N-LDMOS in this paper, and three measuring modes for the CP technique can be seen in Fig. 3. There are no obvious differences between the measured results for the three measuring modes. Mode B is selected in all of the following experiments.

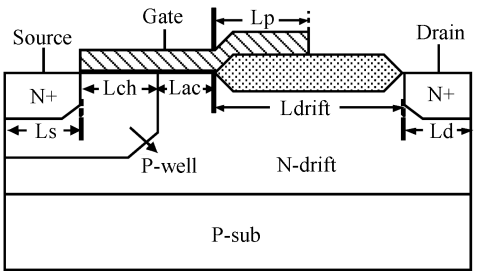

Fig. 1. Schematic cross-section and components of the devices studied in this paper.

* Project supported by the Jiangsu Provincial Natural Science Foundation (No. BK2008287).
† Corresponding author. Email: qianqinsong@seu.edu.cn
Received 13 April 2009, revised manuscript received 15 May 2009

Table 1. Main geometrical parameters of devices A and B.

Parameter	Symbol	Value	
		Type A	Type B
Channel length (μm)	L_{ch}	3	1.5
Accumulation region length (μm)	L_{ac}	1.5	0.5
Effective drift region length (μm)	L_{drift}	8	8
Poly overlap field oxide (μm)	L_p	4	4
Drain and source length (μm)	L_d, L_s	3	3

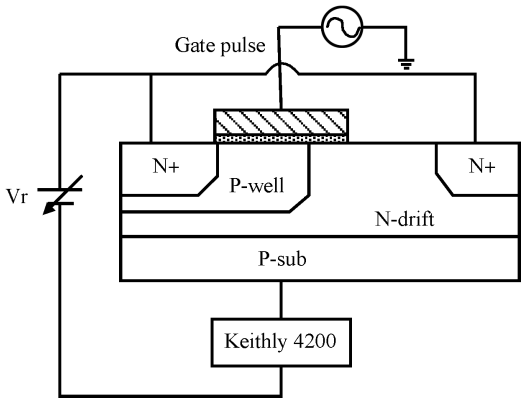

Fig. 2. Experimental facilities of CP measurement for an N-LDMOS device.

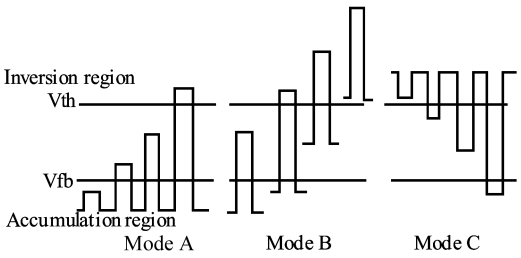

Fig. 3. Schematic diagram of three measuring modes for the CP technique. Mode A: keeping the pulse base level in accumulation and pulsing the top into inversion while increasing the voltage amplitude. Mode B: varying the pulse base level from accumulation to inversion while keeping the amplitude of the pulse constant. Mode C: keeping the pulse base level in inversion and pulsing the top into accumulation while increasing the voltage amplitude.

3. Measurements and discussion

3.1. CP measurement comparisons for high voltage N-LDMOS and LV-NMOS (device A is selected to enhance the impact on the configuration of N-LDMOS)

Figure 4 displays the CP curves under mode B before and after a stress time of 10^4 s at V_{gs} = –15 V and V_{ds} = 0 V for a LV-NMOS and a high voltage N-LDMOS respectively. As clearly shown: (1) The CP curve shape of the unstressed high voltage N-LDMOS is basically the same as the one for the unstressed NMOS, but the peak values of CP current and the horizontal positions of the curves are different from each other. The difference of the peak CP current is due to the inequality of the Si–SiO_2 interface state quantity and the difference of V_{th} and V_{fb} in the two devices is responsible for the shift

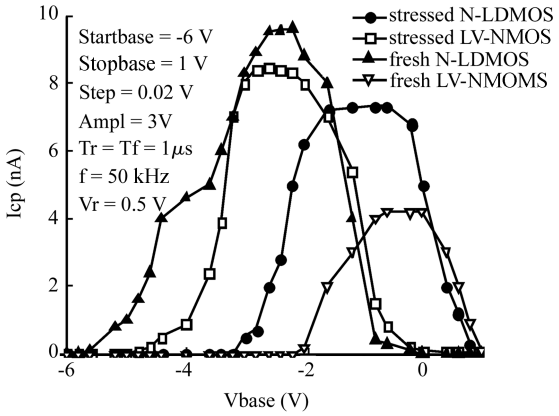

Fig. 4. Measured CP spectra for a LV-NMOS and a high voltage N-LDMOS.

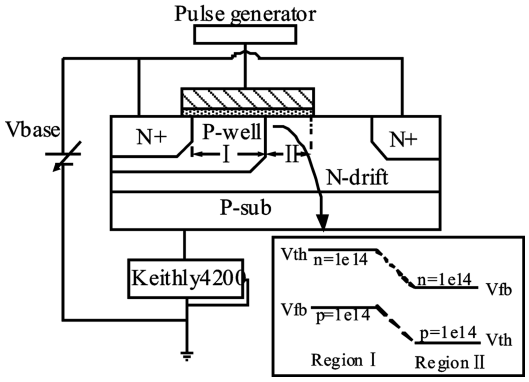

Fig. 5. Configuration difference illustration of N-LDMOS and LV-nMOS.

of the horizontal points of the curves. (2) The shapes of unstressed and stressed NMOS are essentially identical; however, the peak values of CP current are different, but the reasons for this are discrepant. It can be concluded that new interface states have been generated during the stressed process, which will contribute to the total CP current, increasing the CP current. Furthermore, positive oxide charge may occur in the accumulation at that moment, thereby making V_{th} and V_{fb} shift towards the negative direction of the x axis; consequently, the CP curve of the stressed NMOS will shift in the same direction too. (3) It is very obvious that the curve of the stressed N-LDMOS is different from the other three curves, having two steps. However, the reasons for the changes of the peak CP current and the curve's horizontal position in the stressed high voltage N-LDMOS are the same as in (2). The cause for the appearance of two steps in the curve of the stressed N-LDMOS will be explained in the following paragraphs.

Hot-carrier degradation is not very serious in the unstressed N-LDMOS, so the Si–SiO_2 interface state quantity under the gate of the device is finite, which limits the influence on the CP curve from the N-LDMOS configuration; the CP curve shape of the unstressed N-LDMOS is therefore basically similar to that of the unstressed LV-NMOS. However, once stressed, there are so many interface states generated under the gate that the influence from the configuration of N-LDMOS cannot be ignored. As shown in Fig. 5, the gate region

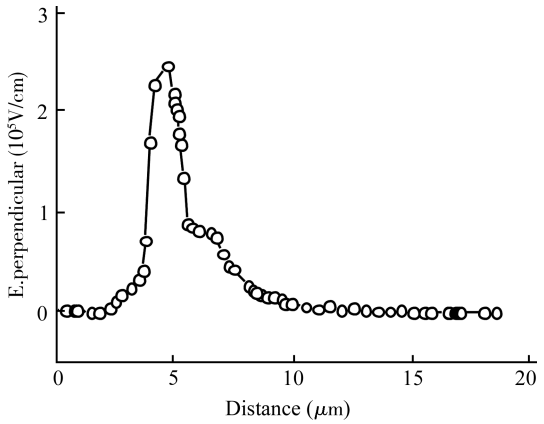

Fig. 6. Perpendicular electric field along the Si–SiO_2 interface of the studied N-LDMOS devices at V_{gs} = –15 V and V_{ds} = 0 V.

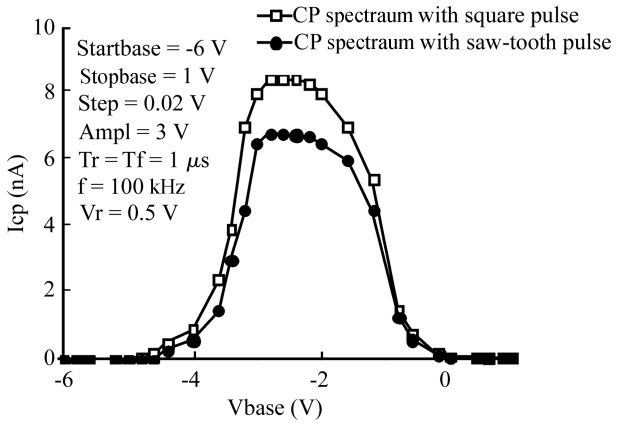

Fig. 7. CP measurement results with different pulse shapes for the same device.

in N-LDMOS consists of two parts: one is the P channel region (I), and the other is the N accumulation region (II), which are both pumped in CP measurement. Figure 5 also shows that V_{th}, V_{fb} in the two regions are different, and region I begins to invert at electron concentration $n = 10^{14}$ cm^{-3} but accumulates at hole concentration $p = 10^{14}$ cm^{-3}, while the region II begins to invert at hole concentration $p = 10^{14}$ cm^{-3} but accumulates at electron concentration $n = 10^{14}$ cm^{-3}, as defined in the figure.

If the measurement is operated under mode B, when the top of the gate pulse reaches V_{th} of region II, CP current begins to increase, but the current is only contributed by region II. However, if the pulse top exceeds V_{fb} of region I, both regions will be pumped, and thus the left step appears. When the pulse top arrives at V_{th} of region I but the pulse base does not exceed V_{th} of region II, the CP current begins to saturate. If the pulse base exceeds V_{th} of region II, the CP current will decline, and the current from region II becomes smaller and smaller. Finally, the CP current will be taken on by region I, and the right step appears[8].

It is very interesting that, according to the report of Cheng *et al.*[9], the CP current for N-LDMOS is contributed by three regions, with the field oxide region also included. It seems likely that the CP curve for the stressed N-LDMOS in our experiment should have three steps, but only two steps can be investigated in this paper. The reason for this can be explained as follows: from the CP curve of fresh N-LDMOS in Fig. 4, it can be concluded that the interface state quantity in the accumulation and field oxide regions is very small for the investigated fresh N-LDMOS due to the disappearance of the steps. However, the simulation results in Figure 6 show the perpendicular electric field along the Si–SiO_2 interface of the stressed N-LDMOS device: it is obvious that the perpendicular electric field in the field oxide region (from 7.5 to 11.5 μm) is much smaller than the one in the channel and accumulation regions, which implies that impact ionization generation along the Si–SiO_2 interface is mainly located in the channel and accumulation regions during stress; this is in agreement with the result from the report of Cheng *et al.*[9]. That is to say that no new interface states and positive oxide charge will be generated in the field oxide region during the whole stress; consequently, the interface state quantity in the field oxide region is always very small before or after stress, and the third step cannot be seen in our experiment.

3.2. Influence of gate pulse shape on CP spectra of LDMOS (device A is selected)

Figure 7 shows CP measurement results with different pulse shapes for the same device. From Fig. 7, a strong dependence of the CP current on the shape of the applied gate pulse is observed, which is illustrated under mode B, and the tested device is unstressed. It is obvious that the peak value of CP current tested with square pulses is greater than the one with saw-tooth pulses, which implies gate stress with square pulses is recommended in CP measurement of N-LDMOS. This phenomenon can be explained by a geometric component, consisting of free minority carriers which do not have enough time to flow back to source and drain, recombining with majority carriers. Therefore, they will also contribute to the CP current. It is believed that when saw-tooth pulses are used, this component could be eliminated because of the longer time available for the mobile carriers to reach source and drain when driving the surface back towards accumulation state.

3.3. Determination of pulse frequency range for high voltage N-LDMOS (device B is selected)

In Fig. 8, the gate pulse frequency dependence of the peak value of CP current is shown; it is obvious that the peak value of CP current is not always proportional to the gate voltage pulse frequency. Hence, the range of gate voltage pulse frequency which is applied in CP measurement for high voltage N-LDMOS needs to be selected correctly in order to get an accurate result. From the figure, it can be concluded that the proper pulse frequency range for N-LDMOS is 10^4–10^7 Hz, in which the result is proportional to the gate voltage pulse frequency. If the frequency is less than 10^4 Hz or greater than 10^7 Hz, the result always fluctuates, which will influence the accuracy of CP measurement. The reasons for this are explained as follows: (1) When the frequency is less than 10^4 Hz, the

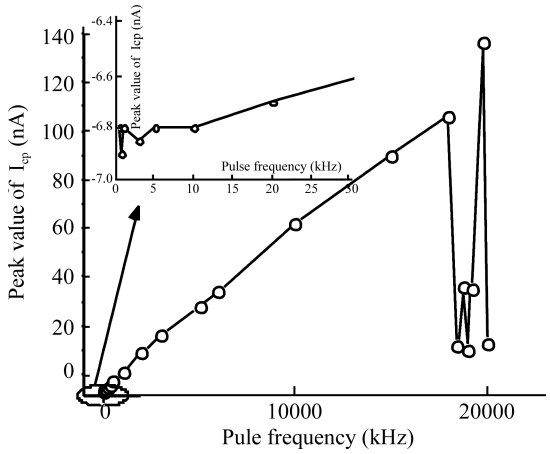

Fig. 8. Peak value of CP current as a function of stress frequency.

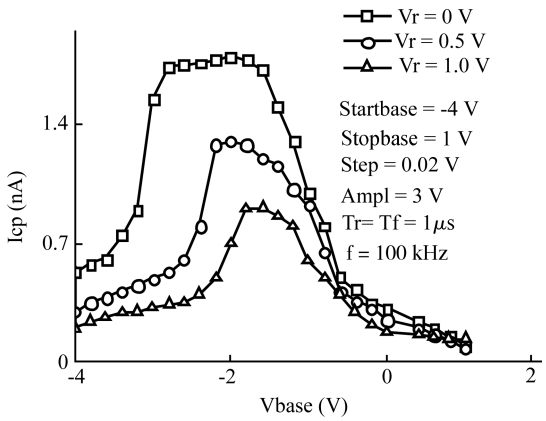

Fig. 9. Comparison of CP curves with different reverse voltages (V_r = 0, 0.5, 1.0 V) for N-LDMOS.

effect of $1/f$ noise must be considered, and the contribution to CP current by the slow interface state cannot be ignored. (2) When the frequency exceeds 10^7 Hz, few inversion and accumulation charges can form during the sweep, and the geometric component has to be taken into consideration; at the same time, high frequency noise can also not be overlooked.

3.4. Relationship between the CP curve and the increasing reverse voltage for N-LDMOS (device B is selected)

In order to research the Si–SiO_2 interface state distribution along the channel, reverse voltages are often stressed on source and drain to bring depletion regions on both sides of the channel during CP measurement, which could shield the partial channel. In Fig. 9 the CP curves of the unstressed high voltage NLDMOS are plotted at different reverse voltages (V_r = 0, 0.5, 1.0 V), while the gate pulses are kept at the same changing conditions. Due to the length of accumulation region (L_{ac} = 0.5 μm), which is much shorter than the channel region (L_{ch} = 1.5 μm), and the fresh condition of the device, the influence from the accumulation region can be neglected. As clearly shown: (1) The CP current decreases as the reverse voltage increases. (2) The V_{base} value where CP current just reaches saturation shifts towards to the positive direction of the x axis when the reverse voltage increases, while the V_{base} value where CP current just exits saturation basically remains consistent. (3) The greater the reverse voltage at source and drain is, the larger the CP current will be at high V_{base}. According to Guido Groeseneken's research[5], the emission time supported for the electrons or holes which are trapped in interface states is given by Eq. (1).

$$t_{em,e/h} = \frac{|V_{fb} - V_{th}|}{|\Delta V_G|} t_{f,r}, \quad (1)$$

where $t_{em,e/h}$ is the emission time supported for the electrons or holes, V_{th}, V_{fb} are the threshold and flatband voltages, respectively, ΔV_G is the amplitude of the gate pulse, and t_r and t_f are the rise and fall times of the gate pulse.

When the reverse voltage increases, $|V_{fb} - V_{th}|$ will also increase due to the body effect, resulting in increase of the emission time supported for the trapped electrons or holes, which means that more electrons or holes can escape from the traps. Consequently, the quantity of recombined electrons or holes decreases, and then CP current decreases. Similarly, because of the increase of the threshold voltage V_{th}, the CP current needs a greater V_{base} to reach saturation; however, the flatband voltage V_{fb} is kept constant when the reverse voltage increases, so the V_{base} value where CP current just exits saturation basically remains consistent. At the same time, as a result of the increase of V_{th}, the CP current needs a greater V_{base} to return to zero; therefore, the greater the reverse voltage is, the larger the CP current will be at high V_{base}, as can be observed in Fig. 9.

4. Conclusions

A measuring technique based on the CP method for high voltage N-LDMOS is developed in this work. The following items are investigated in detail: (1) The influences of the special configuration of high voltage N-LDMOS on CP measuring results, and the reason for the appearance of two steps in the CP curve of stressed N-LDMOS. (2) The influence of gate pulse shape on CP spectra and gate stress with square pulses is recommended in CP measurement of N-LDMOS. (3) The gate voltage pulse frequency range which is suitable for high voltage N-LDMOS in CP measurement is presented and our result is that the range needs to be set between 10^4 and 10^7 Hz. (4) The relationships between the CP measuring results of N-LDMOS and the reverse voltages applied at source and drain are revealed and explained.

These studies and conclusions not only give guidance on measuring the density of interface states with experimental instructions, but also offer theoretic instructions for analyzing CP curves in high voltage N-LDMOS more accurately.

References

[1] Chen J F, Tian K S, Chen S Y, et al. On-Resistance degradation induced by hot-carrier injection in LDMOS transistors with STI in the drift region. IEEE Electron Device Lett, 2008, 29(9): 1071

[2] Su R Y, Chiang P Y, Gong J, et al. Investigation on the ini-

tial hot-carrier injection in P-LDMOS transistors with shallow trench isolation structure. IEEE Trans Electron Devices, 2008, 55(12): 3569

[3] Cortes I, Fernández-Martínez P, Flores D, et al. Static and dynamic electrical performances of STI thin-SOI power LDMOS transistors. Semicond Sci Technol, 2008: 493

[4] Brisbin D, Strachan A, Chaparala P. Optimizing the hot carrier reliability of N-LDMOS transistor arrays. Microelectron Reliab, 2005: 1021

[5] Groeseneken G, Maes H E, Beltran N, et al. A reliable approach to charge pumping measurements in MOS transistors. IEEE Trans Electron Devices, 1984, 31(1): 42

[6] Zhang Weidong, Tang Yusheng, Hao Yue. On measurements of hot-carrier effect in MOSFET. Journal of Xidian University, 1997, 24(4): 509

[7] Chen W, Balasiriski A, Ma T P. Lateral profiling of oxide charge and interface traps near MOSFET junctions. IEEE Trans Electron Devices, 1993, 46(1): 187

[8] Moens P, Van den Bosch G, Groeseneken G. Hot-carrier degradation phenomena in lateral and vertical DMOS transistors. IEEE Trans Electron Devices, 2004, 51(4): 623

[9] Cheng C C, Lin J F, Hsieh T H, et al. Physics and characterization of various hot-carrier degradation modes in LDMOS by using a three-region charge-pumping technique. IEEE Trans Device Mater Reliab, 2006, 6(3): 358