An area-saving dual-path loop filter for low-voltage integrated phase-locked loops

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Abstract: This paper proposes an area-saving dual-path loop filter (LPF) for low-voltage integrated phase-locked loops (PLLs). With this LPF, output current of the lowpass-path charge-pump (CP) is B times ($B > 1$) as great as that of the integration-path CP. By adding voltages across these two paths, the zero-capacitance is magnified B times equivalently. As a result, the chip size is greatly reduced. Based on this LPF, a 1.2 V 3.5 GHz-band PLL is fabricated in SMIC 0.18 μm RFCMOS technology. Its zero-capacitance is only 1/30 of that in conventional second-order LPFs. Measured data show that, at a frequency of 3.20 GHz, phase noise is –120.2 dBc/Hz at 1 MHz offset, reference spur is –72 dBc, and power is 24 mW.

Key words: area-saving; dual-path loop filter; charge-pump; phase-locked loop
DOI: 10.1088/1674-4926/30/10/105011 **EEACC:** 2500

1. Introduction

With the increase of CMOS integrated circuit (IC) complexity, chip sizes are becoming larger, and thus costs are becoming higher. As a result, the whole IC industry has to study methods of greatly improving IC integration. Basically, there are two ways to solve this: (1) To reduce the sizes of active devices or improve density of passive components[1]. However, this suffers from technological and cost restrictions. For example, the density of the metal–insulator–metal (MIM) capacitor is less than several fF/μm^2. It is unimaginable to realize an nF-level MIM capacitor for IC designers. (2) To adopt new circuits or topologies instead. For example, compared to a superheterodyne receiver, a zero-IF receiver does not need any off-chip SAW-filters[2].

Phase-locked loops (PLL) are important modules in RF transceivers. As a high-order negative feedback system, the PLL requires a nonzero zero to provide a proper phase margin to maintain its stabilization. As a rule of thumb, this nonzero zero is usually a fraction of its loop bandwidth. Considering this zero just comes from the loop filter (LPF), such a small zero means that a huge RC-product is required. Moreover, larger resistance means more thermal noise, which will degrade the PLL's in-band phase noise. So, large zero-capacitances are inevitably required for PLLs. In conventional methods, zero-capacitances are usually realized by off-chip capacitors.

In this paper, an area-saving dual-path LPF is proposed. It magnifies its zero-capacitance B times ($B > 1$) equivalently without any change of technology. Compared to LPFs in published papers, this LPF is the simplest. Finally, a 3.5 GHz-band low-voltage PLL based on this LPF is designed and verified.

2. Dual-path loop filter

2.1. Theory of dual-path LPF

In a PLL, the LPF not only converts the charge-pump (CP) output current (I_{cp}) into VCO control voltage (V_c), but also provides zeros and poles for the PLL loop. As shown in Fig. 1, the conventional second-order passive LPF can be expressed as

$$\frac{V_c(s)}{I_{cp}(s)} = \frac{1}{sC_2 + \dfrac{1}{R_1 + 1/sC_1}} = \frac{1 + sR_1C_1}{s(C_1 + C_2)\left(1 + \dfrac{sR_1C_1C_2}{C_1 + C_2}\right)}. \tag{1}$$

It is clear that the nonzero zero and pole are $1/R_1C_1$, $(C_1 + C_2)/R_1C_1C_2$ respectively. To achieve a phase margin around 60°, the LPF parameters can be calculated from the PLL's loop bandwidth (ω_c) as[3]

$$\omega_z = 1/R_1C_1 \approx \omega_c/4, \tag{2}$$

$$\omega_p = (C_1 + C_2)/R_1C_1C_2 \approx 6\omega_c. \tag{3}$$

Taking a 25 kHz-ω_c PLL as an example, when R_1 is

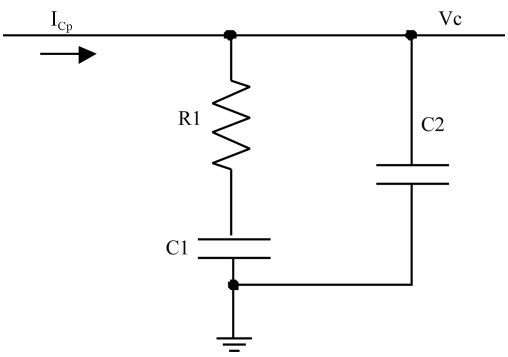

Fig. 1. Conventional second-order passive LPF.

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Received 13 April 2009, revised manuscript received 18 May 2009

Table 1. Comparison of the dual-path LPFs mentioned in Fig. 3.

No.	Reference generator	Output of the lowpass-path CP	Output of the integration-path CP	Input of the OPA	Voltage adder
a	Simple	Large swing	Constant	Constant	Yes
b	Complex	Large swing @ unlocked	Large swing @ unlocked	Large swing @ unlocked	None
		Constant @ locked	Constant @ locked	Constant @ locked	None
c	None	Large swing	Large swing	Large swing	None
d	Simple	Constant	Large swing	Constant	None

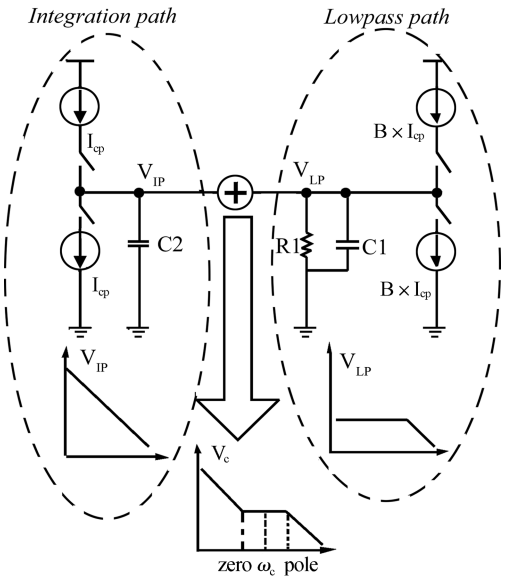

Fig. 2. Theory of dual-path LPF.

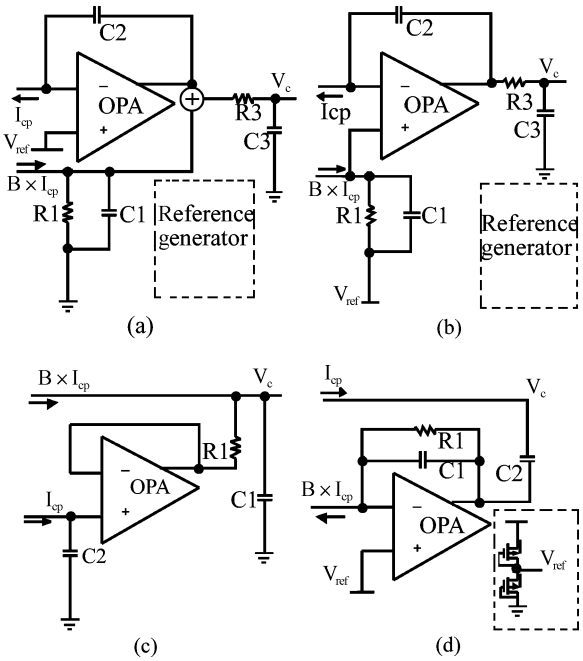

Fig. 3. (a), (b), (c) Published dual-path LPFs; (d) Proposed dual-path LPF.

33 kΩ, C_1 and C_2 will be 772 and 33.6 pF respectively. In SMIC 0.18 μm CMOS technology, the density of MIM-capacitors is only 0.971 fF/μm^2. Thus, C_1 will occupy an area of 892 × 892 μm^2 at least. Moreover, according to the design rule, a large MIM-capacitor should be replaced by a group of small separate MIM-capacitors. As a result, C_1 will occupy an area over 1000 × 1000 μm^2. Obviously, this is unendurable for any IC designer. Maybe MOS-capacitors could substitute for MIM-capacitors. Unfortunately, they are so voltage-sensitive that the LPF's AC characteristics will be badly affected.

The theory of dual-path LPF is a good solution to LPF's huge zero-capacitance, as shown in Fig. 2[4]. In a dual-path LPF, both an integration path and a lowpass path are contained. Because output current of the lowpass-path CP is B times ($B > 1$) as great as that of the integration-path CP, by adding voltages across these two paths, the zero-capacitance can be magnified B times equivalently:

$$\frac{V_c(s)}{I_{cp}(s)} = \frac{1}{sC_2} + \frac{B}{sC_1 + 1/R_1} = \frac{1 + sR_1(C_1 + BC_2)}{sC_2(1 + sR_1C_1)}. \quad (4)$$

It is clear that the nonzero zero and pole are $1/[R_1(C_1 + BC_2)]$, $1/R_1C_1$ respectively. When B is 30, taking the same PLL as above as an example, C_1 and C_2 will be 32.2 and 24.7 pF respectively. Obviously, C_1 and C_2 are not problems to the integrated PLL any longer.

2.2. Design of dual-path LPF

In a PLL, the LPF works together with CP seamlessly, so LPF and CP should be taken into consideration as a whole. Generally speaking, under a low supply voltage, a CP's complexity will increase with its output swing, and an OPA's complexity will increase with its input range. For the purpose of simplifying the design, it is best to avoid rail-to-rail output-swing CP and rail-to-rail input-range OPA. Figure 3 shows the schematics of published and proposed dual-path LPFs, and Table 1 shows a comparison between the LPFs mentioned in Fig. 3, which indicates that the proposed LPF is the simplest for IC designers.

(1) For Fig. 3(a), both an operational amplifier (OPA) and a voltage adder are needed. Such two active blocks will undoubtedly increase noise, power and area[5].

(2) For Fig. 3(b), its reference generator's output impedance should be as small as possible to keep the LPF's AC characteristics[6]. A voltage divider network with a unity-gain buffer can meet this requirement, but its noise, power and complexity will increase. Moreover, ripples are inevitable at the CP outputs, especially when the PLL is unlocked, so the CP output swings should be as large as possible, which increases CP complexity. Otherwise, the PLL's locking process

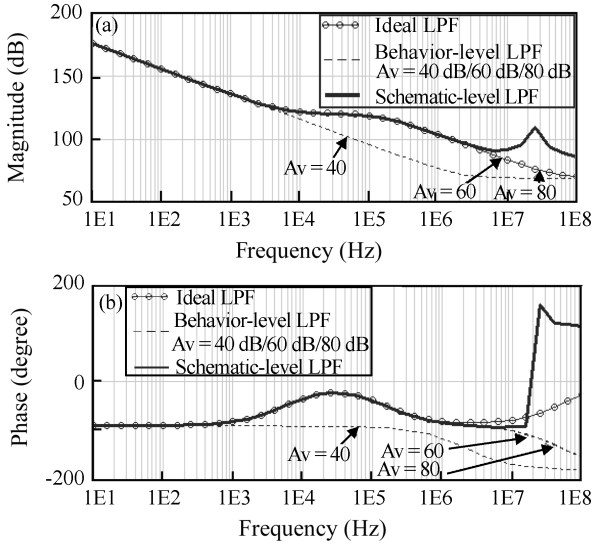

Fig. 4. AC simulation results of this LPF: (a) Magnitude; (b) Phase.

will be affected.

(3) For Fig. 3(c), both the CP output swings and the OPA input range should be rail-to-rail, so complexities of the CPs and the OPA will increase greatly[7].

(4) For Fig. 3(d), its low pass-path CP output is constant, which is helpful in minimizing the CP's current mismatch as well as the PLL's spurious tones. The only challenge in this design comes from its integration-path CP.

The proposed LPF is an active LPF, so the OPA's impacts should be analyzed. Assuming the OPA is a single-pole system, the LPF's transfer function can be calculated as

$$A(s) = \frac{A_0}{1 + s/p_0}, \tag{5}$$

$$\frac{V_c(s)}{I_{cp}(s)} = \frac{BR_1}{1 + sR_1C_1}\frac{A_0/(1 + A_0)}{1 + s/[(1 + A_0)p_0]} + \frac{1}{sC_2}. \tag{6}$$

Equation (6) indicates that the OPA's impacts on LPF transfer function can be omitted when its unity-gain-bandwidth (GBW) exceeds $1/R_1C_1$ greatly. Moreover, AC simulations are performed several times to make a further investigation. First, a behavior-level OPA instead of a circuit-level OPA is used in simulations. As shown in Fig. 4, when the OPA's GBW is set to 50 MHz, a 60 dB DC-gain is high enough to guarantee the LPF's correct function. Thus, as shown in Fig. 5, the OPA is realized by a two-stage OPA because of its moderate gain and large output swing even under a low supply voltage. Then, a schematic-level AC simulation is performed. From Fig. 4, it is clear that the schematic-level LPF based on our OPA works well below 10 MHz, which is enough for this narrow-ω_c PLL.

3. Charge-pumps for dual-path LPF

3.1. Lowpass-path charge-pump

As a current source, a CP's output impedance should be as high as possible. Consequently, in conventional CPs, cascode current mirrors are typically used because of their high

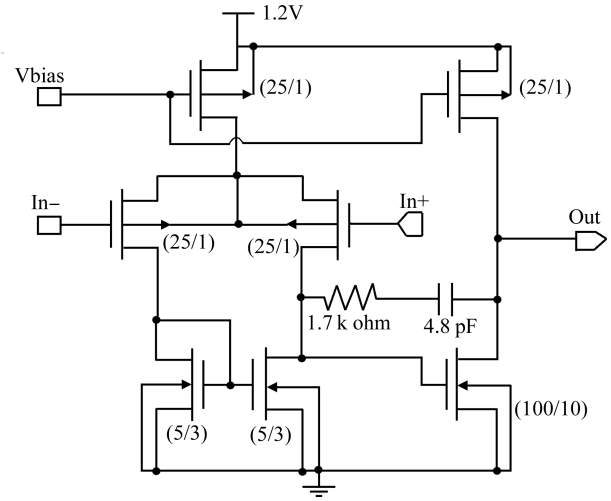

Fig. 5. Schematic of the OPA.

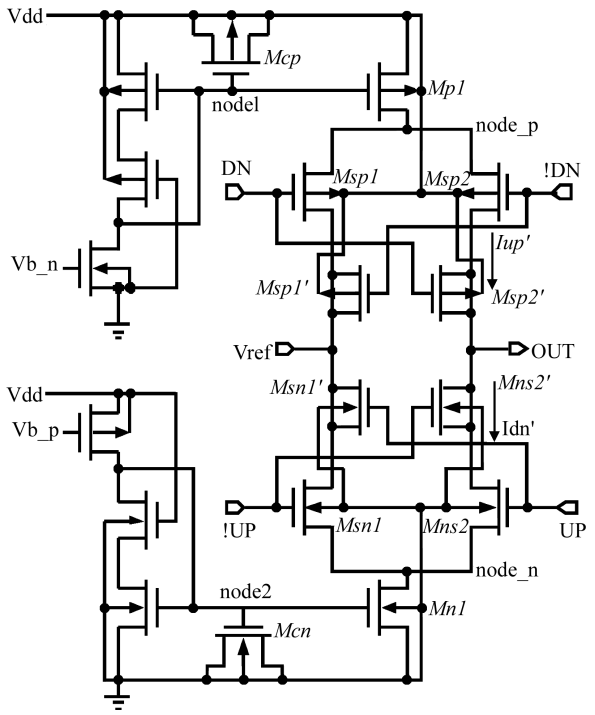

Fig. 6. Lowpass-path CP.

output impedance. But, in this design, because the lowpass-path CP's output is clamped at V_{ref} by the OPA, its output impedance will be infinite. Thus, cascode structures are not necessary any more, which is helpful in lowering this CP's supply voltage.

Similarly, unity-gain buffers are typically used to solve charge sharing effects between the output branch and the dummy branch[8]. Such a unity-gain buffer is usually realized by an OPA whose input range and output swing should be very large, especially under a low supply voltage. As a result, the CP's area, power, noise and complexity will increase excessively. But, in this design, because the output branch and the dummy branch are virtually short circuited by the OPA, the unity-gain buffer is needless. Thus, the unity-gain buffer mentioned above can be saved.

As shown in Fig. 6, MOS-capacitors (Mcp and Mcn) are

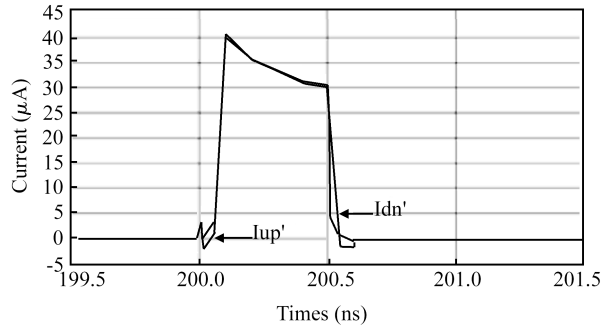

Fig. 7. Transient simulation results.

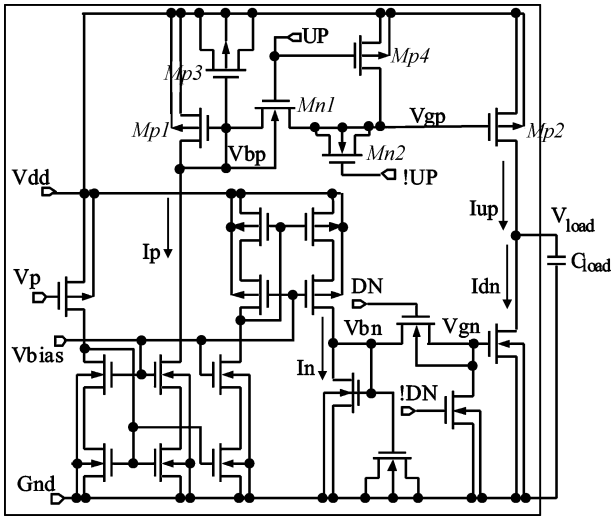

Fig. 8. Proposed integration-path CP.

used to filter high-frequency noise, and dummy switches (Msp1, Msp2, Msn1 and Msn2) are used to provide complementary charges so as to minimize the errors due to charge injection and clock feed-through[9]. When the PLL is locked, it is clear that the output currents (Iup and Idn) are perfectly matched even when the turn-on time is as narrow as 0.5 ns, as shown in Fig. 7.

3.2. Integration-path charge-pump

According to the analysis in section 2.2, the integration-path CP's output swing should be as large as possible. Thus, the VCO can cover a wide frequency range with a small gain (K_{vco}). Under a 1.2 V power supply, it is inadvisable to place switches in the current path because of the limited output swing[10]. In this design, switches are placed at the gates of the current mirrors, so the turnon/turnoff speed is just determined by the speed of charging/discharging the gate capacitors, as shown in Fig. 8. Taking the branch of I_{up} as an example, its working process is as follows.

(1) When the switch (Mn1) is turned on, charge will be redistributed between Mp1's gate and Mp2's gate, and the gate voltages (V_{bp} and V_{gp}) will not be stable until the redistribution is completed. As a result, establishment of I_{up} will be badly affected. To solve this, this paper proposes a charge-tank bias structure. In this design, a large MOS-capacitor (Mp3) is placed at Mp1's gate, which stores abundant charge so as to act

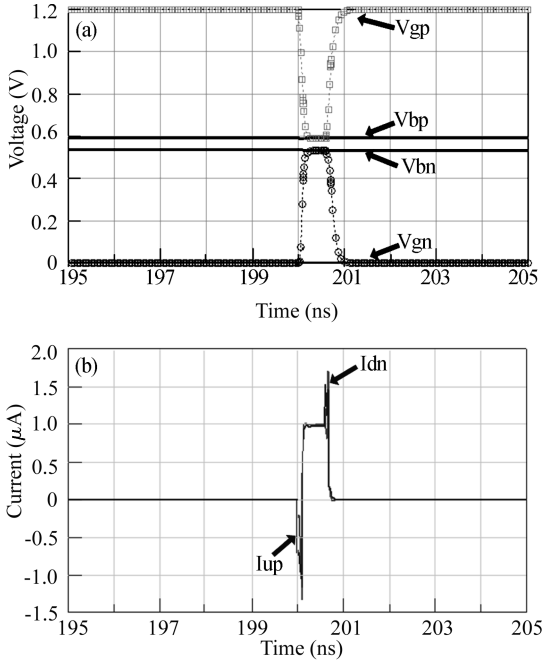

Fig. 9. Transient simulation results: (a) Node voltages; (d) Output currents.

as a tank of charge. Thus, V_{bp} will hardly be affected because the charge injected into Mp2's gate-capacitor is only a very small portion of that stored in the MOS-capacitor. It should be noted that an NMOS switch is preferred because of its smaller parasitical capacitance.

(2) When the switch (Mn1) is turned off, V_{gp} will be pulled up to V_{dd} by a PMOS switch (Mp4) immediately. Mn1's channel charge will inject into Mp2's gate-capacitor, and thus V_{gp}'s pull-up will be badly affected. To alleviate this channel charge injection, a dummy switch Mn2 is placed at Mp2's gate, which is the same as Mn1 but oppositely switched.

Figure 9 shows the CP transient simulation results. In this simulation, the CP's turn-on time is set to 0.5 ns on purpose in order to study its performance at a very high speed. As predicted above, V_{bp} is stable all the time and V_{gp} can establish its correct value rapidly without any ripples. Except for some glitches, it is clear that the up-current (I_{up}) matches the down-current (I_{dn}) perfectly. Because the glitches' fundamental-frequency power is so limited, they will not degrade the PLL's spur performance too much. This prediction will be verified by measurements in the next section.

Figure 10 shows the CP pumping-up and pumping-down waveforms of V_{load}. The dashed line marked with 'Ideal V_{load}' is also plotted so as to give a comparison between simulated waveforms and ideal waveforms. It is clear that the simulated waveforms match the ideal waveforms from 0.15 to 1.05 V perfectly. Under a 1.2 V supply voltage, such a large output swing is very beneficial to lower VCO gain without sacrificing the frequency range. It is also clear that the steps in the HOLD state are very flat, which indicates non-idealities are very limited[11].

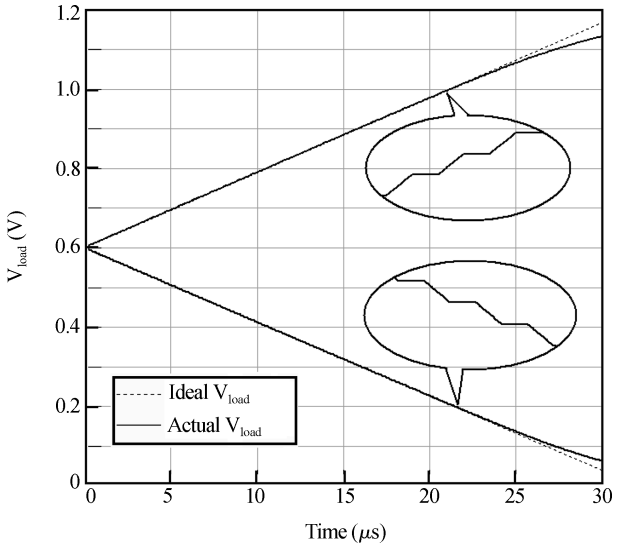

Fig. 10. Pumping-up and pumping-down waveforms of $V_{\rm load}$.

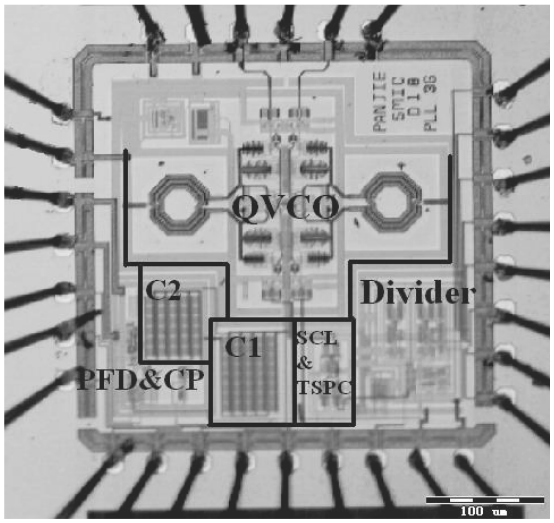

Fig. 11. Die photo of a 3.5 GHz-band PLL based on the proposed dual-path LPF.

4. Experimental results

A 1.2 V 3.5 GHz-band integer-N PLL based on this LPF is designed and fabricated in SMIC 0.18 μm RFCMOS technology. Because it is not used in frequency-hopping systems, a fast channel-switching speed is not necessary any more. Considering that the reference clock is 5 MHz and a small $\omega_{\rm c}$ is helpful in suppressing the reference spur, this PLL's $\omega_{\rm c}$ is set to 25 kHz. Such a small $\omega_{\rm c}$ is a big problem for a passive LPF; however, it is an easy task for the proposed dual-path LPF.

The chip occupies 1.2 × 1.2 mm^2, as shown in Fig. 11. It is clear that all the capacitors (C_1 is 32.2 pF and C_2 is 24.7 pF) only take up a very small portion of the whole chip. This chip is measured on an Agilent signal source analyzer (E5052A). Figures 12 and 13 show the PLL's measured phase noise and spectrum at 3.20 GHz respectively. Measured data show that the phase noise is –120.3 dBc/Hz at 1 MHz offset and the reference spur is about –72 dBc. It should be noted

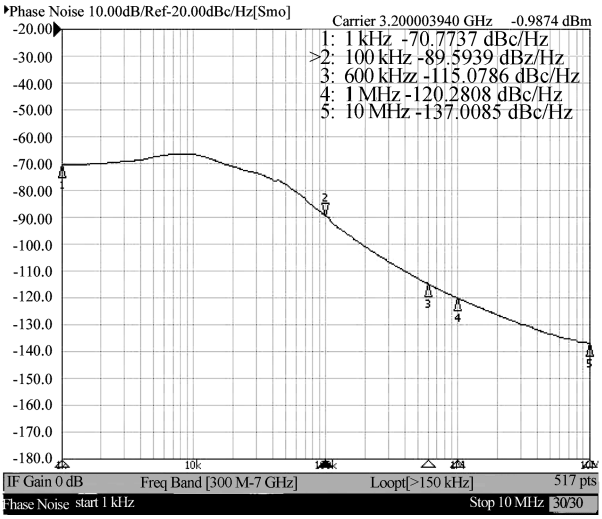

Fig. 12. Measured PLL phase noise at 3.20 GHz.

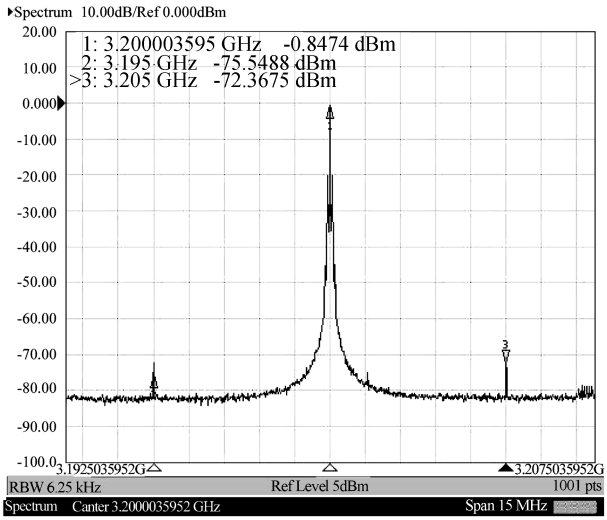

Fig. 13. Measured PLL spectrum at 3.20 GHz.

that measured in-band phase noise is about –71 dBc/Hz at 1 kHz offset, which indicates the OPA and the two CPs in this LPF contribute a great deal of noise to the loop. For the PLL whose in-band phase noise is not very critical, the proposed dual-path LPF will undoubtedly be a good solution to improve integration.

Table 2 shows a detailed performance comparison of the PLLs mentioned in Fig. 3. Among these PLLs, the proposed one shows the lowest power consumption, the second smallest chip size, and the second best phase noise, which demonstrates that the proposed LPF works well in the PLL.

5. Conclusions

In this paper, an area-saving dual-path LPF is proposed and analyzed in detail. It can magnify its zero-capacitance B times ($B > 1$) equivalently without any change of technology, and thus the chip size can be greatly reduced. Based on this LPF, a 3.5 GHz-band low-voltage PLL is fabricated and verified. Experimental results demonstrate that the proposed LPF is a good solution to improve integration.

Table 2. Performance comparison of PLLs mentioned in Fig. 3.

Reference	Process (μm)	ω_c (kHz)	Settling time (μS)	Phase noise (dBc/Hz)	Carrier frequency (GHz)	Area (mm^2)	Power (mW)	Quadrature output
Ref. [5]	0.4	45	< 300	–77 @ 1 kHz –123@1MHz	1.71	1.7 × 1.9	51 @ 3 V	none
Ref. [6]	0.18	50	51	–65@1kHz –111@1MHz	5.478	1.3 × 0.76	27.5 @ 1 V	Yes
Ref. [7]	0.35	1	< 800	–63@1kHz –120@1MHz	1.766	2.5 × 2.0	60 @ 3 V	none
This work	0.18	25	< 92	–71@1kHz –120@1MHz	3.20	1.2 × 1.2	24 @ 1.2 V	Yes

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